MUTHAYAMMAL ENGINEERING COLLEGE

An Autonomous Institution

(Approved by AICTE | Accredited by NBA & NAAC | Affiliated to Anna University)
Rasipuram - 637 408, Namakkal Dist., Tamil Nadu.

Curriculum/Syllabus

Programme Code : **VL**

Programme Name : **M.E.-VLSI DESIGN**

Regulation : **2023**

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Rasipuram - 637 408, Namakkal Dist., Tamil Nadu.

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Email: info@mec.ac.in

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Rasipuram - 637 408, Namakkal Dist., Tamil Nadu.

Estd. 2000

Institution Vision & Mission

Institution Vision

- To be a Centre of Excellence in Engineering, Technology and Management on par with International Standards.

Institution Mission

- To prepare the students with high professional skills and ethical values.
- To impart knowledge through best practices.
- To instill a spirit of innovation through Training, Research and Development.
- To undertake continuous assessment and remedial measures.
- To achieve academic excellence through intellectual, emotional and social stimulation.

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Department of Electronics and Communication Engineering
Muthayammal Engineering College (Autonomous)
Rasipuram, Namakkal - 637 408.

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Department Vision & Mission

Department Vision

- To empower the electronics and communication engineering students on basics and advanced technologies in both theoretical and experimental practices with research attitude and ethics.

Department Mission

- To impart need based in Electronics and communication engineering to meet the requirements of academic, industry and society
- To establish the state-of-art laboratories to prepare the students for facing the challenges ahead
- To prepare the students for employment, higher education and research oriented activities.

Program Educational Objectives

The Electronics and Communication Engineering Graduates should be able to

PEO1 : Graduate should be able to pursue as an Engineer with necessary conceptual, analytical and theoretical knowledge in the domain of Electronics and Communication Engineering

PEO2 : Graduate should be able to acquire the practical knowledge through basics and advanced laboratories in the field of Electronics and Communication Engineering

PEO3 : Graduate should be able to demonstrate the leadership skills through Entrepreneurship, Employment. And Higher studies and to practice ethical values for the benefit of Society and Environment

Program Specific Outcomes

PSO1 : Designandanalyzeelectroniccircuitsandsystemsforvariousapplications

PSO2 : Apply the acquired knowledge and analytical skills for modeling and simulation of advanced communication systems

PSO3 : Ascertain the use of software and hardware tools for developing variety of electronics and communication systems

Program Outcomes

PO1 : **Engineering Knowledge:** Apply the knowledge of mathematics, science, engineering fundamentals, and an engineering specialization to the solution of complex engineering problems.

PO2 : **Problem Analysis:** Identify, formulate, review research literature, and analyze complex engineering problems reaching substantiated conclusions using first principles of mathematics, natural sciences and Engineering sciences.

PO3 : **Design/Development solutions:** Design solutions for complex engineering problems and design system components or processes that meet the specified needs with appropriate consideration for the public health and safety, and the cultural, societal, and environmental considerations.

PO4 : **Conduct investigations of complex problems:** Use research-based knowledge and research methods including design of experiments, analysis and interpretation of data, and synthesis of the information to provide valid conclusions.

PO5 : **Modern tool usage:** Create, select, and apply appropriate techniques, resources, and modern engineering and IT tools including prediction and modeling to complex engineering activities with an understanding of the limitations.

PO6 : **The engineer and society:** Apply reasoning informed by the contextual knowledge to assess societal, health, safety, legal and cultural issues and the consequent responsibilities relevant to the professional engineering practice.

PO7 : **Environment and sustainability:** Understand the impact of the professional engineering solutions in societal and environmental contexts, and demonstrate the knowledge of, and need for sustainable development

PO8 : **Ethics:** Apply ethical principles and commit to professional ethics and responsibilities and norms of the engineering practice.

PO9 : **Individual and team work:** Function effectively as an individual and as a member or leader in diverse teams, and in multidisciplinary settings.

PO10 : **Communication:** Communicate effectively on complex engineering activities with the engineering community and with society at large, such as, being able to comprehend and write effective reports and design documentation, make effective presentations, and give and receive clear instructions.

PO11 : **Project management and finance:** Demonstrate knowledge and understanding of the engineering management principles and apply these to one's own work, as a member and leader in a team, to manage projects and in multidisciplinary environments.

PO12 : **Lifelong learning:** Recognize the need for and have the preparation and ability to engage in independent and lifelong learning in the broadest context of technological change.

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M.E-VLSI DESIGN

Grouping of Courses

I. Foundation Courses (FC)

Sl.No.	Course Code	Course Title	Category	Contact Hours	Instruction Hours/Week/ Credit			
					L	T	P	C
1.	23VLA01	Advanced Numerical Methods	FC	5	3	2	0	4
2.	23VLA02	Applied Mathematics	FC	5	3	2	0	4
3.	23VLA03	Applied Probability and Statistics	FC	5	3	2	0	4

II. Professional Core(PC)

1.	23VLB01	Solid State Electronics Device	PC	5	3	2	0	4
2.	23VLB02	Digital CMOS VLSI Design	PC	3	3	0	0	3
3.	23VLB03	Analog VLSI Circuit Design	PC	3	3	0	0	3
4.	23VLB04	FPGA Based Hardware Accelerators	PC	3	3	0	0	3
5.	23VLB05	VLSI Design Techniques	PC	3	3	0	0	3
6.	23VLB06	CAD for VLSI Circuits	PC	5	3	2	0	4
7.	23VLB07	Low Power VLSI Design	PC	3	3	0	0	3
8.	23VLB08	VLSI Circuit for Biomedical Application	PC	3	3	0	0	3
9.	23VLB09	Testing of VLSI Circuits	PC	3	3	0	0	3
10.	23VLB10	Mixed Signal VLSI Design	PC	3	3	0	0	3
11.	23VLB11	Electromagnetic Interference and Compatibility	PC	3	3	0	0	3
12.	23VLB12	Advanced MOSFET Modeling	PC	3	3	0	0	3
13.	23VLB13	Digital CMOS VLSI Design Laboratory	PC	2	0	0	2	1
14.	23VLB14	VLSI Design Techniques Laboratory	PC	2	0	0	2	1

III. Professional Electives(PE)

1.	23VLC01	Intelligent Optimization Techniques	PE	3	3	0	0	3
2.	23VLC02	Signal Integrity for High Speed Devices	PE	3	3	0	0	3
3.	23VLC03	Advanced Digital System Design	PE	3	3	0	0	3
4.	23VLC04	Submicron VLSI Design	PE	3	3	0	0	3
5.	23VLC05	VLSI Technology	PE	3	3	0	0	3
6.	23VLC06	DSP Integrated Circuits	PE	3	3	0	0	3

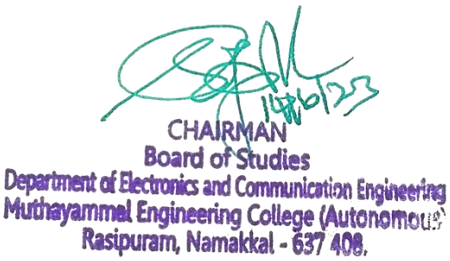
7.	23VLC07	ARM Processor and Applications	PE	3	3	0	0	3
8.	23VLC08	Hardware Design Verification Techniques	PE	3	3	0	0	3
9.	23VLC09	Design and Analysis of Algorithms	PE	3	3	0	0	3
10.	23VLC10	MEMS and NEMS	PE	3	3	0	0	3
11.	23VLC11	ASIC Design	PE	3	3	0	0	3
12.	23VLC12	VLSI for Wireless Communication	PE	3	3	0	0	3
13.	23VLC13	Research Methodology	PE	3	3	0	0	3
14.	23VLC14	ML for VLSI Design	PE	3	3	0	0	3
15.	23VLC15	RF Integrated Circuit Design	PE	3	3	0	0	3

IV. Employability Enhancement Courses(EEC)

1.	23VLD01	Project Work Phase-I	EEC	12	0	0	12	6
2.	23VLD02	Project Work Phase-II	EEC	24	0	0	24	12

V. Audit Courses(AC)

1.	23VLE01	English for Research Paper Writing	AC	2	2	0	0	0
2.	23VLE02	Disaster Management	AC	2	2	0	0	0
3.	23VLE03	Sanskrit for Technical Knowledge	AC	2	2	0	0	0
4.	23VLE04	Value Education	AC	2	2	0	0	0
5.	23VLE05	Constitution of India	AC	2	2	0	0	0
6.	23VLE06	Pedagogy Studies	AC	2	2	0	0	0
7.	23VLE07	Stress Management by Yoga	AC	2	2	0	0	0
8.	23VLE08	Personality Development through Life Enlightenment Skills.	AC	2	2	0	0	0



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M.E - VLSI DESIGN
Curriculum | PG - R2023
Semester -I

Sl.No.	Course Code	Course Title	Category	Contact Hours	Instruction Hours/Week/ Credit			
					L	T	P	C
Theory								
1.	23VLA02	Applied Mathematics	FC	4	3	0	3	3
2.	23VLB01	Solid State Electronics Device	PC	5	3	2	0	4
3.	23VLB02	Digital CMOS VLSI Design	PC	5	3	2	0	4
4.	23VLB03	Analog VLSI Circuit Design	PC	3	3	0	0	3
5.	23VLB04	FPGA Based Hardware Accelerators	PC	3	3	0	0	3
6.	23VLC14	ML for VLSI Design(Elective I)	PE	3	3	0	0	3
7.	23VLB13	Digital CMOS VLSI Design Laboratory	PC	3	3	0	0	3
							Total Credits	**21**

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Semester –II

Sl.No.	Course Code	Course Title	Category	Contact Hours	Instruction Hours/Week/ Credit			
					L	T	P	C
Theory								
1.	23VLB05	VLSI Design Techniques	PC	3	3	0	0	3
2.	23VLB06	CAD for VLSI Circuits	PC	5	3	2	0	4
3.	23VLB07	Low Power VLSI Design	PC	3	3	0	0	3
4.	23VLB08	VLSI Circuit for Biomedical Applications	PC	3	3	0	0	3
5.	23VLC13	Research Methodology(Elective II)	PE	3	3	0	0	3
6.	23VLC12	VLSI for Wireless Communication (Elective III)	PE	3	3	0	0	3
7.	23VLB14	VLSI Design Techniques Laboratory	PC	2	0	0	2	1
8.	23VLE01	English for Research Paper Writing (Audit Course 1)	AC	2	2	0	0	0
							Total Credit	**20**

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M.E - VLSI DESIGN
Curriculum | PG - R2023
Semester -III

Sl.No.	Course Code	Course Title	Category	Contact Hours	Instruction Hours/Week/ Credit			
					L	T	P	C
Theory								
1.	23VLC10	Intelligent Optimization Techniques (Elective IV)	PE	3	3	0	0	3
2.	23VLC15	RF Integrated Circuit Design(Elective V)	PE	3	3	0	0	3
3.	23PSC02	Microcontroller Based System Design (Open Elective I)	PE	3	3	0	0	3
4.	23VLE05	Constitution of India(Audit Course II)	AC	2	2	0	0	0
5.	23VLD01	Project Work Phase-I	EEC	12	0	0	12	6
							Total Credit	**15**

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M.E - VLSI DESIGN
Curriculum | PG - R2023

Semester -IV

Sl.No.	Course Code	Course Title	Category	Contact Hours	Instruction Hours/Week/ Credit			
					L	T	P	C
Theory								
1.	23VLD02	Project Work Phase-II	EEC	24	0	0	24	12
							Total Credit	**12**

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23VLA01	ADVANCED NUMERICAL METHODS	L	T	P	C
		3	2	0	4

Course Objective:

- To learn the algebraic equations which finds applications in many engineering branches.
- To make the student acquire sound knowledge of computational techniques in solving ordinary differential equations that model engineering.
- To solve Elliptic equations by using computational techniques.
- Tointroducenumericaltoolsforthesolutionsofpartialdifferentialequationsthatmodelseveralphysicalprocesses.
- To deal with interpolation and approximation for the application of finite element analysis.

Course Outcomes:

23VLA01.CO1	Demonstrate understanding and implementation of numerical solution algorithms applied to solve algebraic equations.
23VLA01.CO2	Be familiar with numerical solutions of ordinary differential equation and partial differential equations.
23VLA01.CO3	Be competent with finite difference method and finite element method.
23VLA01.CO4	Understanding the theoretical and practical aspects of the use of numerical methods. Implementing numerical methods for a variety of multidisciplinary applications. Establishing the limitations, advantages, and disadvantages of numerical methods.
23VLA01.CO5	The students will have a clear perception of the power of numerical Techniques. This will also serve as a precursor for future research.

Unit-I ALGEBRAIC EQUATIONS 9+6

Systems of linear equations: Gauss Elimination method, pivoting techniques, Thomas algorithm for tridiagonal system – Jacobi, Gauss Seidel, SOR iteration methods - Systems of nonlinear equations: Fixed point iterations, Newton Method, Eigenvalue problems: power method, inverse power method, Faddeev – Leverrier Method.

Unit-II ORDINARY DIFFERENTIAL EQUATIONS 9+6

Runge Kutta Meth ods for systemof IVPs, numerical stability, Adams - Bashforth multistep method, solution of stiff ODEs, shooting method, BVP: Finite difference method, orthogonal collocation method, orthogonal collocation with finite element method, galerkin finite element method.

Unit-III FINITE DIFFERENCE METHOD FOR TIME DEPENDENT PARTIAL DIFFERENTIAL EQUATIONS 9+6

Parabolic equations: explicit and implicit finite difference methods, weighted average approximation- Dirichlet and Neumann conditions– Two dimensional parabolic equations– ADI method; First order hyperbolic equations– method of characteristics, different explicit and implicitmethods; numerical stability analysis, method of lines– Wave equation: Explicit scheme - Stability of above schemes.

Unit-IV FINITE DIFFERENCE METHODS FOR ELLIPTIC EQUATIONS 9+6

Laplace and Poisson's equations in a rectangular region: Five point finite difference schemes, Leibmann's iterative methods, Dirichlet and Neumann conditions – Laplace equation in polar coordinates: finite difference schemes – approximation of derivatives near a curved boundary while using a square mesh.

Unit-V FINITE ELEMENT METHOD 9+6

Partial differential equations – Finite element method – orthogonal collocation method, orthogonal collocation with finite element method, Galerkin finite element method.

Total Periods: 45+30

Reference Books:

Sl.No.	Author(s)	Title of the Book	Publisher	Year of Publication
1.	M.K.Jain, S.R.K. Iyengar, R.K.Jain	Computational Methods for Partial Differential Equations, 2nd Edition	New Age Publishers	2019
2.	S.K. Gupta	Numerical Methods for Engineers, 3rd Edition	New Age International Pvt Ltd Publishers	2015
3.	Saumyen Guhaand Rajesh Srivastava	Numerical methods for Engineering and Science	Oxford Higher Education, New Delhi	2010
4.	M.K. Jain	Numerical Methods for Scientific & Engineering Computation, 6th Edition	New Age International Publishers	2010
5.	Burden,R.L., and Faires, J.D.	Numerical Analysis–Theory and Applications	Cengage Learning, India Edition, New Delhi	2009

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23VLA02	APPLIED MATHEMATICS	L	T	P	C
		3	2	0	4

Course Objective:

- To realize the use of matrix theory techniques in engineering applications and to develop for future applications.
- To analyze and solve the fundamental problem with prescribed or free boundary conditions in simple cases.
- Demonstrate knowledge of mathematics and mechanics to construct, analyze and interpret real world problems.
- Provide a foundation and motivation for exposure to statistical ideas subsequent to the course.
- To formulate and construct a mathematical model for a linear programming problem in real life situation.

Course Outcomes:

23VLA02.CO1	Explain geometrical concepts related to orthogonality and least squares solutions and perform calculations related to orthogonality.
23VLA02.CO2	The variation calculus makes access to mastering in a wide range of classical results of variational calculus. Students get up apply results in technical problem solutions.
23VLA02.CO3	The students will have a basic knowledge of the main fields of mathematics and mechanics, including differential equations, elasticity theory, fluid mechanics.
23VLA02.CO4	The students will have an exposure of various distribution functions and help in acquiring skills in handling situations involving more than one variable.
23VLA02.CO5	The knowledge gained on this course helps the students to do engineering optimization.

Unit-I MATRIX THEORY 9+6

The Cholesky decomposition - Generalized Eigen vectors, Canonical basis - QR factorization - Least squares method - Singular value decomposition.

Unit-II CALCULUS OF VARIATIONS 9+6

Concept of variation and its properties – Euler's equation – Functional dependant on first and higher order derivatives – Functionals dependant on functions of several independent variables – Variational problems with moving boundaries – problems with constraints - Direct methods: Ritz and Kantorovich methods.

Unit-III ONE DIMENSIONAL RANDOM VARIABLES 9+6

Random variables-Probability function – moments– moment generating functions and their properties – Binomial, Poisson, Geometric, Uniform, Exponential, Gamma and Normal distributions – Function of a Random Variable.

Unit-IV LINEAR PROGRAMMING 9+6

Formulation–Graphical solution–Simplex method–Two phase method-Transportation and Assignment Models.

Unit-V FOURIER SERIES AND EIGEN VALUE PROBLEMS 9+6

Fourier Trigonometric series: Periodic function as power signals – Convergence of series – Even and odd function: cosine and sine series – Non-periodic function: Extension to other intervals - Power signals: Exponential Fourier series – Parseval's theorem and power spectrum – Eigen value problems and orthogonal functions – Regular Sturm-Liouville systems – Generalized Fourier series.

Total Periods: 45+30

Reference Books:

Sl.No.	Author(s)	Title of the Book	Publisher	Year of Publication
1.	Mital.K.V.Mohan and Chander	Optimization Methods in Operations Research and Systems Analysis, 4th Edition	New Age International Publishers	2019
2.	Stark.H., and Woods. J.W.	Probability and Random Processes with ApplicationstoSignalProcessing,4th Edition	Pearson Education, Asia	2014
3.	Hamdy A Taha	OperationsResearch,9th Edition(Asia)	Pearson Education, Asia	2014
4.	Gupta,A.S.	Calculus of Variations with Applications	Prentice Hall of India Pvt. Ltd., New Delhi	2011
5.	Richard Bronson	Matrix Operation, Schaum's outline series, 2nd Edition	McGraw Hill	2011

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23VLA03	APPLIED PROBABILITY AND STATISTICS	L	T	P	C
		3	2	0	4

Course Objective:

- To introduce the basic concepts of one dimensional and two dimensional Random Variables.
- To gain knowledge in the application of family of random variables in real life situations.
- To provide information about Correlation and Regression.
- Learn about maximum likelihood estimation, unbiased estimation and least square methods.
- To understand concepts of testing of hypothesis.

Course Outcomes:

23VLA03.CO1	Analyze random or unpredictable experiments and investigate important features of random experiments. Construct probabilistic models for observed phenomena through distributions which play an important role in many engineering applications.
23VLA03.CO2	Associate random variables by designing joint distributions and correlate the random variables.
23VLA03.CO3	Perform and interpret correlation and regression analysis and develop correlation models to predict changes in processes and products for linear and non-linear relationships.
23VLA03.CO4	Provides knowledge to apply testing of hypothesis to real life problems.
23VLA03.CO5	Be familiar with multivariate analysis.

Unit-I ONE DIMENSIONAL RANDOM VARIABLES 9+6

Randomvariables-Probabilityfunction–Moments–Momentgeneratingfunctionsandtheirproperties–Binomial, Poisson, Geometric, Uniform, Exponential, Gamma and Normal distributions – Functions of a Random Variable.

Unit-II TWO DIMENSIONAL RANDOM VARIABLES 9+6

Joint distributions – Marginal and Conditional distributions – Functions of two dimensional random variables – Regression Curve – Correlation.

Unit-III ESTIMATION THEORY 9+6

Unbiased Estimators –Method of Moments –Maximum Likelihood Estimation -Curve fitting by Principle of least squares – Regression Lines.

Unit-IV TESTING OF HYPOTHESES 9+6

Sampling distributions - Type I and Type II errors - Tests based on Normal, t, Chi-Square and F distributions for testing of mean, variance and proportions – Tests for Independence of attributes and Goodness of fit.

Unit-V MULTIVARIATE ANALYSIS 9+6

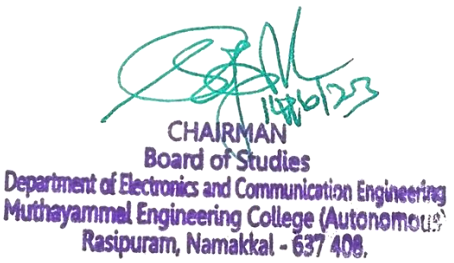
Random Vectors and Matrices- Mean vectors and Covariance matrices-Multivariate Normal density and its properties- Principal components Population principal components – Principal components from standardized variables.

Total Periods: 45+30

Reference Books:

Sl.No.	Author(s)	Title of the Book	Publisher	Year of Publication
1.	Douglas C. Montgomery, George C.Runger	Applied Statistics and Probability for Engineers (International Student Version),6th Edition	John Wiley & Sons, Inc.	2019
2.	Richard A. Johnson andDeanW.Wichern	Applied Multivariate StatisticalAnalysis,6th Edition	Pearson Education, Asia	2015

3.	GuptaS.C.and Kapoor V.K	Fundamentals of Mathematical Statistics	Sultan Chand &Sons	2014
4.	HweiP.Hsu,	Schaum‟s Outline of Theory and Problems of Probability, Random Variables and Random Processes	Tata McGraw Hill Edition, New Delhi	2014
5.	Walpole. R.E., Myers.R.H., Myers. S.L., and Ye.K.,,	Probability and Statistics for Engineers and Scientists, 8thEdition	Pearson Education, Asia	2013



23VLB01	SOLID STATE DEVICE MODELING	L	T	P	C
		3	0	0	3

Course Objective:

- To know the basics of Quantum mechanics.
- To understand the concept bipolar device modeling.
- To gain knowledge on MOSFET modeling.
- To study the measurement of transistor parameters.
- To gain knowledge on optoelectronics device modeling.

Course Outcomes:

23VLB01.CO1	Explain the basics of Quantum mechanics.
23VLB01.CO2	Explain the various BJT models.
23VLB01.CO3	Explain the modeling of MOSFET.
23VLB01.CO4	Analyze the transistor parameters.
23VLB01.CO5	Explain the process of modeling optoelectronic devices.

Unit-I SEMICONDUCTOR PHYSICS 9

Quantum Mechanical Concepts, Carrier Concentration, Transport Equation, Band gap, Mobility and Resistivity, Carrier Generation and Recombination, Avalanche Process,Noise Sources-Diodes: Forward and Reversebiased junctions –Reverse bias breakdown –Transient and AC conditions -Static and Dynamic behavior-Small and Large signal models –SPICE model for a Diode –Temperature and Area effects on Diode Model Parameters.

Unit-II BIPOLAR DEVICE MODELING 9

Transistor Models: BJT –Transistor Action–Minority carrier distribution and Terminal currents -Switching-Eber –Molls and Gummel Poon Model, SPICE modeling -temperature and area effects.

Unit-III MOSFET MODELING 9

OS Transistor –NMOS, PMOS –MOS Device equations -Threshold Voltage –Second order effects -Temperature Short Channel and Narrow Width Effect, Models for Enhancement, Depletion Type MOSFET, CMOS Models in SPICE.

Unit-IV PARAMETER MEASUREMENT 9

Bipolar Junction Transistor Parameter –Static Parameter Measurement Techniques – Large signal parameter Measurement Techniques, Gummel Plots, MOSFET: Long and Short Channel Parameters, Measurement of Capacitance.

Unit-V OPTOELECTRONIC DEVICE MODELING 9

Static and Dynamic Models, Rate Equations, Numerical Technique, Equivalent Circuits, Modeling of LEDs, Laser Diode and Photo detectors.

Total Periods: 45

Reference Books:

Sl.No.	Author(s)	Title of the Book	Publisher	Year of Publication
1.	Ben.G.Streetman	Solid State Devices	Prentice Hall	1997
2.	Giuseppe Massobrio and Paolo Antogentti	Semiconductor Device Modeling with SPICE, Second Edition,	McGraw-HillI nc, New York	1993
3.	Mohammed Ismail & Terri Fiez	Analog VLSI-Signal & Information Processing 1st Edition	Tata McGraw Hill Publishing Company Ltd	2001
4.	RoulstonE.J.,	Bipolar Semiconductor Devices	Mc-Graw Hill	1990
5.	Tor.A.Fijedly	Introduction to Device Modelling and Circuit Simulation	Wiley-interscience	1997

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		L	T	P	C
23VLB02	**DIGITAL CMOS VLSI DESIGN**	**3**	**0**	**0**	**3**

Course Objective:

- To deal comprehensively with all aspects of transistor level design of all the digital building blocks.
- To focus on the transistor level design.
- To address all important issues related to size, speed and power consumption.
- To deal with the memory architectures.
- To know the interconnect and clocking strategies.

Course Outcomes:

23VLB02.CO1	Able to carry out transistor level hand calculation.
23VLB02.CO2	Able to design most important building blocks used in digital CMOS VLSI circuits.
23VLB02.CO3	Able to develop strong understanding of the design methodology.
23VLB02.CO4	Able to develop tradeoffs of the various circuit choices for each of all the blocks discussed.
23VLB02.CO5	Able to know the interconnect and clocking strategies.

Unit-I MOS TRANSISTOR PRINCIPLES AND CMOS INVERTER 9

MOS(FET) Transistor Characteristic under Static and Dynamic Conditions, (Add)MOS device Design equation, MOS Transistor Secondary Effects, Process Variations, Technology Scaling, CMOS Inverter - Static Characteristic, Dynamic Characteristic, Power, Energy, and Energy Delay parameters,(Add) Tristate inverters.

Unit-II COMBINATIONAL LOGIC CIRCUITS 9

Propagation Delays, Stick diagram, Layout diagrams, Examples of combinational logic design, Elmore's constant, Dynamic Logic Gates, Pass Transistor Logic, Power Dissipation, Low Power Design principles.

Unit-III SEQUENTIAL LOGIC CIRCUITS 9

Static Latches and Registers, Dynamic Latches and Registers, Timing Issues, Pipelines, Pulse and sense amplifier based Registers, Non bistable Sequential Circuits.

Unit-IV ARITHMETIC BUILDING BLOCKS AND MEMORY ARCHITECTURES 9

Data path circuits, Architectures for Adders, Accumulators, Multipliers, Barrel Shifters, Speed and Area Tradeoffs, Memory Architectures, and Memory control circuits.

Unit-V INTERCONNECT AND CLOCKING STRATEGIES 9

Interconnect Parameters – Capacitance, Resistance, and Inductance, Electrical Wire Models, Timing classification of Digital Systems, Synchronous Design, Self-Timed Circuit Design.

Total Periods: 45

Reference Books:

Sl.No.	Author(s)	Title of the Book	Publisher	Year of Publication
1.	Jan Rabaey, Anantha Chandrakasan, B Nikolic	Digital Integrated Circuits: A Design Perspective	Pentice Hall of India.	2003
2	N. Weste, K. Eshraghian	Principles of CMOS VLSI Design	Addision Wesley	1993

3.	MJ Smith	Application Specific Integrated Circuits	Addisson Wesley	1997
4.	David A. Hodges, Horace G.Jackson, and Resve A. Saleh	Analysis and Design of Digital Integrated Circuits	McGraw-Hill	2004
5.	Ken Martin	Digital Integrated Circuit Design	Oxford University Press	2000

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23VLB03	ANALOG VLSI CIRCUIT DESIGN	L	T	P	C
		3	0	0	3

Course Objective:

- To study the concepts of CMOS and BICMOS analog circuits.
- To understand the concepts of A/D convertors and analog integrated sensors.
- To understand the testing concepts in analog VLSI circuits and its statistical modeling.
- To understand the concepts of VLSI interconnects.
- To impart in-depth knowledge about switched capacitors, ADCs and DACs.

Course Outcomes:

23VLB03.CO1	To be able to know the concepts of CMOS and BICMOS analog circuits.
23VLB03.CO2	To be able to understand the concepts of A/D convertors and analog integrated sensors.
23VLB03.CO3	To be able to understand the testing concepts in analog VLSI circuits and its statistical modeling.
23VLB03.CO4	To be able to analyze VLSI interconnects.
23VLB03.CO5	To be able to impart in-depth knowledge about switched capacitors, ADCs and DACs.

Unit-I **BASIC CMOS CIRCUIT TECHNIQUES, CONTINUOUS TIME AND LOW VOLTAGE SIGNAL PROCESSING** **9**

Mixed-Signal VLSI Chips - Basic CMOS Circuits – Basic Gain Stage - Gain Boosting Techniques – Super MOS Transistor- Primitive Analog Cells-Linear Voltage-Current Converters –MOS Multipliers and Resistors-CMOS, Bipolar and Low- Voltage Bi CMOS Op- Amp Design-Instrumentation Amplifier Design-Low Voltage Filters.

Unit-II **BASICBICMOSCIRCUITTECHNIQUES,CURRENT-MODESIGNALPROCESSINGAND NEURAL INFORMATION PROCESSING** **9**

Continuous-Time Signal Processing-Sampled-Data Signal Processing-Switched-Current Data Converters-Practical Considerations in SI Circuits Biologically-Inspired Neural Networks - Floating - Gate, Low-Power Neural Networks-CMOS Technology and Models-Design Methodology-Networks-Contrast Sensitive Silicon Retina.

Unit-III **SAMPLED-DATA ANALOGFILTERS, OVER SAMPLED A/D CONVERTERS AND ANALOG INTEGRATED SENSORS** **9**

First-order and Second SC Circuits-Bilinear Transformation - Cascade Design-Switched-Capacitor Ladder Filter-Synthesis of Switched-Current Filter- Nyquist rate A/D Converters-Modulators for Over sampled A/D Conversion-First and Second Order and Multibit Sigma-Delta Modulators-Interpolative Modulators–Cascaded Architecture-Decimation Filters, mechanical, Thermal, Humidity and Magnetic Sensors Sensor Interfaces.

Unit-IV **DESIGN FOR TESTABILITY AND ANALOG VLSI INTERCONNECTS** **9**

Fault modeling and Simulation -Testability-Analysis Technique-AdHoc Methods and General Guidelines-Scan Techniques- Boundary Scan-Built-in Self Test-Analog Test Buses- Design for Electron -Beam Testability-Physics of Interconnects in VLSI-Scaling of Interconnects-A Model for Estimating Wiring Density-A Configurable Architecture for Prototyping Analog Circuits.

Unit-V **STATISTICAL MODELING AND SIMULATION** **9**

Review of Statistical Concepts - Statistical Device Modeling- Statistical Circuit Simulation- Automation Analog Circuit Design-automatic Analog Layout-CMOS Transistor Layout- Resistor Layout-Capacitor Layout-Analog Cell Layout-Mixed Analog -Digital Layout.

Total Periods: 45

Reference Books:

Sl.No.	Author(s)	Title of the Book	Publisher	Year of Publication
1.	Mohammed Ismail, Terri Fief	Analog VLSI signal and Information Processing	McGraw-Hill	1994
2.	Malcom R. Haskard, Lan C. May	Analog VLSI Design-NMOS and CMOS	Prentice Hall	1998
3.	Randall L Geiger, Phillip E. Allen, Noel K. Strader	VLSI Design Techniques for Analog and Digital Circuits	McGraw Hill	1990
4.	Jose E. France, Yannis T sividis	Design of Analog-Digital VLSI Circuits for Telecommunication and signal Processing	Prentice Hall	1994
5.	Philip Allen &D. Holberg	CMOS Analog Circuit Design	Oxford University Press	2002

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23VLB04	FPGA BASED HARDWARE ACCELERATORS	L	T	P	C
		3	0	0	3

Course Objective:

- To understand the design techniques of FPGA.
- To know the core architectures of searching networks.
- To know the core architectures of sorting networks.
- To deal with FPGA for solving computational problems.
- To gain knowledge on co-design using Zynq.

Course Outcomes:

23VLB04.CO1	Explain the design techniques of FPGA.
23VLB04.CO2	Explain the core architecture of searching networks for data search.
23VLB04.CO3	Explain the core architecture of sorting networks.
23VLB04.CO4	Use FPGA for solving computational problems.
23VLB04.CO5	Use Zynq for co-design.

Unit-I FPGA DESIGN TECHNIQUES 9

FPGA and SoC - Design and Prototyping - Design Methodology - Basic objectives and requirements of hardware accelerators - Combinational Versus Sequential Circuits - Core Architectures of FPGA-Based Hardware Accelerators - Design and Implementation of FPGA-Based Hardware Accelerators.

Unit-II FPGAS FOR DATA SEARCH 9

Core Architectures of Searching Networks - Modeling Searching Networks in Software - Implementing Searching Networks in Hardware - Search in Large Data Sets – Pipelining - Frequent Items Computations with the Address-Based Technique - Frequent Items Computations for a Set of Sorted Data Items.

Unit-III FPGAS FOR DATA SORT 9

Core Architectures of Sorting Networks - Modeling Sorting Networks in Software - Implementing Sorting Networks in Hardware - Extracting Sorted Subset - Modeling Networks for Data Extraction and Filtering in Software - Processing Non- repeated Values - Address-Based Data Sorting - Data Sorting with Ring Pipeline.

Unit-IV FPGAS FOR COMPUTATIONAL PROBLEMS 9

Counting Networks - Low-Level Designs from Elementary Logic Cells - Very Fast and Economical Hamming Weight Counter - Arithmetical Units and Mixed Solutions - LUT Functions Generator.

Unit-V CO-DESIGN 9

Hardware/Software Partitioning - Hardware/Software Co-design using Zynq - Managing Priorities - Managing Complexity - Processing and Filtering Table Data.

Total Periods: 45

Reference Books:

Sl.No.	Author(s)	Title of the Book	Publisher	Year of Publication
1.	Iouliia Skliarova, Valery Sklyarov	FPGA-BASEDHardware Accelerators	Springer	2019

23VLB05	VLSI DESIGN TECHNIQUES	L	T	P	C
		3	0	0	3

Course Objective:

- To understand the concepts of MOS transistors operations and their AC and DC characteristics.
- To know the fabrication process of CMOS technology and its layout design rules.
- To understand the latch up problem in CMOS circuits.
- To study the concepts of CMOS invertors and their sizing methods.
- To know the concepts of power estimation and delay calculations in CMOS circuits.
- To study the concepts of digital VLSI circuits.

Course Outcomes:

23VLB05.CO1	To be able to understand the concepts of MOS transistors operations and their AC and DC characteristics.
23VLB05.CO2	To be able to know the fabrication process of CMOS technology and its layout design rules.
23VLB05.CO3	To be able to understand the latch up problem in CMOS circuits.
23VLB05.CO4	To be able to know the concepts of CMOS invertors and their sizing methods.
23VLB05.CO5	To be able to know the concepts of power estimation and delay calculations in CMOS circuits.

Unit-I MOS TRANSISTOR THEORY 9

NMOS and PMOS transistors, CMOS logic, MOS transistor theory – Introduction, Enhancement mode transistor action,Ideal I-V characteristics, DC transfer characteristics, Threshold voltage- Body effect- Design equations-Second ordereffects. MOS models and small signal AC characteristics, Simple MOS capacitance Models, Detailed MOS gate capacitance model, Detailed MOS Diffusion capacitance mode.

Unit-II CMOS TECHNOLOGY AND DESIGN RULE 9

CMOS fabrication and Layout, CMOS technologies, P -Well process, N -Well process, twin –tub process, MOS layers stick diagrams and Layout diagram, Layout design rules, Latch up in CMOS circuits, CMOS process enhancements, Technology – related CAD issues, Fabrication and packaging.

Unit-III INVERTERS AND LOGIC GATES 9

NMOS and CMOS Inverters, Inverter ratio, DC and transient characteristics , switching times, Super buffers, Driving large capacitance loads, CMOS logic structures , Transmission gates, Static CMOS design, dynamic CMOS design.

Unit-IV CIRCUIT CHARACTERISATION AND PERFORMANCE ESTIMATION 9

Resistance estimation, Capacitance estimation, Inductance, switching characteristics, transistor sizing, power dissipation and design margining, Charge sharing, Scaling.

Unit-V VLSI SYSTEM COMPONENTS CIRCUITS AND SYSTEM LEVEL PHYSICAL DESIGN 9

Multiplexers, Decoders, comparators, priority encoders, Shift registers. Arithmetic circuits – Ripple carry adders, Carry look ahead adders, High-speed adders, Multipliers. Physical design – Delay modeling, cross talk, floor planning, power distribution. Clock distribution. Basics of CMOS testing.

Total Periods: 45

Reference Books:

Sl.No.	Author(s)	Title of the Book	Publisher	Year of Publication
1.	Neil H. E. Weste and Kamran Eshraghian	Principles of CMOS VLSI Design	Pearson EducationASIA,2nd edition	2000
2.	John P. Uyemura	Introduction to VLSI Circuits and Systems	John Wiley & Sons, Inc.	2002
3.	Eugene D. Fabricius	Introduction to VLSI Design	McGraw Hill International Editions	1990
4.	Pucknell	Basic VLSI Design	Prentice Hall of India Publication	1995
5.	Wayne Wolf	Modern VLSI Design System on chip	Pearson Education	2002

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23VLB06	CAD FOR VLSI CIRCUITS	L	T	P	C
		3	2	0	4

Course Objective:

- To introduce the basic CAD algorithm.
- To understand the Partitioning.
- To study about Placement, Floor Planning.
- To learn about Global, Detail routing.
- To know the Modeling and synthesis in CAD flow.
- To understand the High level transformations.

Course Outcomes:

23VLB06.CO1	Learn the Fundamentals of basic algorithm in CAD.
23VLB06.CO2	Study the different partitioning algorithm.
23VLB06.CO3	Understand the floor planning and placement algorithm.
23VLB06.CO4	Learn about different routing algorithms.
23VLB06.CO5	Know about modeling and synthesis techniques of CAD.

Unit-I VLSIDESIGNMETHODOLOGIES **9**

Introduction to VLSI Design methodologies - Review of Data structures and algorithms - Review of VLSI Design automation tools - Algorithmic Graph Theory and Computational Complexity – Tractable and Intractable problems – general purpose methods for combinatorial optimization.

Unit-II DESIGNRULES **9**

Layout Compaction - Design rules - problem formulation - algorithms for constraint graph compaction - placement and partitioning - Circuit representation – Placement algorithms – partitioning.

Unit-III FLOORPLANNING **9**

Floor planning concepts - shape functions and floor plan sizing - Types of local routing problems - Area routing - channel routing - global routing - algorithms for global routing

Unit-IV SIMULATION **9**

Simulation - Gate-level modeling and simulation - Switch-level modeling and simulation - Combinational Logic Synthesis - Binary Decision Diagrams – Two Level Logic Synthesis

Unit-V MODELLINGANDSYNTHESIS **9**

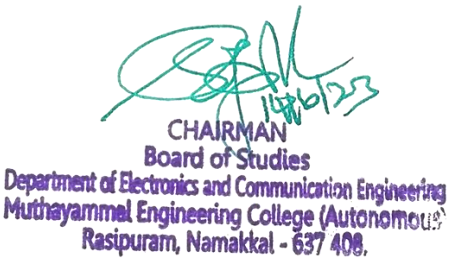
High level Synthesis - Hardware models - Internal representation - Allocation - assignment and scheduling - Simple scheduling algorithm – Assignment problem - High level transformations.

Total Periods: 45

Reference Books:

Sl.No.	Author(s)	Title of the Book	Publisher	Year of Publication
1.	S. H .Gerez	Algorithms for VLSI Design Automation	John Wiley & Sons	2002
2.	N. A. Sherwani	Algorithms for VLSI Physical Design Automation	Kluwer Academic Publishers	2002

3.	Giovanni De Micheli	Synthesis and Optimization of Digital Circuits	Tata McGraw Hill	1994
4.	M. Sarrafzadeh and C.K.Wong	An Introduction to VLSI Physical Design	McGraw Hill	1996
5.	Samir Palnitkar	Verilog HDL	Sun Microsystems Press A Prentice Hall Title	2001



23VLB07	LOWPOWERVLSIDESIGN	L	T	P	C
		3	0	0	3

Course Objective:

- To understand different sources of power dissipation in CMOS & MIS structure.
- To understand the different types of low power adders and multipliers
- To focus on synthesis of different level low power transforms.
- To gain knowledge on low power static RAM architecture & the source of power dissipation in SRAM
- To understand the various energy recovery techniques used in low power design
- To understand the Special techniques of low power VLSI design

Course Outcomes:

23VLB07.CO1	An ability to analyze different source of power dissipation and the factors involved in.
23VLB07.CO2	Able to understand the different techniques involved in low power adders and multipliers
23VLB07.CO3	Understandings of the impact of various low power transform
23VLB07.CO4	An ability to identify and analyze the different techniques involved in low power SRAM.
23VLB07.CO5	Able to understand various energy recovery techniques.

Unit-I POWER DISSIPATION **9**

Hierarchy of limits of power – Sources of power consumption – Physics of power dissipation in CMOS FET devices – Basic principle of low power design. (Add) Power dissipation in Domino CMOS- Low power VLSI design limits

Unit-II POWER OPTIMIZATION **9**

Logic level power optimization – Circuit level low power design – circuit techniques for reducing power consumption in adders and multipliers.

Unit-III DESIGN OF LOW POWER CIRCUITS **9**

Computer arithmetic techniques for low power system – reducing power consumption in memories – low power clock, Inter connect and layout design – Advanced techniques –Special techniques.

Unit-IV POWER ESTIMATION **9**

Power Estimation technique – logic power estimation – Simulation power analysis –Probabilistic power analysis, (Add) Modeling of signals- Signal probability calculation.

Unit-V SYNTHESIS AND SOFTWARE DESIGN **9**

Synthesis for low power – Behavioral level transform – software design for low power overlap and digital correction.

Total Periods: 45

Reference Books:

Sl.No.	Author(s)	Title of the Book	Publisher	Year of Publication
1.	Kaushik Roy and S.C.Prasad	Low power CMOS VLSI circuit design	Wiley	2000
2.	Dimitrios Soudris, Christians Pignet, Costas Goutis	Designing CMOS Circuits for Low Power	Kluwer	2002
3.	J.B.Kulo and J.H Lou	J.B.Kulo and J.H Lou	Wiley	1999
4.	A.P.Chandrasekaran and R.W.Broadersen	Low power digital CMOS design	Kluwer	1995
5.	Gary Yeap	Practical low power digital VLSI design	Kluwer	1998

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23VLB08	VLSI CIRCUITS FOR BIOMEDICAL APPLICATIONS	L	T	P	C
		3	0	0	3

Course Objective:

- To study the biomedical amplifiers, filters and analog to digital converters.
- To understand the structure and operation of implantable medical devices.
- To get an overview on non-invasive medical electronics.
- To review the ultra-low-power analog and digital design principles.
- To discuss the energy-harvesting circuits and energy sources
- To study the biomedical amplifiers, filters and analog to digital converters.

Course Outcomes:

23VLB08.CO1	Design biomedical amplifiers, filters and analog to digital converters.
23VLB08.CO2	Explain the concept of implantable medical devices
23VLB08.CO3	Understand the noninvasive medical electronics.
23VLB08.CO4	Analyse the ultra-low-power analog and digital design principles.
23VLB08.CO5	Contribute to the development energy-harvesting circuits for biomedical devices.

Unit-I LOW-POWER ANALOG BIOMEDICAL CIRCUITS 9

Low power trans impedance amplifiers and photoreceptors, Low power trans conductance amplifiers and scaling laws for power in analog circuits, Low-power filters and resonators, Low power current - mode circuits, Ultra-low- power and neuron-inspired analog-to-digital conversion for biomedical system

Unit-II ULTRA LOW POWER IMPLANTABLE MEDICAL ELECTRONICS 9

Introduction, Cochlear implants or bionic ears, An ultra-low-power programmable analog bionic ear processor, Low- power electrode stimulation, Highly miniature electrode-stimulation circuits, Brain machine interfaces for the blind, Brain-machine interfaces for paralysis, speech, and other disorders

Unit-III ULTRA-LOW-POWER NONINVASIVE MEDICAL ELECTRONICS 9

Introduction, Analog integrated-circuit switched-capacitor model of the heart, the electrocardiogram, a micro power electrocardiogram amplifier, Low-power pulse oximetry, Battery-free tags for body sensor networks, Intra-body galvanic communication networks, Bio molecular sensing

Unit-IV PRINCIPLES FOR ULTRA LOW POWER ANALOG AND DIGITAL DESIGN 9

Sizing and topologies for robust sub threshold operation digital design, Types of power dissipation, Energy efficiency and optimization in digital systems, Varying the power-supply voltage and threshold voltage, Gated clocks, Basics of adiabatic computing, Architectures and algorithms for improving energy efficiency, Power consumption in analog and digital systems, The optimum point for digitization in a mixed-signal system, The Shannon limit for energy efficiency, Collective analog or hybrid computation, HSMs: general-purpose mixed-signal systems with feedback - General principles for low-power mixed-signal system design, Sensors and actuators.

Unit-V ENERGY-HARVESTING CIRCUITS AND ENERGY SOURCES 9

Wireless inductive power links for medical implants, Energy-harvesting RF antenna power links, Low power RF telemetry in biomedical implants, Batteries and electrochemistry, Energy harvesting and the future of energy.

Total Periods: 45

Reference Books:

Sl.No.	Author(s)	Title of the Book	Publisher	Year of Publication
1.	Rahul Sarpeshkar	Ultra Low Power Bioelectronics: Fundamentals, Biomedical Applications, and Bio-inspired Systems	Cambridge University Press	2010
2.	R.S. Khandpur	Handbook of Biomedical Instruments	3rd Edition, McGraw Hill	2014
3.	Krzysztof Iniewski	CMOS Bio micro systems where Electronics Meet Biology	Wiley	2011
4.	N.A. Sherwani	Algorithms for VLSI Physical Design Automation	Kluwer Academic Publishers	2002
5.	Mohammed Ismail, Terri Fief	Analog VLSI signal and Information Processing	McGraw- Hill	1994

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23VLB09	TESTING OF VLSI CIRCUITS	L	T	P	C
		3	0	0	3

Course Objective:

- To study basics of testing and fault modeling
- To gain knowledge on digital testing as applied to VLSI design.
- To acquire knowledge on testing of algorithms for digital circuits
- To learn the concept of memory, delay fault and IDDQ testing
- To learn various testing methods for digital circuits.
- To understand the BIST architectures

Course Outcomes:

23VLB09.CO1	To ensure that, before fabrication, the circuit behavior satisfies the intent of the designer.
23VLB09.CO2	To detect faulty devices, after fabrication
23VLB09.CO3	To know about testing algorithm for digital circuits
23VLB09.CO4	To Implement the concept of memory, delay fault in circuits
23VLB09.CO5	To ensure that, implement the various testing methods for digital circuits.

Unit-I BASICS OF TESTING AND FAULT MODELING **9**

Introduction- Principle of testing - types of testing - DC and AC parametric tests - fault modeling Stuck-at fault - fault equivalence - fault collapsing - fault dominance - fault simulation.

Unit-II TESTING AND TEST ABILITY OF COMBINATIONAL CIRCUITS **9**

Test generation basics - test generation algorithms - path sensitization - Boolean difference – D-algorithm – PODEM - Testable combinational logic circuit design.

Unit-III TESTING AND TESTABILITY OF SEQUENTIAL CIRCUITS **9**

Testing of sequential circuits as iterative combinational circuits - state table verification - test generation based on circuit structure - Design of testable sequential circuits - Ad Hoc design rules - scan path technique (scan design) - partial scan - Boundary scan.

Unit-IV MEMORY, DELAY FAULT AND IDDQ TESTING **9**

Testable memory design - RAM fault models - test algorithms for RAMs – Delay faults - Delay test- IDDQ testing - testing methods - limitations of IDDQ testing.

Unit-V BUILT-IN SELF-TEST **9**

Test pattern generation of Built-in Self-Test (BIST) - Output response analysis - BIST architectures.

Total Periods: 45

Reference Books:

Sl.No.	Author(s)	Title of the Book	Publisher	Year of Publication
1.	P. K. Lala	Digital Circuit Testing and Testability	Academic Press	2002
2.	M.L. Bushnell and V.D. Agrawal	Essentials of Electronic Testing for Digital, Memory and Mixed-Signal VLSI Circuits	Kluwar Academic Publishers	2004
3.	N.K. Jha and S.G. Gupta	Testing of Digital Systems	Cambridge University Press	2003
4.	Zainalabe Navabi	Digital System Test and Testable Design: Using HDL Models and Architectures	Springer	2010
5.	M. Abramovici, M.A.Breuer and A.D. Friedman	Digital Systems and Testable Design	Jaico Publishing House	2002

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23VLB10	MIXED SIGNAL VLSI DESIGN	L	T	P	C
		3	0	0	3

Course Objective:

- To understand the types of filters.
- To understand the different techniques of ADC
- To understand the different techniques of DAC
- To understand the different techniques of VHDL
- To understand the different techniques of Verilog
- To understand the Multi -disciplinary model

Course Outcomes:

23VLB10.CO1	Analyze the types of filters.
23VLB10.CO2	The ability to use DAC techniques for data conversions.
23VLB10.CO3	The ability to use ADC techniques for data conversions.
23VLB10.CO4	The ability to VHDL program , Mixed Signal VLSI Circuits
23VLB10.CO5	Able to Verilog program, Mixed Signal VLSI Circuits

Unit-I INTRODUCTION TO ACTIVE FILTERS (PLL) & SWITCHED CAPACITOR FILTERS 9

Active RC Filters for monolithic filer design: First & Second order filter realizations – universal active filter (KHN) - self tuned filter - programmable filters- Switched capacitor filters: Switched capacitor resistors - amplifiers – comparators - sample & hold circuits – Integrator- Biquad.

Unit-II CONTINUOUS TIME FILTERS & DIGITAL FILTERS 9

Introduction to Gm - C filters - bipolar trans conductors - CMOS Trans conductors using Triode transistors, active transistors – BiCMOS trans conductors –MOSFET C Filters- Tuning Circuitry -Dynamic range performance - Digital Filters: Sampling–decimation– interpolation – implementation of FIR and IIR filters.

Unit-III DIGITAL TO ANALOG & ANALOG TO DIGITAL CONVERTERS 9

Non-idealities in the DAC - Types of DAC's: Current switched, Resistive, Charge redistribution (capacitive), Hybrid, segmented DAC's - Techniques for improving linearity - Analog to Digital Converters: quantization errors - non-idealities - types of ADC's: Flash, two step, pipelined, successive approximation, folding ADC's. Sigma Delta Converters: Over sampled converters - over sampling without noise & with noise - implementation imperfections - first order modulator - decimation filters - second order modulator - sigma delta DAC & ADC's

Unit-IV ANALOG AND MIXED SIGNAL EXTENSIONS TO VHDL 9

Introduction - Language design Course Objectives - Theory of differential algebraic equations – the 1076 .1 Language - Tolerance groups - Conservative systems - Time and the simulation cycle - A/D and D/A Interaction - Quiescent Point - Frequency domain modeling and examples.

Unit-V ANALOG EXTENSIONS TO VERILOG 9

Introduction –data types –Expressions-Signals-Analog Behavior-Hierarchical structures-Mixed Signal Interaction. Introduction - Equation construction - solution - waveform Filter functions - simulator - Control Analysis - Multi - disciplinary model.

Total Periods: 45

Reference Books:

Sl.No.	Author(s)	Title of the Book	Publisher	Year of Publication
1.	David A. Johns, Ken Martin	Analog Integrated Circuit Design	John Wiley & Sons	2002
2.	Rudy van de Plassche	Integrated Analog-to-Digital and Digital-to-Analog Converters	Kluwer	1999
3.	Antoniou	Digital Filters Analysis and Design	Tata McGraw Hill	1998
4.	Phillip Allen and Douglas Holmberg	CMOS Analog Circuit Design	Oxford University. Press	2000

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23VLB11	ELECTROMAGNETIC INTERFERENCE AND COMPATIBILITY	L	T	P	C
		3	0	0	3

Course Objective:

- To understand the concepts related to Electromagnetic interference in PCBs learn RF design and circuit board components
- To provide solutions for minimizing EMI in PCBs
- To learn EMI standards in the design of PCBs
- To learn various EMI coupling principles, EMI standards and measurements
- To provide knowledge on EMI control techniques and design procedures to make EMI Compatible PCBs
- Understand the Transient Suppressors

Course Outcomes:

23VLB11.CO1	Analyze Electromagnetic interference effects in PCBs
23VLB11.CO2	Propose solutions for minimizing EMI in PCBs
23VLB11.CO3	Analyze Electromagnetic environment, EMI coupling
23VLB11.CO4	Able to understand the EMI standards and measurement
23VLB11.CO5	Able to design a EMI Control techniques

Unit-I EMI ENVIRONMENT **9**

EMI/EMC concepts and definitions, Sources of EMI, conducted and radiated EMI, Transient EMI, Time domain Vs Frequency domain EMI, Units of measurement parameters, Emission and immunity concepts, ESD.

Unit-II EMI COUPLING PRINCIPLES **9**

Conducted, Radiated and Transient Coupling, Common Impedance Ground Coupling, Radiated Common Mode and Ground Loop Coupling, Radiated Differential Mode Coupling, Near Field Cable to Cable Coupling, Power Mains and Power Supply coupling.

Unit-III EMI/EMC STANDARDS AND MEASUREMENTS **9**

Civilian standards - FCC,CISPR,IEC, EN, Military standards - MIL STD 461D/462, EMI Test Instruments Systems, EMI Shielded Chamber, Open Area Test Site, TEM Cell, Sensors/Injectors/Couplers, Test beds for ESD and EFT, Military Test Method and Procedures.

Unit-IV EMI CONTROL TECHNIQUES **9**

Shielding, Filtering, Grounding, Bonding, Isolation Transformer, Transient Suppressors, Cable Routing, Signal Control, Component Selection and Mounting.

Unit-V EMC DESIGN OF PCBs **9**

PCB Traces Cross Talk, Impedance Control, Power Distribution Decoupling, Zoning, Motherboard Designs and Propagation Delay Performance Models.

Total Periods: 45

Reference Books:

Sl.No.	Author(s)	Title of the Book	Publisher	Year of Publication
1.	Clayton Paul	Introduction to Electromagnetic Compatibility	Wiley Inter science	2006
2.	Henry W.Ott	Noise Reduction Techniques in Electronic Systems	John Wiley and Sons, New York	1988
3.	V.P.Kodali	Engineering EMC Principles, Measurements and Technologies	IEEE Press, New York	2001
4.	Dr Kenneth L Kaiser	The Electromagnetic Compatibility Handbook	CRC Press	2005
5.	Henry W. Ott,	Electromagnetic Compatibility Engineering	John Wiley & Sons	2009

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23VLB12	ADVANCED MOSFET MODELING ALGORITHMS	L	T	P	C
		3	0	0	3

Course Objective:

- To understand basic device physics
- To understand MOSFET devices
- To understand nano scaled MOSFETS
- To understand noise modeling and process variation
- To understand compact models for circuit simulators
- To understand the BSIM model

Course Outcomes:

23VLB12.CO1	Able to understand basic device physics
23VLB12.CO2	Able to understand MOSFET devices
23VLB12.CO3	Able to understand nano scaled MOSFETS
23VLB12.CO4	Able to understand noise modeling and process variation
23VLB12.CO5	Able to understand compact models for circuit simulators

Unit-I BASIC DEVICE PHYSICS **9**

Intrinsic and extrinsic semiconductors, direct and indirect semiconductors- Electrons and holes in silicon energy bands: electron and hole densities in equilibrium- Fermi Dirac statistics, carrier concentration, ionization of impurities. Carrier transport in silicon: drift current, diffusion current. pn junctions built in potential, electric field, current voltage characteristics.

Unit-II MOSFET DEVICES **9**

MOS capacitors surface potential- structure characteristics, electrostatic potential and charge distribution- threshold voltage- polysilicon work function- interface states and oxide traps. Long channel MOSFETs: threshold voltage, substrate bias and temperature dependence of threshold voltage, drain current model, sub threshold characteristics, channel mobility, capacitances.

Unit-III NANO SCALED MOSFETs **9**

Scaling of MOSFETs: Short channel MOSFETs – short channel effects, velocity saturation, channel length modulation, DIBL, GIDL. Variability in MOSFETs. Reliability of MOSFETs high field effects, hot carrier degradation, negative bias temperature instability, MOSFET breakdown, high k dielectrics. Non classical MOSFETs : SOI MOSFETs Current voltage equations, fully depleted SOI MOSFETs, partially depleted SOI MOSFETs, Hetero structure MOSFETs, strained channel MOSFETs, Power MOSFETs, SiC MOSFETs- Silicon Nano wires-Carbon Nano tubes.

Unit-IV NOISE MODELING AND PROCESS VARIATION **9**

Noise sources in MOSFET: Flicker noise modeling, Thermal noise modeling- model for accurate distortion analysis- nonlinearities in CMOS devices and modeling- calculation of distortion in analog CMOS circuits. Influence of process variation- modeling of device mismatch for Analog/RF Applications- Benchmark circuits for quality assurance Automation of the tests

Unit-V COMPACT MODELS FOR CIRCUIT SIMULATORS **9**

Introduction to compact models, SPICE Level 1, 2 and 3 MOS models, BSIM model, EKV model, High frequency models- Parameter extraction of MOSFETs.

Total Periods: 45

Reference Books:

Sl.No.	Author(s)	Title of the Book	Publisher	Year of Publication
1.	Taur and T. H. Ning	Fundamentals of Modern VLSI Devices	Cambridge University Press, Cambridge, United Kingdom	1998
2.	Trond Ytterdal, Yuhua Cheng and Tor A. Fjeldly Wayne Wolf	Device Modeling for Analog and RF CMOS Circuit Design	John Wiley & Sons Ltd	2003
3.	N. DasGupta and A. DasGupta	Semiconductor Devices – Modeling and Technology	Prentice Hall of India Pvt. Ltd, New Delhi, India	2004
4.	A. B. Bhattacharyya	Compact MOSFET Models for VLSI Design	John Wiley & Sons Inc.	2009
5.	Weidong Liuand Chemming Hu	BSIM 4 and MOSFET Modeling for IC simulation	World scientific and Publishing Co. Pte. Ltd	2011

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23VLB13	DIGITAL CMOS VLSI DESIGN LABORATORY	L	T	P	C
		0	0	2	1

Sl.No.	List of Experiments
1.	Design and simulate frequency response and noise analysis of any followers.
2.	Design and simulate operational amplifier performance parameters One stage OpAmps, Two stage OpAmps.
3.	Design and simulate cascade current mirrors and active current mirrors.
4.	Design of various routing–local routing, Area routing, Channel routing and global routing.
5.	Design and simulation of Gate-level modeling.
6.	Design and simulation of Switch-level modeling.
7.	Modeling and synthesis of simple scheduling algorithm.
8.	Design and implement reducing power consumption in memories.
9.	Design and simulation of Power Estimation.

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23VLB14	VLSI DESIGN TECHNIQUES LABORATORY	L	T	P	C
		0	0	2	1

Sl.No.	List of Experiments
10.	Design and simulation of combinational circuits using HDL.
11.	Design and simulation of Sequential circuits using HDL.
12.	Writing Test benches using VHDL/Verilog.
13.	Design and simulation of 8-Bit shift register using HDL.
14.	Design and simulation of 4-bit carry save adder, Ripple carry adder using HDL.
15.	Design and simulation of 8-bit adder/subtractor using HDL.
16.	Design and simulation of Multiplier using HDL.
17.	Design and simulation of FSM using HDL.
18.	Design and Implementation of Traffic Light Controller using VHDL.

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23VLC01	INTELLIGENT OPTIMIZATION TECHNIQUES	L	T	P	C
		3	0	0	3

Course Objective:

- To impart knowledge on.
- To impart in-depth knowledge on different advanced optimization techniques to solve engineering problems.
- To impart the concept of multi-objective optimization and its applications to real world problems.

Course Outcomes:

23VLC01.CO1	Familiarize with the basic concept of optimization techniques.
23VLC01.CO2	Apply Genetic Algorithm for solving engineering problems.
23VLC01.CO3	Apply Swarm Optimization techniques for solving engineering problems.
23VLC01.CO4	Explain the concept of different advanced optimization techniques and their applications.
23VLC01.CO5	Explain the concept of Multi-objective optimization and apply it for solving real world problems.

Unit-I FUNDAMENTALS OF OPTIMIZATION 9

Definition - Classification of optimization problems - Unconstrained and Constrained optimization - Optimality conditions - Classical Optimization techniques - Linear and non - linear programming - Quadratic programming - Mixed integer programming - Intelligent Search methods - Evolutionary algorithms - Tabu search - Particle swarm optimization – Advantages of intelligent techniques over classical optimization techniques.

Unit-II EVOLUTIONARY COMPUTATION TECHNIQUES 9

Evolution in nature - Fundamentals of Evolutionary algorithms - Principle of Genetic Algorithm - Evolutionary Strategy and Evolutionary Programming - Genetic Operators - Selection, Crossover and Mutation - Issues in GA implementation - Differential Evolution technique.

Unit-III PARTICLES WARM OPTIMIZATION 9

Fundamental principle -VelocityUpdation -Parameter selection- hybrid approaches -hybrid ofGAand PSO - hybrid of EP and PSO - Binary, discrete and combinatorial PSO - Implementation issues - Convergence issues – Fly Bee Algorithm.

Unit-IV ADDITIONAL OPTIMIZATION METHODS 9

Simulated annealing algorithm - Tabu search algorithm - Ant colony optimization - Bacteria Foraging optimization - Artificial immune system.

Unit-V MULTI OBJECTIVE OPTIMIZATION 9

Concept of pareto optimality - Conventional approaches for MOO - Weighted Sum and Constrained methods - Multi objective GA - Fitness assignment - Multi-objective PSO -Dynamic neighbourhood PSO - Vector evaluated PSO – Necessity for multi-criteria decision making.

Total Periods: 45

Reference Books:

Sl.No.	Author(s)	Title of the Book	Publisher	Year of Publication
1.	Kalyanmoy Deb	Optimization for Engineering Design- Algorithms and Examples	Prentice Hall of India	1995
2.	David Goldberg	Genetic Algorithms in Search, Optimization, and Machine Learning	Addison-Wesley, Reading	1989

3.	Kwang Y. Lee	Modern heuristic optimization techniques	John Wiley and Sons	2008
4.	Kalyanmoy Deb	Multi objective optimization using Evolutionary Algorithms	John Wiley and Sons	2008
5.	Carlos A. Coello Coello, Gary B. Lamont, David A. Van Veldhuizen	Evolutionary Algorithms For solving Multi Objective Problems	2ndEdition, Springer	2007

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23VLC02	SIGNAL INTEGRITY FOR HIGH SPEED DEVICES	L	T	P	C
		3	0	0	3

Course Objective:

- To learn the fundamental and importance of signal integrity.
- To analyze and minimize cross talk in unbounded conductive media.
- To study about differential signaling.
- To study about the different types of Di-Electric materials.
- To learn about differential cross talk and CMOS based transmission line model.
- To understand physical transmission line model.

Course Outcomes:

23VLC02.CO1	To learn the fundamental and importance of signal integrity.
23VLC02.CO2	To analyze and minimize cross talk in unbounded conductive media.
23VLC02.CO3	To study about the different types of Di-Electric materials.
23VLC02.CO4	To study about differential signaling.
23VLC02.CO5	To learn about differential cross talk and CMOS based transmission line model.
23VLC02.CO6	Able to analyze the loosy dielectric and realistic conductors.

Unit-I FUNDAMENTALS 9

The importance of signal integrity-new realm of bus design-Electromagnetic fundamentals for signal integrity-maxwell equations common vector operators-wave propagations-Electro statics magneto statics-Power flow and the poynting vector- Reflections of electromagnetic waves.

Unit-II CROSSTALK 9

Introduction -mutual inductance and capacitance-coupled wave equation-coupled line analysis modal analysis-cross talk minimization signal propagation in unbounded conductive media-classic conductor model for transmission model.

Unit-III DI-ELECTRICMATERIALS 9

Polarization of Dielectric-Classification of Di electric material-frequency dependent di electric material-Classification of Di electric material fiber-Weave effect-Environmental variation in di electric behaviour Transmission line parameters for loosy dielectric and realistic conductors.

Unit-IV DIFFERENTIAL SIGNALING 9

DC operating point and Load line-Q point-Bias Stability, Transistor biasing methods: Fixed bias-Collector to base bias-Self biasing, Bias compensation methods, Thermistor and sensistor compensation techniques, thermal runaway, thermal stability, FET biasing methods: Self bias-Source bias-Voltage divider bias-Biasing enhancement and depletion MOSFET.

Unit-V PHYSICAL TRANSMISSION LINE MODEL 9

Introduction- non ideal return paths-Vias-IO design consideration-Push-pull transmitter-CMOS receivers-ESSD protection circuits-On chip Termination.

Total Periods: 45

Reference Books:

Sl.No.	Author(s)	Title of the Book	Publisher	Year of Publication
1.	Stephen H. Hall, Howard L. Heck	Advanced Signal Integrity for High- Speed Digital Designs	Wiley	2009
2.	James Edgar Buchanan	Signal and power integrity in digital systems: TTL, CMOS, and BiCMOS	Hardcover	1996
3.	Hanqiao Zhang Steven, Krooswyk, Jeffrey Ou	High Speed Digital Design: Design of High Speed Interconnects and Signaling	MK	2015
4.	Stephen H. Hall, Garrett W.HallJames A. McCall	High-Speed Digital System Design: A Handbook of Interconnect Theory and Design Practices	Kindly Edition	2000
5.	Eric Bogatin	Signal and Power Integrity-Simplified (Prentice Hall Modern Semiconductor Design Series)	Kindly Edition	2009

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23VLC03	ADVANCED DIGITAL SYSTEM DESIGN	L	T	P	C
		3	0	0	3

Course Objective:

- To understand the concepts of advanced Boolean algebra.
- To understand the concepts of threshold logic.
- To understand the concepts of symmetric functions.
- To understand the concepts of sequential logic circuits.
- To study the concepts of Fault Diagnosis and Testability Algorithms.
- To understand the concept of test generation.

Course Outcomes:

23VLC03.CO1	To apply knowledge of Boolean algebra to the analysis and design of digital logic circuits.
23VLC03.CO2	To acquire the knowledge of threshold logic.
23VLC03.CO3	To acquire the knowledge of symmetric functions.
23VLC03.CO4	To view advanced digital design from a hierarchical viewpoint.
23VLC03.CO5	To acquire the knowledge of testability concepts.
23VLC03.CO6	To analyze the Built-in Self Test.

Unit-I ADVANCED TOPICS IN BOOLEAN ALGEBRA 9

Shannon's expansion theorem, Consensus theorem, Octal designation, Run measure, INHIBIT/INCLUSION/AOI/ Driver/ Buffer gates, Gate expander, Reed Muller expansion, Synthesis of multiple output combinational logic circuits by product map method, Design of static hazard free and dynamic hazard free logic circuits.

Unit-II THRESHOLD LOGIC 9

Linear seperability, Unateness, Physical implementation, Dual comparability, Reduced functions, Various theorems in threshold logic, Synthesis of single gate and multigate threshold Network.

Unit-III SYMMETRIC FUNCTIONS 9

Elementary symmetric functions, Partially symmetric and total ly symmetric functions, McCluskey decomposition method, Unity ratio symmetric ratio functions, Synthesis of symmetric function by contact networks.

Unit-IV SEQUENTIAL LOGIC CIRCUITS 9

Mealy machine, Moore machine, Trivial / Reversible / Isomorphic sequential machines, State diagrams, State table minimization, Incompletely specified sequential machines, State assignments, Design of synchronous and asynchronous sequential logic circuits working in the fundamental mode and pulse mode, Essential hazards Unger's theorem.

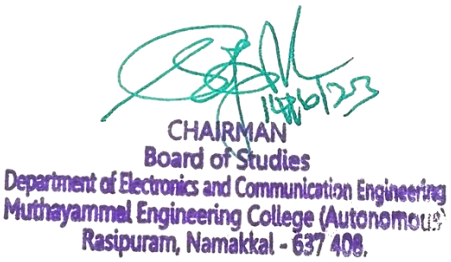
Unit-V FAULT DIAGNOSIS AND TESTABILITY ALGORITHMS 9

Fault Table Method –Path Sensitization Method –Boolean Difference Method –Kohavi Algorithm –Tolerance Techniques – The Compact Algorithm –Fault in PLA –Test Generation –Masking Cycle –Built-in Self Test.

Total Periods: 45

Reference Books:

Sl.No.	Author(s)	Title of the Book	Publisher	Year of Publication
1.	Charles H. Roth Jr	Fundamentals of Logic Design	Thomson Learning	2004
2	Nripendra N Biswas	Logic Design Theory	Prentice Hall of India	2001
3	Parag K. Lala	Digital system Design using PLD	BS Publications	2003
4	Lucien N galamou	Advanced Digital Systems Design with Rapid Prototyping on FPGAs Using VHDL	Springer	2012
5	Kuruvilla Varghese	Digital System Design with PLDs and FPGAs	Prentice Hall	2007



23VLC04	SUBMICRON VLSI DESIGN	L	T	P	C
		3	0	0	3

Course Objective:

- To introduce the concepts of Silicon realization of ASIC.
- To introduce the concepts of CMOS devices at deep submicron level.
- To study and apply the deep submicron concepts to CMOS low power devices.
- To study and discuss about RF CMOS transistor sizing.
- To study and discuss about RF CMOS transistor sizing limitations.
- To understand the scaling perspectives.

Course Outcomes:

23VLC04.CO1	Able to known the concepts of Silicon realization of ASIC.
23VLC04.CO2	Known the concepts of CMOS devices at deep submicron level.
23VLC04.CO3	Known the concepts to CMOS low power devices.
23VLC04.CO4	Importance of RF CMOS transistor sizing.
23VLC04.CO5	RF CMOS transistor sizing limitations.
23VLC04.CO6	Able to analyze the package-Signal propagation.

Unit-I SILICON REALIZATION OF ASIC **9**

Introduction-Handcrafted layout implementation-bit-slice layout implementation-Cell based layout implementation-gate array layout implementation - Hierarchial design approach-The choice of layout implementation form

Unit-II LOW POWER DESIGN **9**

Sources of CMOS power consumption-technology options for low power-reduction of P-leak by technological measures Reduction of P-dyn by technology measures-reduction of P-dyn by reduced voltage process-design option for low power- computing power Vs chip power-scaling perspectives.

Unit-III DESIGN FOR RELIABILITY **9**

Introduction-latch up in CMOS circuits-Electrostatics discharge-and its protection-Electro migration-Hot carrier degradation design for signal integrity -clock distribution and critical timing issues-clock generation and synchronization in different domain on a chip-the influence of interconnection-design organization.

Unit-IV DEEP SUBMICRON **9**

RF CMOS Transistor downsizing limitations- RF basic blocks layout implementation Submicron technology and layout dependent effects - input output interfacing, the bonding pad, the pad ring, electrostatic discharge prevention.

Unit-V CMOS DEVICES **9**

Clamp CMOS devices, zener diode-input structure-output structure-pull up-pull down-i/o pad, power clamp-core/pad limitation I/O Pad description using Ibis-Connecting to the package-Signal propagation between integrated circuits**.**

Total Periods: 45

Reference Books:

Sl.No.	Author(s)	Title of the Book	Publisher	Year of Publication
1.	Harry J. M. Veendrick	Deep-Submicron Cmos Ics: From Basics to Asics	Thomson Learning	2004
2.	W. Nebel, Jean P. Mermet	Low Power Design in Deep Submicron Electronics	Prentice Hall of India	2001
3.	P. R. Van Der Meer, Arie van Staveren, Arthur H. M. van Roermund	Low-Power Deep Sub-Micron CMOS Logic: Sub-threshold Current Reduction	Prentice Hal lof India	2003
4.	Philip E. Madrid	Device Design And Process Window Analysis Of A Deep Submicron CMOS VLSI Technology	Springer	2012
5.	Kuruvilla Varghese	Digital System Design with PLDs and FPGAs	Prentice Hall	2007

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23VLC05	VLSI TECHNOLOGY	L	T	P	C
		3	0	0	3

Course Objective:

- To understand the Fabrication of ICs and purification of Silicon in different technologies.
- To impart in-depth knowledge about Etching and deposition of different layers.
- To understand the different packaging techniques of VLSI devices.
- To understand the fabrication technologies.
- To understand the integration techniques.
- To understand the MOS Memory IC technology.

Course Outcomes:

23VLC05.CO1	The ability to use metallization techniques to create three-dimensional device structures devices.
23VLC05.CO2	The ability to know methodology to fabricate an IC's.
23VLC05.CO3	The ability to observe the implementation techniques in chip designing.
23VLC05.CO4	The ability to learn the application areas of VLSI technologies.
23VLC05.CO5	Able to understand the integration techniques.
23VLC05.CO6	Able to analyze the MOS Memory IC technology.

Unit-I CRYSTAL GROWTH, WAFER PREPARATION, EPITAXY AND OXIDATION 9

Electronic Grade Silicon, Czochralski crystal growing, Silicon Shaping, processing consideration,Vapor phase Epitaxy, Molecular Beam Epitaxy, Epitaxial Evaluation, Growth Mechanism andkinetics, Thin Oxides, Oxidation Techniques and Systems, Oxide properties, Redistribution ofDopants at interface, Oxidation of Poly Silicon, Oxidation induced Defects.

Unit-II LITHOGRAPHY AND REACTIVE PLASMA ETCHING 9

Optical Lithography, Electron Lithography, X-Ray Lithography, Ion Lithography, Nano imprint Lithography, Plasma properties, Feature Size control and Anisotropic Etch mechanism, reactive Plasma Etching techniques and Equipments.

Unit-III DEPOSITION, DIFFUSION AND ION IMPLANTATION 9

Deposition process, Polysilicon, plasma assisted Deposition, Models of Diffusion in Solids, Fick's one dimensional Diffusion Equation - Measurement techniques - Range theory- Implant equipment –Annealing- Shallow junction, High - energy implantation.

Unit-IV METALLIZATION AND VLSI PROCESS INTEGRATION 9

Physical Vapour Deposition(PVD) –Patterning-NMOS IC Technology– CMOS IC Technology–BICMOS IC Technology- MOS Memory IC technology - Bipolar IC Technology –Silicon on Insulator Technology–Noise in VLSI Technologies

Unit-V ANALYTICAL, ASSEMBLY TECHNIQUES AND PACKAGING OF VLSI DEVICES 9

Analytical Beams – Beams Specimen interactions - Chemical methods – Package types – packaging design consideration – VLSI assembly technology – Package fabrication technology. Scanning Probe Techniques-Analysis by diffraction and fluorescence methods

Total Periods: 45

Reference Books:

Sl.No.	Author(s)	Title of the Book	Publisher	Year of Publication
1.	S.M .S ze	VLSI Technology	McGraw Hill	2003
2.	Amar Mukherjee	Introduction to NMOS and CMOS VLSI System Design	PHI	2000
3.	James D Plummer, Michael D. Dealand Peter B. Griffin	Silicon VLSI Technology: Fundamentals Practice and Modeling	PHI	2000
4.	Wai Kai Chen	VLSI Technology	CRC press	2003
5.	Rainer Waser	Nano Electronics and Information Technolgy	Wiley-IEEE Press	2004

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23VLC06	DSP INTEGRATED CIRCUITS	L	T	P	C
		3	0	0	3

Course Objective:

- To study the procedural flow of system design in DSP and Integrated circuit.
- To design FIR and IIR filters for the given specifications.
- To study the architectures for DSP system.
- To learn the design layout for VLSI circuits.
- To understand the concept of DSP Processor Architecture and code optimization.
- To learn the applications of DSP Integrated circuits.

Course Outcomes:

23VLC06.CO1	To design filter and analysis the concept of finite word length effects.
23VLC06.CO2	To synthesis DSP Architecture and design integrated circuits.
23VLC06.CO3	To learn DSP Processor Architecture.
23VLC06.CO4	The ability to learn the optimization techniques.
23VLC06.CO5	TounderstandtheconceptofDSPProcessorArchitectureandcodeoptimization.
23VLC06.CO6	To learn the applications of DSP Integrated circuits.

Unit-I DSP SYSTEMS AND MOS TECHNOLOGIES 9

Standard digital signal processors–Application specific IC's for DSP –DSP systems–DSP system design–Integrated circuit design – MOS transistors- MOS logic - VLSI process technologies – Trends in CMOS technologies.

Unit-II DIGITAL FILTERS AND FINITE WORD LENGTH EFFECTS 9

FIR filters: FIR filter structures, FIR chips -IIR filters structures-Real time filtering – Circular buffering- Adaptive filtering: LMS and RLS Algorithm –Multi-rate filters: Interpolation with an integer factor L, Sampling rate change with a ratio L/M Finite Word Length Effects: Parasitic oscillations - Scaling of signal levels - Round-off noise –Measuring round-off noise.

Unit-III DSP ARCHITECTURES AND ITS SYNTHESIS 9

DSP system architectures - Standard DSP architecture - Ideal DSP architectures - Multiprocessors and multicomputer – Systolic and Wave front arrays -Shared memory architectures –Mapping of DSP algorithms on to hardware -Implementation based on complex PEs - Shared memory architecture with Bi-serial PEs.

Unit-IV ARITHMETIC UNITS AND INTEGRATED CIRCUIT DESIGN 9

Conventional number system-Redundant Number system-Residue Number System-Bit-parallel and Bit-Serial arithmetic-Basic shift accumulator –Reducing the memory size –Complex multipliers -Improved shift-accumulator-Layout of VLSI circuits - FFT processor - DCT processor and Interpolator as case studies - Cordic algorithm.

Unit-V TMS320C6X, DSP56XXX PROCESSORS ARCHITECTURE AND CODE OPTIMIZATION 9

CPU Operation – Pipelined CPU- Velocity TI – C64XDSP- Software tools: EVM – DSK Target C6x board – Assembly file– Memory management- Compiler utility- Code initialization – Code composer studio – Interrupt data processing, Code Optimization: Word- wide optimization – Mixing C and assembly- Software pipelining – C64X improvements – Overview on Free scale DSP56XXX Core Architecture. Design of modulo multipliers using RNS-complex multipliers-accumulator.

Total Periods: 45

Reference Books:

Sl.No.	Author(s)	Title of the Book	Publisher	Year of Publication
1.	Lars Wanhammer	DSP Integrated Circuits	Academic press, New York	1999
2	Nasser Kehtarnavaz	DSP System Design Using the TMS320C6000	Wiley Prentice Hall	2001
3	Richard G. Lyons	Understanding Digital Signal Processing 2004.	Prentice Hall	2010
4	John G. Proakis, Dimitris K. Manolakis	Digital Signal Processing: Principles, Algorithms, and Applications.	Kluwer Academic Publisher	2006
5	Mohammed El-Sharkawy	DigitalSignalProcessingApplications withMotorola's DSP56002 Processor.	Prentice Hall	2006

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23VLC07	ARM PROCESSOR AND ITS APPLICATIONS	L	T	P	C
		3	0	0	3

Course Objective:

- To study the concepts of Architecture and Assembly language programming of ARM Processor.
- To study the concepts of Architectural Support for High level language.
- To understand the memory hierarchy of processors.
- To study the concepts of Architectural support for system Development.
- To understand the processors Operating system.
- To learn applications of ARM processor.

Course Outcomes:

23VLC07.CO1	Analysis the different types of Architectures.
23VLC07.CO2	To learn about instruction Set for different architectures.
23VLC07.CO3	To understand and analysis about the Assembly language Program for various industry based.
23VLC07.CO4	The ability to observe the real time applications of operating system Development.
23VLC07.CO5	The ability to observe the real time applications of operating system.
23VLC07.CO6	Able to learn applications of ARM processor.

Unit-I ARM ARCHITECTURE 9

Abstraction in hardware design – MUO -Acorn RISC Machine – Architecture Inheritance – ARM programming model – ARM Development Tools – 3 and 5 Stage Pipeline ARM Organization – ARM Instruction Execution and Implementation – ARM Co-Processor Interface.

Unit-II ARM ASSEMBLY LANGUAGE PROGRAMMING 9

ARM Instruction Types – data Transfer, Data Processing and Control Flow Instructions – ARM Instruction set – Co- Processor Instruction.

Unit-III ARCHITECTURAL SUPPORT FOR HIGH LEVEL LANGUAGE AND MEMORY HIERARCHY 9

Data Types – Abstraction in software design – expressions – Loops – Functions and Procedures –Conditional Statements – use of memory- Memory size and speed – On Chip Memory – Caches Design – an example – Memory management.

Unit-IV ARCHITECTURAL SUPPORT FOR SYSTEM DEVELOPMENT 9

Physical Vapour Deposition (PVD) –Patterning- NMOS IC Advantaged Microcontroller Bus Architecture – ARM memory Interface – ARM Reference Peripheral Specification– Hardware System Prototyping Tools – Emulator – Debug Architecture

Unit-V ARCHITECTURAL SUPPORT FOR OPERATING SYSTEM 9

An introduction to Operating systems – ARM system Control Coprocessor – CP15 Protection unit Registers – ARM Protection unit – CP15 MMU Registers – ARM MMU Architecture –Synchronization context Switching input and output. Design of various real time applications using ARM processor

Total Periods: 45

Reference Books:

Sl.No.	Author(s)	Title of the Book	Publisher	Year of Publication
1.	Steve Furber	ARM System on Chip Architecture	Wesley Professional	2000
2	Ricardo Reis	Design of System on a Chip: Devices and Components	Springer	2004
3	Daniel Nenni,Don Dingee	Mobile Unleashed: The Origin and Evolution of ARM Processors in our Devices	Springer	2015
4	Joseph Yiu	The Definitive Guide to the Arm Cortex-M0	Newnes	2011
5	Jason Andrews	Verification of Hardware and Software for ARM System on Chip Design(Embedded Technology) BK and CD-ROM	PHI	2004

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23VLC08	HARDWARE DESIGN VERIFICATION TECHNIQUES	L	T	P	C
		3	0	0	3

Course Objective:

- To understand the Concepts of Verification Techniques and Tools.
- To study the concepts of Verification Plan.
- To know the Stimulus and Response.
- To understand the concepts of Architecting Test benches.
- To know the concept of System Verilog.

Course Outcomes:

23VLC08.CO1	To acquire knowledge, how to analyze and design small scale combinational logic circuits using HDLs.
23VLC08.CO2	To learn to analyze the problems in digital design using HDLs.
23VLC08.CO3	To view VLSI design from a hierarchical viewpoint.
23VLC08.CO4	To learn to analyze RTL design.
23VLC08.CO5	Understand the SVA and UVM verification.

Unit-I VERIFICATION TECHNIQUES AND TOOLS 9

Testing vs. Verification–Verification and Design Reuse –Functional Verification, Timing Verification, Formal Verification, and Linting Tools – Simulators – Third Party Models – Waveform Viewers – Code Coverage issue Tracking Metrics.

Unit-II VERIFICATION PLAN 9

Verification plan –LevelsofVerification–VerificationStrategies–SpecificationFeatures–Testcases–TestBenches.

Unit-III STIMULUSANDRESPONSE 9

SimpleStimulus–OutputVerification–SelfCheckingTestBenches–ComplexStimulusandResponse–Predictionof Output.

Unit-IV ARCHITECTINGTESTBENCHES 9

Reusable Verification Components – VHDL and Verilog Implementation – Autonomous Generation and Monitoring – Input and Output Paths – Verifying Configurable Design.

Unit-V SYSTEMVERILOG 9

Data types, RTL design, Interfaces, clocking, Assertion based verification, classes, Testbench automation and constraints. System verilog for design and verification- SVA and UVM for verification.

Total Periods: 45

Reference Books:

Sl.No.	Author(s)	Title of the Book	Publisher	Year of Publication
1.	Janick Bergeron	Writing Test Benches Functional Verification of HDL Models	Springer	2003
2	Andrea Meyer	Principles of Functional Verification	Newnes	2003

3	William K. Lam	Hardware Design Verification: Simulation and Formal Method-Based Approaches	Prentice Hall	2015
4	T. Kropf	Introduction to Formal Hardware Verification	Springer Verlag	2010
5	Chris Spear	System Verilog for Verification: A Guide to Learning the Test bench Language Features	Springer	2008

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23VLC09	DESIGN AND ANALYSIS OF ALGORITHMS	L	T	P	C
		3	0	0	3

Course Objective:

- Learn algorithms for various computing problems.
- Analyze the time and space complexity of algorithms.
- Learn the algorithm analysis techniques.
- Become familiar with the different algorithm design techniques.

Course Outcomes:

23VLC09.CO1	Design algorithms for various computing problems.
23VLC09.CO2	Analyze the time and space complexity of algorithms.
23VLC09.CO3	Critically analyze the different algorithm design techniques for a given problem.
23VLC09.CO4	Modify existing algorithms to improve efficiency.
23VLC09.CO5	Implementation of coping with the limitations of algorithm power.

Unit-I INTRODUCTION 9

Notion of an Algorithm – Fundamentals of Algorithmic Problem Solving – Important Problem Types – Fundamentals of the Analysis of Algorithm Efficiency – Analysis Framework – Asymptotic Notations and its properties – Mathematical analysis for Recursive and Non-recursive algorithms.

Unit-II BRUTE FORCE AND DIVIDE-AND-CONQUER 9

Brute Force – Closest-Pair and Convex-Hull Problems-Exhaustive Search – Traveling Salesman Problem – Knapsack problem – Assignment problem. Divide and conquer methodology – Merge sort – Quick sort – Binary search – Multiplication of Large Integers – Strassen's Matrix Multiplication-Closest-Pair and Convex-Hull Problems.

Unit-III DYNAMIC PROGRAMMING AND GREEDY TECHNIQUE 9

Computing a Binomial Coefficient – Warshall's and Floyd' algorithm – Optimal Binary Search Trees – Knapsack Problem and Memory functions. Greedy Technique– Prim's algorithm- Kruskal's Algorithm- Dijkstra's Algorithm-Huffman Trees

Unit-IV ITERATIVE IMPROVEMENT 9

The Simplex Method-The Maximum-Flow Problem – Maximm Matching in Bipartite Graphs- The Stable marriage Problem.

Unit-V COPING WITH THE LIMITATIONS OF ALGORITHM POWER 9

Limitations of Algorithm Power-Lower-Bound Arguments-Decision Trees-P, NP and NP-Complete Problems– Coping with the Limitations – Backtracking – n-Queens problem – Hamiltonian Circuit Problem – Subset Sum Problem-Branch and Bound – Assignment problem- Knapsack Problem – Traveling Salesman Problem- Approximation Algorithms for NP- Hard Problems- Traveling Salesman Problem- Knapsack problem.

Total Periods: 45

Reference Books:

Sl.No.	Author(s)	Title of the Book	Publisher	Year of Publication
1.	Anany Levitin	Introduction to the Design and Analysis of Algorithms	Third Edition, Pearson Education	2012
2.	Thomas H.Cormen, Charles E. Leiserson, Ronald L. Rivest And Clifford Stein	Introduction to Algorithms	Third Edition, PHI Learning Private Limited	2012

3.	Alfred V. Aho, John E. Hopcroft and Jeffrey D. Ullman	Data Structures and Algorithms	Pearson Education	2006
4.	Donald E. Knuth	The Art of Computer Programming	Volumes 1& 3 Pearson Education	2009
5.	Steven S. Skiena	The Algorithm Design Manual	Springer, Second Edition,	2009

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23VLC10	MEMS AND NEMS	L	T	P	C
		3	0	0	3

Course Objective:

- To introducing the concepts of micro electro mechanical devices.
- To know the fabrication process of Microsystems.
- To know the design concepts of micro sensors and micro actuators.
- To introducing concepts of quantum mechanics.
- To introducing concepts of nano systems.
- To learn applications of MEMs.

Course Outcomes:

23VLC10.CO1	Able to introduce the concepts of micro electro mechanical devices.
23VLC10.CO2	Able to know the fabrication process of Microsystems.
23VLC10.CO3	Able to know the design concepts of micro sensors and micro actuators.
23VLC10.CO4	Able to introducing concepts of quantum mechanics.
23VLC10.CO5	Able to introducing concepts of nano systems.
23VLC10.CO6	Able to learn applications of MEMS.

Unit-I OVERVIEWANDINTRODUCTION 9

New trends in Engineering and Science: Micro and Nano scale systems Introduction to Design of MEMS and NEMS, Overview of Nano and Micro electromechanical Systems, Applications of Micro and Nano electromechanical systems, Micro electromechanical systems, devices and structures Definitions, Materials for MEMS: Silicon, silicon compounds, polymers, metals.

Unit-II MEMSFABRICATIONTECHNOLOGIES 9

Micro system fabrication processes: Photolithography, Ion Implantation, Diffusion, Oxidation. Thin film depositions: LPCVD, Sputtering, Evaporation, Electroplating; Etching techniques: Dry and wet etching, electrochemical etching; Micromachining: Bulk Micromachining, Surface Micro machining, High Aspect-Ratio (LIGA and LIGA-like) Technology; Packaging: Microsystems packaging, Essential packaging technologies, Selection of packaging materials.

Unit-III MICROSENSORS 9

MEMS Sensors: Design of Acoustic wave sensors, resonant sensor, Vibratory gyroscope, Capacitive and Piezo Resistive Pressure sensors- engineering mechanics behind these Micro sensors. Case study: Piezo-resistive pressure sensor.

Unit-IV MICROACTUATORS 9

Design of Actuators: Actuation using thermal forces, Actuation using shape memory Alloys, Actuation using piezoelectric crystals, Actuation using Electrostatic forces (Parallel plate, Torsion bar, Comb drive actuators), Micromechanical Motors and pumps. Case study: Comb drive actuators.

Unit-V NANOSYSTEMSANDQUANTUMMECHANICS 9

Atomic Structures and Quantum Mechanics, Molecular and Nanostructure Dynamics: Shrodinger Equation and Wavefunction Theory, Density Functional Theory, Nanostructures and Molecular Dynamics, Electromagnetic Fields and their quantization, Molecular Wires and Molecular Circuits.

Total Periods: 45

Reference Books:

Sl.No.	Author(s)	Title of the Book	Publisher	Year of Publication
1.	Marc Madou	Fundamentals of Micro fabrication	CRC press	1997
2	Stephen D. Senturia	Micro system Design	Kluwer Academic Publishers	2001
3	Tai Ran Hsu	MEMS and Microsystems Design and Manufacture	Tata Mcraw Hill	2002
4	Chang Liu	Foundations of MEMS	Pearson education India limited	2006
5	Sergey Edward Lyshevski	MEMS and NEMS: Systems, Devices, and Structures	CRC Press	2002

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23VLC11	ASIC DESIGN	L	T	P	C
		3	0	0	3

Course Objective:

- To acquire knowledge about various logics of ASICS and CMOS.
- To acquire knowledge about different types of ASICs design.
- To study about various types of Programmable ASICs architectures.
- To study about various types of Programmable ASICs interconnects.
- To comprehend the low power design techniques and methodologies.
- To understand the floor planning, placement and routing.

Course Outcomes:

23VLC11.CO1	Analysis the different types of ASICs design.
23VLC11.CO2	Analysis the different Logic cell architecture and interconnects.
23VLC11.CO3	Analysis about different programmable ASIC design software.
23VLC11.CO4	Identification of new developments in SOC.
23VLC11.CO5	Identification of developments in low power design.
23VLC11.CO6	To analyze the Flash architecture, Pipelined Architecture.

Unit-I INTRODUCTION TO ASICS, CMOS LOGIC, ASIC LIBRARY DESIGN 9

Types of ASICs - Design flow –CMOS transistors-CMOS Design rules –Combinational logic Cell Sequential logic cell - Transistor as Resistors -Transistor parasitic capacitance –Logical effort -Library cell design –Library architecture-gate array design-standard cell design-data path cell design.

Unit-II PROGRAMMABLE ASICS, PROGRAMMABLE ASIC LOGIC CELLS AND ROGRAMMABLE ASIC I/O CELLS 9

Anti fuse -Static RAM -EPROM and EEPROM technology -PREP benchmarks -Actel ACT -Xilinx LCA –Altera FLEX - Altera MAX-DC & AC inputs and outputs –clock input-power input -Xilinx I/O blocks.

Unit-III PROGRAMMABLE ASIC INTERCONNECT, PROGRAMMABLE ASIC DESIGN SOFTWARE AND LOW LEVEL DESIGN ENTRY 9

Actel ACT -Xilinx LCA -Xilinx EPLD -Altera MAX 5000 and 7000 -Altera MAX 9000 -Altera FLEX –Design systems - Logic Synthesis -Half gate ASIC -Low level design language -PLA tools EDIF-CFI design representation.

Unit-IV ASIC CONSTRUCTION 9

Performance metric, Flash architecture, Pipelined Architecture, Successive approximation architecture, Time interleaved architecture.

Unit-V FLOOR PLANNING, PLACEMENT AND ROUTING 9

Floor planning –placement-physical design flow-information formats-Routing-Global routing, detailed routing, special routing, circuit extraction and DRC.

Total Periods: 45

Reference Books:

Sl.No.	Author(s)	Title of the Book	Publisher	Year of Publication
1.	M. J. S. Smith	Application Specific Integrated Circuits	Pearson Education	2008
2	Farzad Nekoogarand Faranak Nekoogar	From ASICs to SOCs: A Practical Approach	Prentice Hall PTR	2003
3	Wayne Wolf	FPGA-Based System Design	Prentice Hall PTR	2009
4	Wai- Kai Chen	Memory, Microprocessor, and ASIC	Prentice Hall	2006
5	Khosrow Golshan	Physical Design Essentials: An ASIC Design Implementation Perspective	Prentice Hall	2007

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23VLC12	VLSI FOR WIRELESS COMMUNICATION	L	T	P	C
		3	0	0	3

Course Objective:

- To understand the basics of wireless communication.
- To understand the concepts of transceiver architectures.
- To introduce to the students the low power design techniques of VLSI circuits.
- To learn the design and implementation of VLSI circuits for wireless communication systems.
- To learn to design Frequency Synthesizer.
- To learn applications of wireless communication.

Course Outcomes:

23VLC12.CO1	Understanding of application of VLSI circuits in wireless communication.
23VLC12.CO2	Knowledge of various architectures used in implementing wireless systems.
23VLC12.CO3	Discussion about design and simulation of low power techniques using software.
23VLC12.CO4	Learn the VLSI design of wireless circuits.
23VLC12.CO5	Able to design Frequency Synthesizers.
23VLC12.CO6	Able to learn applications of wireless communication.

Unit-I OVERVIEW OF MODULATION SCHEMES 9

Classical Channel - Wireless Channel Description - Path Loss - Channel Model and Envelope Fading - Multipath Fading : Frequency Selective and Fast Fading - Basics of Spread Spectrum and Spread Spectrum Techniques - PN Sequence.

Unit-II TRANSCEIVER ARCHITECTURE 9

Transceiver Design Constraints - Baseband Subsystem Design - RF Subsystem Design - Super Heterodyne Receiver and Direct Conversion Receiver - Receiver Front-End - Filter Design- Non-Idealities and Design Parameters - Derivation of Noise Figure.

Unit-III LOW POWER DESIGN TECHNIQUES 9

Source of Power Dissipation - Estimation of Power Dissipation - Reducing Power Dissipation at Device and Circuit Levels - Low Voltage and Low Power Operation - Reducing Power Dissipation at Architecture and Algorithm Levels.

Unit-IV WIRELESS CIRCUITS 9

VLSI Design of LNA - Wideband and Narrow Band - Impedance Matching - Automatic Gain Control (AGC) Amplifier - Power Amplifier - Active Mixer - Analysis, Conversion Gain, Distortion Analysis - Low Frequency and High Frequency Case, Noise - Passive Mixer - Sampling Mixer and Switching Mixer Analysis of Distortion, Gain and Noise Conversion.

Unit-V FREQUENCY SYNTHESIZERS 9

VLSI Design Of Frequency Synthesizers (FS) - Parameters Of FS - PLL Based Frequency Synthesizer, Phase Detector/Charge Pump- Dividers- VCO- LC Oscillators- Ring Oscillator- Phase Noise- Loop Filter Description, Design Approaches.

Total Periods: 45

Reference Books:

Sl.No.	Author(s)	Title of the Book	Publisher	Year of Publication
1.	BoscoLeung	VLSI for Wireless Communication	Springer	2011
2	Elmad N Farag and Mohamed I Elmasry	Mixed Signal VLSI Wireless Design- Circuits and Systems	Kluwer Academic Publishers	2002
3	Marc Snir	Lower Bounds on VLSI Implementations of Communication Networks	Palala Press	2015
4	Richard Cole	Lower Bounds on Communication Complexity in VLSI	27thForgottenBooks	2015
5	Xiaohua Tian, Thinh M. Le, Yong Lian	EntropyCodersoftheH.264/AVC Standard: Algorithms and VLSI Architectures	17thSpringer	2010

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23VLC13	RESEARCH METHODOLOGY	L	T	P	C
		3	0	0	3

Course Objective:

- To know introduction to research course outcomes.
- To learn experimental design.
- To know data collection methods.
- To learn multivariate statistical techniques.
- To impart knowledge research report.

Course Outcomes:

23VLC13.CO1	Learn to know introduction to research course outcomes.
23VLC13.CO2	Learn to understand experimental design.
23VLC13.CO3	Learn to know data collection methods.
23VLC13.CO4	Learn to know multivariate statistical techniques.
23VLC13.CO5	Learn to know knowledge research report.

Unit-I INTRODUCTION TO RESEARCH 9

The hallmarks of scientific research – Building blocks of science in research – Concept of Applied and Basic research – Quantitative and Qualitativse Research Techniques – Need for theoretical frame work – Hypothesis development – Hypothesis testing with quantitative data. Research design – Purpose of the study: Exploratory, Descriptive, Hypothesis Testing.

Unit-II EXPERIMENTAL DESIGN 9

Laboratory and the Field Experiment – Internal and External Validity – Factors affecting Internal validity. Measurement of variables – Scales and measurements of variables. Developing scales – Rating scale and attitudinal scales – Validity testing of scales – Reliability concept in scales being developed – Stability Measures.

Unit-III DATA COLLECTION METHODS 9

Interviewing, Questionnaires, etc. Secondary sources of data collection. Guidelines for Questionnaire Design – Electronic Questionnaire Design and Surveys. Special Data Sources: Focus Groups, Static and Dynamic panels. Review of Advantages and Disadvantages of various Data-Collection Methods and their utility. Sampling Techniques – Probabilistic and non-probabilistic samples.

Unit-IV MULTIVARIATE STATISTICAL TECHNIQUES 9

Data Analysis – Factor Analysis – Cluster Analysis – Discriminant Analysis – Multiple Regression and Correlation – Canonical Correlation – Application of Statistical (SPSS) Software Package in Research

Unit-V RESEARCH REPORT 9

Purpose of the written report – Concept of audience – Basics of written reports. Integral parts of a report – Title of a report, Table of contents, Abstract, Synopsis, Introduction, Body of a report – Experimental, Results and Discussion – Recommendations and Implementation section – Conclusions and Scope for future work.

Total Periods: 45

Reference Books:

Sl.No.	Author(s)	Title of the Book	Publisher	Year of Publication
1.	Donald R. Cooperand Ramela S. Schindler	Business Research Methods	Tata McGraw-Hill Publishing Company Limited, New Delhi	2000
2	Uma Sekaran	Research Methods for Business,	John Wiley and Sons Inc., New York,	2000
3	C.R .Kothari,	Research Methodology	Wishva Prakashan, New Delhi	2001
4	Donald H. Mc Burney	Research Methods, Thomson Asia Pvt. Ltd..	Singapore	2002
5	G.W.Ticehurstand A.J.Veal	Business Research Methods,	Longman,	1999

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23VLC14	ML FOR VLSI DESIGN	L	T	P	C
		3	0	0	3

Course Objective:

- To deal comprehensively with all aspects of transistor level design of all the digital building blocks.
- To focus on the transistor level design.
- To address all important issues related to size, speed and power consumption.
- To deal with the memory architectures.
- To know the interconnect and clocking strategies.
- To understand the design of combinational and sequential CMOS circuits.

Course Outcomes:

23VLC14.CO1	Able to carry out transistor level hand calculation.
23VLC14.CO2	Able to design most important building blocks used in digital CMOS VLSI circuits.
23VLC14.CO3	Able to develop strong understanding of the design methodology.
23VLC14.CO4	Able to develop tradeoffs of the various circuit choices for each of all the blocks discussed.
23VLC14.CO5	Able to know the interconnect and clocking strategies.
23VLC14.CO6	Able to design combinational and sequential CMOS circuits.

Unit-I MACHINE LEARNING FOR ANALOG DESIGN 9

Machine Learning Taxonomy - VLSI CAD Abstraction Levels – Challenges in Analog – Mixed Signal design – Pre-Silicon Validation: Moment Estimation, Distribution Estimation – Post Silicon Tuning.

Unit-II LITHOGRAPHY AND PHYSICAL DESIGN 9

The Lithographic Patterning Process - Representation of the Lithographic Patterning Process - Machine Learning of Compact Process Models - Neural Network Compact Patterning Models.

Unit-III MASK SYNTHESIS 9

Machine Learning for Mask Synthesis - Machine Learning-Guided OPC - Machine Learning-Guided EPC: Etch Bias and EPC, Rule- and Model-Based EPC, Preparation of Training Segments, Extracting Parameters, Construction of Etch Bias Model, EPC Algorithm.

Unit-IV MACHINE LEARNING IN PHYSICAL VERIFICATION 9

Layout Feature Extraction and Encoding - Machine Learning Models for Hotspot Detection - Machine Learning for Sub- resolution Assist Features - Machine Learning for Optical Proximity Correction - Machine Learning for Routability-Driven Placement - Machine Learning for Clock Optimization.

Unit-V HARDWARE ARCHITECTURES 9

Software and Co-design Optimizations - Hardware-Level Techniques - Error Resilience Analysis: DNN-Specific Approximations for Low-Power Accelerators - Energy-Efficient Hardware Accelerator Design Methodology for Neural Networks - Efficient Machine Learning Architecture.

Total Periods: 45

Reference Books:

Sl.No.	Author(s)	Title of the Book	Publisher	Year of Publication
1.	Ibrahim (Abe)M. Elfadel, Duane S. Boning	Machine Learning in VLSI Computer-Aided Design	Springer	2019
2	Sandeep Saini, Kusum Lata, G.R. Sinha	VLSI and Hardware Implementations using Modern Machine Learning Methods	CRC Press	2021

23VLC15	RF INTEGRATED CIRCUIT DESIGN	L	T	P	C
		3	0	0	3

Course Objective:

- To understand the design considerations for RF Applications.
- To know the transceivers and amplifiers design procedures.
- To know the mixers for RF applications.
- To study about the Voltage Controlled Oscillators.
- To Understand the PLL and frequency synthesizers.

Course Outcomes:

23VLC15.CO1	Able to interpret the design concepts and considerations for RF applications.
23VLC15.CO2	Able to design the transceivers and amplifiers.
23VLC15.CO3	Able to apply the concepts to design mixers for RF.
23VLC15.CO4	Able to estimate the figure of merits of VCOs.
23VLC15.CO5	Able to analyze the performance of PL Land Frequency synthesizer.

Unit-I RF DESIGN **9**

RF Design Considerations – Effects of Nonlinearity – Noise – Sensitivity and Dynamic Range – Passive Impedance Transformation – Analysis of Nonlinear Dynamic Systems.

Unit-II TRANSCEIVERS AND AMPLIFIERS **9**

Receiver Architectures: Basic Heterodyne Receivers, Direct-Conversion Receivers, Image-Reject Receivers, Low-IF Receivers - Transmitter Architectures: Direct-Conversion Transmitters, Heterodyne Transmitters – Low Noise Amplifier: Common-Source Stage with Inductive Load and Resistive Feedback – Differential LNAs.

Unit-III MIXERS **9**

Mixer Noise Figures – Single-Balanced and Double-Balanced Mixers – Passive Down-conversion Mixers – Active Down-conversion Mixers.

Unit-IV OSCILLATORS **9**

Voltage-Controlled Oscillators – LC VCOs with Wide Tuning Range – Phase Noise: Basic Concepts, Effect of Phase Noise, Noise of Bias Current Source, Figures of Merit of VCOs – Design Procedure of Low-Noise VCOs – Mathematical Model of VCOs.

Unit-V PLL AND FREQUENCY SYNTHESIZERS **9**

Phase Detector – Phase Locked Loops: Analysis, Loop Dynamics, Frequency Multiplications – Charge Pumps – Charge-Pump PLLs Transient Response – Phase Noise in PLLs – Integer-N Synthesizer.

Total Periods: 45

Reference Books:

Sl.No.	Author(s)	Title of the Book	Publisher	Year of Publication
1.	B. Razavi	RF Microelectronics	Prentice-Hall	2007
2	Thomas H. Lee	The Design of CMOS Radio – Frequency Integrated Circuits	Cambridge University Press	2003

3	Bosco H Leung	VLSI for Wireless Communication	Springer	2011
4	Behzad Razavi	Design of Analog CMOS Integrated Circuits	McGraw-Hill	2017
6	Jia-sheng Hong	Micro strip filters for RF/Microwave applications	Wiley	2001

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23VLE01	ENGLISH FOR RESEARCH PAPER WRITING	L	T	P	C
		2	0	0	0

Course Objective:

Students will be able to:

- Understand that how to improve your writing skills and level of readability.
- Learn about what to write in each section.
- Understand the skills needed when writing a Title Ensure the good quality of paper at very first-time submission.

Unit-I **4**

Planning and Preparation, Word Order, Breaking up long sentences, Structuring Paragraphs and Sentences, Being Concise and Removing Redundancy, Avoiding Ambiguity and Vagueness

Unit-II **4**

Clarifying Who Did What, Highlighting Your Findings, Hedging and Criticising, Paraphrasing and Plagiarism, Sections of a Paper, Abstracts. Introduction 4 3 Review of the

Unit-III **4**

Review of the Literature, Methods, Results, Discussion, Conclusions, The Final Check

Unit-IV **4**

key skills are needed when writing a Title, key skills are needed when writing an Abstract, key skills are needed when writing an Introduction, skills needed when writing a Review of the Literature

Unit-V **4**

skills are needed when writing the Methods, skills needed when writing the Results, skills are needed when writing the Discussion, skills are needed when writing the Conclusions.

Unit-VI **4**

skills are needed when writing the Methods, skills needed when writing the Results, skills are needed when writing the Discussion, skills are needed when writing the Conclusions first- time submission

Total Periods 24

Reference Books:

Sl.No.	Author(s)	Title of the Book	Publisher	Year of Publication
1.	Goldbort R	Writing for Science	Yale University Press (available on Google Books)	2006
2	Day R	How to Write and Publish a Scientific Paper	Cambridge University Press	2006
3	Highman N	Handbook of Writing for the Mathematical Sciences	SIAM. Highman's book	1998
4	Adrian Wallwork	English for Writing Research Papers	Springer New York Dordrecht Heidelberg London	2011

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23VLE02	DISASTER MANAGEMENT	L	T	P	C
		2	0	0	0

Course Objective:

Students will be able to:

- Learn to demonstrate a critical understanding of key concepts in disaster risk reduction and humanitarian response.
- Critically evaluate disaster risk reduction and humanitarian response policy and practice from multiple perspectives.
- Develop and understanding of standards of humanitarian response and practical relevance in specific types of disasters and conflict situations.
- Critically understand the strengths and weaknesses of disaster management approaches, planning and programming in different countries, particularly their home country or the countries they work.

Unit-I Introduction Disaster **4**

Definition, Factors And Significance; Difference Between Hazard And Disaster; Natural And Manmade Disasters: Difference, Nature, Types And Magnitude.

Unit-II Repercussions Of Disasters And Hazards **4**

Economic Damage, Loss Of Human And Animal Life, Destruction Of Ecosystem. Natural Disasters: Earthquakes, Volcanisms, Cyclones, Tsunamis, Floods, Droughts And Famines, Landslides And Avalanches, Man-made disaster: Nuclear Reactor Meltdown, Industrial Accidents, Oil Slicks And Spills, Outbreaks Of Disease And Epidemics, War And Conflicts.

Unit-III Disaster Prone Areas In India Study Of Seismic Zones **4**

Areas Prone To Floods And Droughts, Landslides And Avalanches; Areas Prone To Cyclonic And Coastal Hazards With Special Reference To Tsunami; Post-Disaster Diseases And Epidemics

Unit-IV Disaster Preparedness And Management Preparedness **4**

Monitoring Of Phenomena Triggering A Disaster Or Hazard; Evaluation Of Risk: Application Of Remote Sensing, Data From Meteorological And Other Agencies, Media Reports: Governmental And Community Preparedness.

Unit-V Risk Assessment Disaster Risk **4**

Risk Reduction, Global And National Disaster Risk Situation. Techniques Of Risk Assessment, Global Co Operation In Risk Assessment And Warning, People's Participation In Risk Assessment. Strategies for Survival.

Unit-VI Disaster Mitigation: **4**

Meaning, Concept And Strategies Of Disaster Mitigation, Emerging Trends In Mitigation. Structural Mitigation And Non-Structural Mitigation, Programs Of Disaster Mitigation In India.

Total Periods 24

Reference Books:

Sl.No.	Author(s)	Title of the Book	Publisher
1.	R. Nishith, Singh AK	Disaster Management in India: Perspectives, issues and strategies	New Royal book Company.
2	Sahni, PardeepEt. Al.	Disaster Mitigation Experiences And Reflections	Prentice Hall Of India, New Delhi.
3	Goel S.L.	Disaster Administration And Management Text And Case Studies	1. Deep & Deep Publication Pvt. Ltd., New Delhi.

23VLE03	SANSKRIT FOR TECHNICAL KNOWLEDGE	L	T	P	C
		2	0	0	0

Course Objective:

- To get a working knowledge in illustrious Sanskrit, the scientific language in the world.
- Learning of Sanskrit to improve brain functioning.
- Learning of Sanskrit to develop the logic in mathematics, science & other subjects enhancing the memory power.
- The engineering scholars equipped with Sanskrit will be able to explore the huge knowledge from ancient literature.

Course Outcomes:

23VLE03.CO1	Understanding basic Sanskrit language.
23VLE03.CO2	Ancient Sanskrit literature about science & technology can be understood.
23VLE03.CO3	Being a logical language will help to develop logic in students.

Unit-I **8**

Alphabets in Sanskrit, Past/Present/Future Tense, Simple Sentences

Unit-II **8**

Order -Introduction of roots -Technical information about Sanskrit Literature

Unit-III **8**

Technical concepts of Engineering-Electrical, Mechanical, Architecture, Mathematics

Total Periods: 24

Reference Books:

Sl.No.	Author(s)	Title of the Book	Publisher
1.	Dr.Vishwas	Abhyaspustakam	Samskrita-Bharti Publication, New Delhi
2	Prathama Deeksha-Vempati Kutumbshastri	Teach Yourself Sanskrit	Rashtriya Sanskrit Sansthanam, New Delhi Publication
3	Suresh Soni	India's Glorious Scientific Tradition	Ocean books (P) Ltd., New Delhi

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23VLE04	VALUE EDUCATION	L	T	P	C
		2	0	0	0

Course Objective:

- To get a working knowledge in illustrious Sanskrit, the scientific language in the world.
- Learning of Sanskrit to improve brain functioning.
- Learning of Sanskrit to develop the logic in mathematics, science & other subjects enhancing the memory power.
- The engineering scholars equipped with Sanskrit will be able to explore the huge knowledge from ancient literature.

Course Outcomes:

23VLE04.CO1	Knowledge of self-development.
23VLE04.CO2	Learn the importance of Human values.
23VLE04.CO3	Developing the overall personality.

Unit-I **4**

Values and self-development –Social values and individual attitudes. Work ethics, Indian vision of humanism. Moral and non- moral valuation. Standards and principles. Value judgements

Unit-II **4**

Importance of cultivation of values. Sense of duty. Devotion, Self-reliance. Confidence, Concentration. Truthfulness, Cleanliness. Honesty, Humanity. Power of faith, National Unity. Patriotism. Love for nature ,Discipline

Unit-III **4**

Personality and Behavior Development - Soul and Scientific attitude. Positive Thinking. Integrity and discipline. Punctuality, Love and Kindness. Avoid fault Thinking. Free from anger, Dignity of labour. Universal brotherhood and religious tolerance. True friendship. Happiness Vs suffering, love for truth. Aware of self-destructive habits. Association and Cooperation. Doing best for saving nature

Unit-IV **4**

Character and Competence –Holy books vs Blind faith. Self-management and Good health. Science of reincarnation. Equality, Nonviolence, Humility, Role of Women. All religions and same message. Mind your Mind, Self-control. Honesty, Studying effectively

Total Periods: 16

Reference Books:

Sl.No.	Author(s)	Title of the Book	Publisher
1.	Chakroborty, S.K.	Values and Ethics for organizations Theory and practice	Oxford University Press, New Delhi

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23VLE05	CONSTITUTION OF INDIA	L	T	P	C
		2	0	0	0

Course Objective:

Students will be able to:

- Understand the premises in forming the twin themes of liberty and freedom from a civil rights perspective.
- To address the growth of Indian opinion regarding modern Indian intellectuals' constitutional role and entitlement to civil and economic rights as well as the emergence of nationhood in the early years of Indian nationalism.
- To address the role of socialism in India after the commencement of the Bolshevik Revolution in 1917 and its impact on the initial drafting of the Indian Constitution.

Course Outcomes:

23VLE05.CO1	Discuss the growth of the demand for civil rights in India for the bulk of Indians before the arrival of Gandhi in Indian politics.
23VLE05.CO2	Discusstheintellectualoriginsoftheframeworkofargumentthatinformedthe conceptualization of social reforms leading to revolution in India.
23VLE05.CO3	Discuss the circumstances surrounding the foundation of the Congress Socialist Party[CSP] under the leadership of Jawaharlal Nehru and the eventual failure of the proposal of direct elections through adult suffrage in the Indian Constitution.
23VLE05.CO4	DiscussthepassageoftheHinduCodeBillof1956.

Unit-I History of Making of the Indian Constitution 4

History Drafting Committee, (Composition & Working)

Unit-II Philosophy of the Indian Constitution 4

Preamble Salient Features

Unit-III Contours of Constitutional Rights & Duties 4

Fundamental Rights Right to Equality Right to Freedom Right against Exploitation Right to Freedom of Religion Cultural and Educational Rights Right to Constitutional Remedies Directive Principles of State Policy Fundamental Duties.

Unit-IV Organs of Governance 4

Parliament Composition Qualifications and Disqualifications Powers and Functions Executive President Governor Council of Ministers Judiciary, Appointment and Transfer of Judges, Qualifications Powers and Functions

Unit-V Local Administration 4

District's Administration head: Role and Importance, Municipalities: Introduction, Mayor and role of Elected Representative, CEO of Municipal Corporation. Pachayati raj: Introduction, PRI: Zila Pachayat. Elected officials and their roles, CEO Zila Pachayat: Position and role. Block level: Organizational Hierarchy (Different departments), Village level: Role of Elected and Appointed officials, Importance of grass root democracy

Unit-VI Election Commission 4

Election Commission: Role and Functioning. Chief Election Commissioner and Election Commissioners. State Election Commission: Role and Functioning. Institute and Bodies for the welfare of SC/ST/OBC and women.

Total Periods 24

Reference Books:

Sl.No.	Author(s)	Title of the Book	Publisher	Year of Publication
1.	Dr. B.R. Ambedkar	The Constitution of India, 1950 (Bare Act)	Government Publication	1950

2	Dr. S. N. Busi	Dr. B. R. Ambedkar framing of Indian Constitution, 1st Edition, 2015	Government Publication	2015
3	M. P. Jain	Indian Constitution Law, 7th Edn.,	Lexis Nexis	2014
4	D.D. Basu	Introduction to the Constitution of India	Lexis Nexis	2015

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23VLE06	PEDAGOGY STUDIES	L	T	P	C
		2	0	0	0

Course Objective:

Students will be able to:

- Review existing evidence on the review topic to inform programme design and policy making undertaken by the DfID, other agencies and researchers.
- Identify critical evidence gaps to guide the development.

Course Outcomes:

23VLE06.CO1	What pedagogical practices are being used by teachers in formal and informal classrooms in developing countries?
23VLE06.CO2	What is the evidence on the effectiveness of these pedagogical practices, in what conditions, and with what population of learners?
23VLE06.CO3	How can teacher education (curriculum and practicum)and the school curriculum and guidance materials best support effective pedagogy?

Unit-I Introduction and Methodology: 4

Aims and rationale, Policy background, Conceptual framework and terminology Theories of learning, Curriculum, Teacher education. Conceptual framework, Research questions**.** Overview of methodology and Searching.

Unit-II 4

Thematic overview: Pedagogical practices are being used by teachers in formal and informal classrooms in developing countries. Curriculum, Teacher education.

Unit-III 4

Evidence on the effectiveness of pedagogical practices Methodology for the in depth stage: quality assessment of included studies. How can teacher education (curriculum and practicum) and the school curriculum and guidance materials best support effective pedagogy? Theory of change. Strength and nature of the body of evidence for effective pedagogical practices. Pedagogic theory and pedagogical approaches. Teachers' attitudes and beliefs and Pedagogic strategies.

Unit-IV 4

Professional development: alignment with classroom practices and follow-up Support Peer support Support from the head teacher and the community. Curriculum and assessment Barriers to learning: limited resources and large class sizes

Unit-V Research gaps and future directions 4

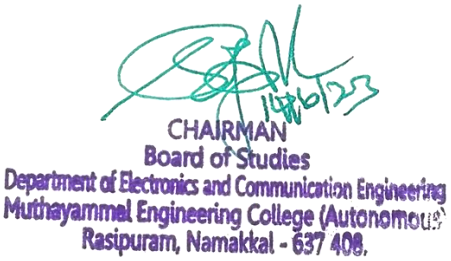
Research design Contexts Pedagogy Teacher education Curriculum and assessment Dissemination and research impact.

Total Periods 20

Reference Books:

Sl.No.	Author(s)	Title of the Book	Publisher	Year of Publication
1.	Ackers J, Hardman F	Classroom interaction in Kenyan primary schools	Compare, 31 (2):245-261	2001
2	Agrawal M	Curricular reform in schools: The importance of evaluation	Journal of Curriculum Studies, 36 (3): 361-379.	2004
3	Akyeampong K	Teacher training in Ghana - does it count? Multi-site teacher education research project (MUSTER) country report 1.	London: DFID	2003

4	Akyeampong K, Lussier K, Pryor J, Westbrook J	Improving teaching and learning of basic maths and reading in Africa: Does teacher preparation count?	International Journal Educational Development, 33 (3): 272–282.	2013
5	AlexanderRJ	Culture and pedagogy: International comparisons in primary education	Oxford and Boston: Blackwell.	2001
6	ChavanM	Read India: A mass scale, rapid, 'learning to read' campaign www.pratham.org/images/resource%20working%20paper%202.pdf.	Nil	2003



23VLE07	STRESS MANAGEMENT BY YOGA	L	T	P	C
		2	0	0	0

Course Objective:

- To achieve overall health of body and mind.
- To overcome stress.

Course Outcomes:

23VLE07.CO1	Develop healthy mind in a healthy body thus improving social health also.
23VLE07.CO2	Improve efficiency.

Unit-I **8**

Definitions of Eight parts of yoga. (Ashtanga)

Unit-II **8**

Yam and Niyam. Do`s and Don't's in life. Ahinsa, satya, astheya, bramhacharya and aparigraha Shaucha, santosh, tapa, swadhyay, ishwarpranidhan

Unit-III **8**

Asan and Pranayam Various yoga poses and their benefits for mind & body- Regularization of breathing techniques and its effects-Types of pranayam

Total Periods 24

Reference Books:

Sl.No.	Author(s)	Title of the Book	Publisher
1.	Janardan Swami	Yogic Asanas for Group Tarining-Part-I	Yogabhyasi Mandal, Nagpur
2	Swami Vivekananda	Rajayoga or conquering the Internal Nature	Advaita Ashrama (Publication Department), Kolkata

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23VLE08	PERSONALITY DEVELOPMENT THROUGH LIFE ENLIGHTENMENT SKILLS	L	T	P	C
		2	0	0	0

Course Objective:

- To learn to achieve the highest goal happily.
- To become a person with stable mind, pleasing personality and determination.
- To awaken wisdom in students.

Course Outcomes:

23VLE08.CO1	Study of Shrimad-Bhagwad-Geeta will help the student in developing his personality and achieve the highest goal in life.
23VLE08.CO2	The person who has studied Geeta will lead the nation and mankind to peace and prosperity.
23VLE08.CO3	Study of Neetishatakam will help in developing versatile personality of students.

Unit-I **8**

Neetisatakam-Holistic development of personality:

- Verses- 19,20,21,22 (wisdom)
- Verses- 29,31,32 (pride & heroism)
- Verses- 26,28,63,65 (virtue)
- Verses- 52,53,59 (dont's)
- Verses- 71,73,75,78 (do's)

Unit-II **8**

- Approach to day to day work and duties.
- Shrimad Bhagwad Geeta : Chapter 2-Verses 41, 47,48,
- Chapter 3-Verses 13, 21, 27, 35, Chapter 6-Verses 5,13,17, 23, 35,
- Chapter 18-Verses 45, 46, 48.

Unit-III **8**

- Statements of basic knowledge.
- Shrimad Bhagwad Geeta: Chapter2-Verses 56, 62, 68
- Chapter 12 -Verses 13, 14, 15, 16,17, 18
- Personality of Role model. Shrimad Bhagwad Geeta:
- Chapter2-Verses 17, Chapter 3-Verses 36,37,42,
- Chapter 4-Verses 18, 38,39
- Chapter18 – Verses 37,38,63

Total Periods **24**

Reference Books:

Sl.No.	Author(s)	Title of the Book	Publisher
1.	Swami Swarupananda	Srimad Bhagavad Gita	Advaita Ashram (Publication Department), Kolkata
2	Bhartrihari's Three Satakam (Niti-sringar-vairagya)	P.Gopinath	Rashtriya Sanskrit Sansthanam, New Delhi.

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