MUTHAYAMMAL ENGINEERING COLLEGE
(An Autonomous Institution)
(Approved by AICTE, New Delhi, Accredited by NAAC, NBA & Affiliated to Anna University)
Rasipuram - 637 408, Namakkal Dist., Tamil Nadu.

Curriculum/Syllabus

Programme Code   : VL

Programme Name : M.E.- VLSI DESIGN

Regulation   : R-2019

MUTHAYAMMAL ENGINEERING COLLEGE
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Rasipuram - 637 408, Namakkal Dt, Tamil Nadu.

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Rasipuram - 637 408, Namakkal Dist., Tamil Nadu.

INSTITUTION VISION & MISSION

INSTITUTION VISION

To be a Centre of Excellence in Engineering, Technology and Management on par with International Standards

INSTITUTION MISSION

- To prepare the students with high professional skills and ethical values
- To impart knowledge through best practices
- To instill a spirit of innovation through Training, Research and Development
- To undertake continuous assessment and remedial measures
- To achieve academic excellence through intellectual, emotional and social stimulation

INSTITUTION MOTTO

Rural upliftment through Technical Education

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DEPARTMENT VISION & MISSION

DEPARTMENT VISION

To empower the electronics and communication engineering students on basics and advanced technologies in both theoretical and experimental practices with research attitude and ethics

DEPARTMENT MISSION

- To impart need based education in electronics and communication engineering to meet the requirements of academic, industry and society
- To establish the state-of-art laboratories to prepare the students for facing the challenges ahead
- To prepare the students for employment, higher education and research oriented activities

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DEPARTMENT PROGRAM EDUCATIONAL OBJECTIVES, PROGRAM OUTCOMES
& PROGRAM SPECIFIC OUTCOMES

PROGRAM EDUCATIONAL OBJECTIVES

The Electronics and Communication Engineering Graduates should be able to

PEO1: Pursue as an engineer with necessary conceptual, analytical and theoretical knowledge in the domain of electronics and communication engineering

PEO2: Acquire the practical knowledge through basics and advanced laboratories in the field of electronics and communication engineering

PEO3: Demonstrate the leadership skills through entrepreneurship, employment and higher studies and to practice ethical values for the benefit of society and environment

PROGRAM OUTCOMES

1. **Engineering Knowledge:** Apply the knowledge of mathematics, science, engineering fundamentals, and an engineering specialization to the solution of complex engineering problems.

2. **Problem Analysis:** Identify, formulate, review research literature, and analyze complex engineering problems reaching substantiated conclusions using first principles of mathematics, natural sciences, and engineering sciences

3. **Design/Development solutions:** Design solutions for complex engineering problems and design system components or processes that meet the specified needs with appropriate consideration for the public health and safety, and the cultural, societal, and environmental considerations.

4. **Conduct investigations of complex problems:** Use research-based knowledge and research methods including design of experiments, analysis and interpretation of data, and synthesis of the information to provide valid conclusions.

5. **Modern tool usage:** Create, select, and apply appropriate techniques, resources, and modern engineering and IT tools including prediction and modeling to complex engineering activities with an understanding of the limitations.

6. **The engineer and society:** Apply reasoning informed by the contextual knowledge to assess societal, health, safety, legal and cultural issues and the consequent responsibilities relevant to the professional engineering practice.

7. **Environment and sustainability**: Understand the impact of the professional engineering solutions in societal and environmental contexts, and demonstrate the knowledge of, and need for sustainable development.

8. **Ethics:** Apply ethical principles and commit to professional ethics and responsibilities and norms of the engineering practice.

9. **Individual and team work:** Function effectively as an individual and as a member or leader in diverse teams, and in multidisciplinary settings.

10. **Communication:** Communicate effectively on complex engineering activities with the engineering community and with society at large, such as, being able to comprehend and write effective reports and design documentation, make effective presentations, and give and receive clear instructions.

11. **Project management and finance:** Demonstrate knowledge and understanding of the engineering management principles and apply these to one's own work, as a member and leader in a team, to manage projects and in multidisciplinary environments.

12. **Lifelong learning:** Recognize the need for and have the preparation and ability to engage in independent and lifelong learning in the broadest context of technological change.

PROGRAM SPECIFIC OUTCOMES

PSO1: Design and analyze electronic circuits and systems for various applications

PSO2: Apply the acquired knowledge and analytical skills for modeling and simulation of advanced communication systems

PSO3: Ascertain the use of software and hardware tools for developing variety of electronics and communication systems

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M.E. – VLSI DESIGN

GROUPING OF COURSES

FOUNDATION COURSES (FC):

S.No.	Course Code	Course Title	Category	Contact Hours	Instruction Hours/week			Credit
					L	T	P	C
1.	19VLA01	Advanced Numerical Methods	FC	5	3	2	0	4
2.	19VLA02	Applied Mathematics	FC	5	3	2	0	4
3.	19VLA03	Applied Probability and Statistics	FC	5	3	2	0	4

Professional Core (PC):

S.No.	Course Code	Course Title	Category	Contact Hours	Instruction Hours/week			Credit
					L	T	P	C
1.	19VLB01	VLSI Signal Processing	PC	5	?	2	0	4
2.	19VLB02	VLSI Design Techniques	PC	3	3	0	0	3
3.	19VLB03	Analog VLSI Circuit Design	PC	3	3	0	0	3
4.	19VLB04	Solid State Device Modeling and Simulation	PC	3	3	0	0	3
5.	19VLB05	ASIC Design		3	3	0	0	3
6.	19VLB07	Digital CMOS VLSI Design	PC	5	3	0	0	3
7.	19VLB08	CAD for VLSI Circuits	PC	5	3	2	0	4
8.	19VLB09	Low Power VLSI Design	PC	3	3	0	0	3
9.	19VLB11	Testing of VLSI Circuits	PC	3	3	0	0	3
10.	19VLB06	VLSI Design Techniques Laboratory	PC	2	0	0	2	1
11.	19VLB10	Digital CMOS VLSI Design Laboratory	PC	2	0	0	2	1

Professional Electives (PE):

S.No.	Course Code	Course Title	Category	Contact Hours	Instruction Hours/week			Credit
					L	T	P	C
1.	19VLC01	Signal Integrity for High Speed Devices	PE	3	3	0	0	3
2.	19VLC02	Advanced Digital System Design	PE	3	3	0	0	3
3.	19VLC03	Submicron VLSI Design	PE	3	3	0	0	3
4.	19VLC04	VLSI Technology	PE	3	3	0	0	3
5.	19VLC05	DSP Integrated Circuits	PE	3	3	0	0	3
6.	19VLC06	ARM Processor and Applications	PE	3	3	0	0	3
7.	19VLC07	Hardware Design Verification Techniques	PE	3	3	0	0	3
8.	19VLC08	Design and Analysis of Algorithms	PE	3	3	0	0	3
9.	19VLC09	MEMS and NEMS	PE	3	3	0	0	3
10.	19VLC10	Soft Computing	PE	3	3	0	0	3
11.	19VLC11	VLSI for Wireless Communication	PE	3	3	0	0	3
12.	19VLC12	Reconfigurable Architectures	PE	3	3	0	0	3
13.	19VLC13	Research Methodology	PE	3	3	0	0	3
14.	19VLC14	RF Integrated Circuit Design	PE	3	3	0	0	3
15.	19VLC15	Electromagnetic Interference and Compatibility	PE	3	3	0	0	3
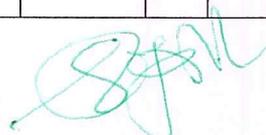
Employability Enhancement Courses (EEC):

S.No.	Course Code	Course Title	Category	Contact Hours	Instruction Hours/week			Credit
					L	T	P	C
1.	19VLD01	Project Work Phase -I	EEC	12	0	0	12	6
2.	19VLD02	Project Work Phase -II	EEC	24	0	0	24	12

Audit Courses (AC) :

S.No.	Course Code	Course Title	Category	Contact Hours	Instruction Hours/week			Credit
					L	T	P	C
1.	19VLE01	English for Research Paper Writing	AC	2	2	0	0	0
2.	19VLE02	Disaster Management	AC	2	2	0	0	0
3.	19VLE03	Sanskrit for Technical Knowledge	AC	2	2	0	0	0
4.	19VLE04	Value Education	AC	2	2	0	0	0
5.	19VLE05	Constitution of India	AC	2	2	0	0	0
6.	19VLE06	Pedagogy Studies	AC	2	2	0	0	0
7.	19VLE07	Stress Management by Yoga	AC	2	2	0	0	0
8.	19VLE08	Personality Development through Life Enlightenment Skills.	AC	2	2	0	0	0

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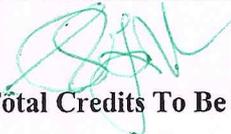Rasipuram, Namakkal - 637 408.

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	CURRICULUM PG R - 2019

Department	Electronics and Communication Engineering
Programme	M.E. – VLSI Design

SEMESTER - I

SI. No.	Course Code	Course Name	Hours/ Week			Credit	Contact Hours
			L	T	P	C	
THEORY							
1.	19VLA02	Applied Mathematics	3	2	0	4	5
2.	19VLB01	VLSI Signal Processing	3	2	0	4	5
3.	19VLB02	VLSI Design Techniques	3	0	0	3	5
4.	19VLB03	Analog VLSI Circuit Design	3	0	0	3	3
5.	19VLB04	Solid State Device Modeling and Simulation	3	0	0	3	3
6.	19VLB05	ASIC Design	3	0	0	3	3
7.	19VLB06	VLSI Design Techniques Laboratory	0	0	2	1	2
			Total Credits			**21**	

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	CURRICULUM PG R - 2019

Department	Electronics and Communication Engineering
Programme	M.E. – VLSI Design

SEMESTER - II

SI. No.	Course Code	Course Name	Hours/ Week			Credit	Contact Hours
			L	T	P	C	
THEORY							
1.	19VLB07	Digital CMOS VLSI Design	3	0	0	3	5
2.	19VLB08	CAD for VLSI Circuits	3	2	0	4	5
3.	19VLB09	Low Power VLSI Design	3	0	0	3	3
4.		Elective I	3	0	0	3	3
5.		Elective II	3	0	0	3	3
6.		Elective III	3	0	0	3	3
7	19VLB10	Digital CMOS VLSI Design Laboratory	0	0	2	1	2
8.		Audit Course 1	2	0	0	0	2
			Total Credits			**20**	

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CURRICULUM PG R - 2019

Department	Electronics and Communication Engineering
Programme	M.E. – VLSI Design

SEMESTER - III

Sl. No.	Course Code	Course Name	Hours/ Week			Credit	Contact Hours
			L	T	P	C	
THEORY							
1.	19VLB09	Testing of VLSI Circuits	3	0	0	3	3
2.		Elective IV	3	0	0	3	3
3.		Elective V	3	0	0	3	3
4.		Audit Course - 2	2	0	0	0	2
PRACTICAL							
5.	19VLD01	Project Work Phase-I	0	0	12	6	12
					Total Credits	**15**	

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CURRICULUM PG R - 2019

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SEMESTER - IV

Sl. No.	Course Code	Course Name	Hours/ Week			Credit	Contact Hours
			L	T	P	C	
PRACTICAL							
1.	19VLD02	Project Work Phase-II	0	0	24	12	24
					Total Credits	**12**	

Total Credits To Be Earned For The Award Of Degree: 68

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19VLA01	ADVANCED NUMERICAL METHODS	L T P C
		3 2 0 4

COURSE OBJECTIVES :

- To learn the algebraic equations which finds applications in many engineering branches.
- To make the student acquire sound knowledge of computational techniques in solving ordinary differential equations that model engineering.
- To solve Elliptic equations by using computational techniques.
- To introduce numerical tools for the solutions of partial differential equations that model several physical processes.
- To deal with interpolation and approximation for the application of finite element analysis.
- To impart knowledge on numerical methods that will come in handy to solve numerically the problems that arise in engineering and technology.

COURSE OUTCOMES :

- Demonstrate understanding and implementation of numerical solution algorithms applied to solve algebraic equations.
- Be familiar with numerical solutions of ordinary differential equation and partial differential equations.
- Be competent with finite difference method and finite element method.
- Understanding the theoretical and practical aspects of the use of numerical methods. Implementing numerical methods for a variety of multidisciplinary applications. Establishing the limitations, advantages, and disadvantages of numerical methods.
- The students will have a clear perception of the power of numerical Techniques. This will also serve as a precursor for future research.
- Students would be able to demonstrate the applications of numerical techniques to problems drawn from industry, management and other engineering fields.

UNIT I : ALGEBRAIC EQUATIONS   9+6
Systems of linear equations: Gauss Elimination method, pivoting techniques, Thomas algorithm for tridiagonal system – Jacobi, Gauss Seidel, SOR iteration methods - Systems of nonlinear equations: Fixed point iterations, Newton Method, Eigenvalue problems: power method, inverse power method, Faddeev – Leverrier Method.

UNIT II : ORDINARY DIFFERENTIAL EQUATIONS   9+6
Runge Kutta Methods for system of IVPs, numerical stability, Adams - Bashforth multistep method, solution of stiff ODEs, shooting method, BVP: Finite difference method, orthogonal collocation method, orthogonal collocation with finite element method, galerkin finite element method.

UNIT III : FINITE DIFFERENCE METHOD FOR TIME DEPENDENT PARTIAL DIFFERENTIAL EQUATIONS
                                                                     9+6
Parabolic equations: explicit and implicit finite difference methods, weighted average approximation - Dirichlet and Neumann conditions – Two dimensional parabolic equations – ADI method; First order hyperbolic equations – method of characteristics, different explicit and implicit methods; numerical stability analysis, method of lines – Wave equation: Explicit scheme - Stability of above schemes.

UNIT IV : FINITE DIFFERENCE METHODS FOR ELLIPTIC EQUATIONS   9+6
Laplace and Poisson's equations in a rectangular region: Five point finite difference schemes, Leibmann's iterative methods, Dirichlet and Neumann conditions – Laplace equation in polar coordinates: finite difference schemes – approximation of derivatives near a curved boundary while using a square mesh.

UNIT V : FINITE ELEMENT METHOD   9+6

Partial differential equations – Finite element method – orthogonal collocation method, orthogonal collocation with finite element method, Galerkin finite element method.

TOTAL: 45 + 30 Hours

REFERENCE BOOKS:

Sl.No	Author(s)	Title of the Book	Publisher	Year of Publication
1.	M.K. Jain , S.R.K. Iyengar, R.K. Jain	Computational Methods for Partial Differential Equations, 2nd Edition	New Age Publishers	2019
2.	S. K. Gupta	Numerical Methods for Engineers, 3rd Edition	New Age International Pvt Ltd Publishers	2015
3.	Saumyen Guha and Rajesh Srivastava	Numerical methods for Engineering and Science	Oxford Higher Education, New Delhi	2010
4.	M.K. Jain	Numerical Methods for Scientific & Engineering Computation, 6th Edition	New Age International Publishers	2010
5.	Burden, R.L., and Faires, J.D.	Numerical Analysis –Theory and Applications	Cengage Learning, India Edition, New Delhi	2009

WEB URLs :
1. http://nptel.ac.in/courses/103101111/downloads/Lecture-notes/Module_4_Solving_Ax=b.pdf
2. www.youtube.com/watch?v=FmhMUTmUjhM
3. https://mat.iitm.ac.in/home/sryedida/public_html/caimna/pde/fifth/example.html
4. www.youtube.com/watch?v=BERb9PRiVB4
5. www.math.tifr.res.in/~publ/ln/tifr49.pdf

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19VLA02	APPLIED MATHEMATICS	L T P C
		3 2 0 4

COURSE OBJECTIVES :

- To realize the use of matrix theory techniques in engineering applications and to develop for future applications.
- To analyze and solve the fundamental problem with prescribed or free boundary conditions in simple cases
- Demonstrate knowledge of mathematics and mechanics to construct, analyze and interpret real world problems
- Provide a foundation and motivation for exposure to statistical ideas subsequent to the course.
- To formulate and construct a mathematical model for a linear programming problem in real life situation
- To introduce Fourier series analysis which is central to many applications in engineering

COURSE OUTCOMES :

- Explain geometrical concepts related to orthogonality and least squares solutions and perform calculations related to orthogonality.
- The variation calculus makes access to mastering in a wide range of classical results of variational calculus. Students get up apply results in technical problem solutions
- The students will have a basic knowledge of the main fields of mathematics and mechanics, including differential equations, elasticity theory, fluid mechanics.
- The students will have an exposure of various distribution functions and help in acquiring skills in handling situations involving more than one variable
- The knowledge gained on this course helps the students to do engineering optimization.
- Demonstrate an understanding of the basic concepts of Fourier series analysis

UNIT I : MATRIX THEORY   9+6
The Cholesky decomposition - Generalized Eigen vectors, Canonical basis - QR factorization - Least squares method - Singular value decomposition.

UNIT II : CALCULUS OF VARIATIONS   9+6
Concept of variation and its properties – Euler's equation – Functional dependant on first and higher order derivatives – Functionals dependant on functions of several independent variables – Variational problems with moving boundaries – problems with constraints - Direct methods: Ritz and Kantorovich methods.

UNIT III: ONE DIMENSIONAL RANDOM VARIABLES   9+6
Random variables - Probability function – moments – moment generating functions and their properties – Binomial, Poisson, Geometric, Uniform, Exponential, Gamma and Normal distributions – Function of a Random Variable.

UNIT IV: LINEAR PROGRAMMING   9+6
Formulation – Graphical solution – Simplex method – Two phase method - Transportation and Assignment Models

UNIT V: FOURIER SERIES AND EIGEN VALUE PROBLEMS   9+6
Fourier Trigonometric series: Periodic function as power signals – Convergence of series – Even and odd function: cosine and sine series – Non-periodic function: Extension to other intervals - Power signals: Exponential Fourier series – Parseval's theorem and power spectrum – Eigen value problems and orthogonal functions – Regular Sturm-Liouville systems – Generalized Fourier series.

TOTAL: 45 + 30 Hours

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REFERENCE BOOKS:

Sl.No	Author(s)	Title of the Book	Publisher	Year of Publication
1.	Mital.K.V. Mohan and Chander	Optimization Methods in Operations Research and Systems Analysis, 4th Edition	New Age International Publishers	2019
2.	Stark. H., and Woods. J.W.	Probability and Random Processes with Applications to Signal Processing, 4th Edition	Pearson Education, Asia	2014
3.	Hamdy ATaha	Operations Research, 9th Edition (Asia)	Pearson Education, Asia	2014
4.	Gupta, A.S.	Calculus of Variations with Applications	Prentice Hall of India Pvt. Ltd., New Delhi	2011
5.	Richard Bronson	Matrix Operation, Schaum's outline series, 2nd Edition	McGraw Hill	2011

WEB URLs

1. http://nptel.ac.in/courses/111108066/ http://www.cs.utexas.edu/~pingali/CS378/2011sp/lectures/chol4.pdf
2. http://www.math.uni-leipzig.de/~miersemann/variabook.pdf
3. http://nptel.ac.in/courses/IIT-MADRAS/Principles_of_Communication1/Pdfs/1_5.pdf
4. http://nptel.ac.in/courses/111104027/
5. http://nptel.ac.in/courses/111106046/

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19VLA03	APPLIED PROBABILITY AND STATISTICS	L T P C
		3 2 0 4

COURSE OBJECTIVES :

- To introduce the basic concepts of one dimensional and two dimensional Random Variables.
- To gain knowledge in the application of family of random variables in real life situations
- To provide information about Correlation and Regression
- Learn about maximum likelihood estimation, unbiased estimation and least square methods.
- To understand concepts of testing of hypothesis
- To enable the students to use the concepts of multivariate normal distribution and principle components analysis.

COURSE OUTCOMES :

- Analyze random or unpredictable experiments and investigate important features of random experiments. Construct probabilistic models for observed phenomena through distributions which play an important role in many engineering applications.
- Associate random variables by designing joint distributions and correlate the random variables
- Perform and interpret correlation and regression analysis and develop correlation models to predict changes in processes and products for linear and non-linear relationships
- Provides knowledge to apply testing of hypothesis to real life problems.
- Be familiar with multivariate analysis.
- The student will able to acquire the basic concepts of Probability and Statistical techniques for solving mathematical problems which will be useful in solving Engineering problems.

UNIT I : ONE DIMENSIONAL RANDOM VARIABLES   9+6

Random variables - Probability function – Moments – Moment generating functions and their properties – Binomial, Poisson, Geometric, Uniform, Exponential, Gamma and Normal distributions – Functions of a Random Variable.

UNIT II: TWO DIMENSIONAL RANDOM VARIABLES   9+6

Joint distributions – Marginal and Conditional distributions – Functions of two dimensional random variables – Regression Curve – Correlation.

UNIT III : ESTIMATION THEORY   9+6

Unbiased Estimators – Method of Moments – Maximum Likelihood Estimation - Curve fitting by Principle of least squares – Regression Lines..

UNIT IV: TESTING OF HYPOTHESES   9+6

Sampling distributions - Type I and Type II errors - Tests based on Normal, t, Chi-Square and F distributions for testing of mean, variance and proportions – Tests for Independence of attributes and Goodness of fit.

UNIT V: MULTIVARIATE ANALYSIS   9+6

Random Vectors and Matrices - Mean vectors and Covariance matrices - Multivariate Normal density and its properties - Principal components Population principal components – Principal components from standardized variables.

TOTAL: 45 + 30 Hours

REFERENCE BOOKS:

Sl.No	Author(s)	Title of the Book	Publisher	Year of Publication
1.	Douglas C. Montgomery, George C. Runger	Applied Statistics and Probability for Engineers (International Student Version), 6th Edition	John Wiley & Sons, Inc.	2019
2.	Richard A. Johnson and Dean W. Wichern,	Applied Multivariate Statistical Analysis, 6th Edition	Pearson Education, Asia	2015

3.	Gupta S.C. and Kapoor V.K	Fundamentals of Mathematical Statistics	Sultan Chand & Sons	2014
4.	HweiP.Hsu,	Schaum"s Outline of Theory and Problems of Probability, Random Variables and Random Processes	Tata Mc Graw Hill Edition, New Delhi	2014
5.	Walpole. R.E., Myers. R.H., Myers. S.L., and Ye. K., ,	Probability and Statistics for Engineers and Scientists, 8th Edition	Pearson Education, Asia	2013

WEB URLs :
1. http://www.maths.qmul.ac.uk/~pettit/MAS109/chp4.pdf
2. http://nptel.ac.in/courses/117104117/
3. http://www.efunda.com/math/leastsquares/leastsquares.cfm
4. http://nptel.ac.in/courses/111105041/33
5. http://nptel.ac.in/courses/110105060/

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Professional Core (PC)

19VLB01	VLSI SIGNAL PROCESSING	L T P C 3 2 0 4

COURSE OBJECTIVES:

- To understand the various VLSI architectures for digital signal processing
- To know the methods of critical path reduction.
- To know the techniques of critical path and algorithmic strength reduction in the filter structures.
- To study the performance parameters, viz. area, speed and power
- To carry out HDL simulation of various DSP algorithms.
- To understand synchronous ,asynchronous pipelining

COURSE OUTCOMES:

- To be able to design architectures for DSP algorithms.
- To be able to optimize design in terms of area, speed and power
- To be able to design recursive and adaptive filters.
- To be able to incorporate pipeline based architectures in the design
- To be able to carry out HDL simulation of various DSP algorithms
- To be able to analyze synchronous, asynchronous pipelining

UNIT I: INTRODUCTION   9
Overview of DSP – FPGA Technology – DSP Technology requirements – Design Implementation.

UNIT II: METHODS OF CRITICAL PATH REDUCTION   9
Binary Adders – Binary Multipliers – Multiply-Accumulator (MAC) and sum of product (SOP) –Pipelining and parallel processing – retiming – unfolding – systolic architecture design.

UNIT III: ALGORITHMIC STRENGTH REDUCTION METHODS AND RECURSIVE FILTER DESIGN   9
Fast convolution-pipelined and parallel processing of recursive and adaptive filters – fast IIR filters design.

UNIT IV: DESIGN OF PIPELINED DIGITAL FILTERS   9
Designing FIR filters – Digital lattice filter structures – bit level arithmetic architecture – redundant arithmetic – scaling and round-off noise.

UNIT V: SYNCHRONOUS, ASYNCHRONOUS PIPELINING AND PROGRAMMABLE DSP   9
Numeric strength reduction – synchronous – wave and asynchronous pipelines – low power design – programmable DSPs – DSP architectural features/alternatives for high performance and low power.

TOTAL: 45 Hours

REFERENCE BOOKS:

Sl.No	Author(s)	Title of the Book	Publisher	Year of Publication
1.	Keshab K.Parhi	VLSI Digital Signal Processing Systems, Design and Implementation	John Wiley	2007
2.	U. Meyer – Baese	Digital Signal Processing with Field Programmable Arrays	Springer, Second Edition,	2007
3.	S.Y.Kuang, H.J. White house, T. Kailath	VLSI and Modern Signal Processing	Prentice Hall	1995
4.	Gary Yeap	Practical Low Power Digital VLSI Design	Kluwer Academic Publishers	1998
5.	Mohammed Ismail and Terri Fiez	Analog VLSI Signal and Information Processing	Mc Graw-Hill	1994

WEB URLs :

1. nptel.kmeacollege.ac.in/syllabus/117101006/
2. www.smdp2vlsi.gov.in/smdp2vlsi/publicationIEP-vlsi-dsp-design-iikgp-n.jsp
3. nptel.ac.in/courses/117106087
4. www.ee.ucla.edu/~ingrid/ee213a/lectures/lectures.html
5. www.ee.iitm.ac.in/videolectures/doku.php?id=ee658_2008:start

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19VLB02	VLSI DESIGN TECHNIQUES	L T P C
		3 0 0 3

COURSE OBJECTIVES:

- To understand the concepts of MOS transistors operations and their AC and DC characteristics.
- To know the fabrication process of cmos technology and its layout design rules
- To understand the latch up problem in cmos circuits.
- To study the concepts of cmos invertors and their sizing methods
- To know the concepts of power estimation and delay calculations in cmos circuits.
- To study the concepts of digital VLSI circuits

COURSE OUTCOMES:

- To be able to understand the concepts of MOS transistors operations and their AC and DC characteristics.
- To be able to know the fabrication process of cmos technology and its layout design rules
- To be able to understand the latch up problem in cmos circuits.
- To be able to know the concepts of cmos invertors and their sizing methods
- To be able to know the concepts of power estimation and delay calculations in cmos circuits.
- To be able to design digital VLSI circuits

UNIT I: MOS TRANSISTOR THEORY 9
NMOS and PMOS transistors, CMOS logic, MOS transistor theory – Introduction, Enhancement mode transistor action, Ideal I-V characteristics, DC transfer characteristics, Threshold voltage- Body effect- Design equations- Second order effects. MOS models and small signal AC characteristics, Simple MOS capacitance Models, Detailed MOS gate capacitance model, Detailed MOS Diffusion capacitance mode.

UNIT II: CMOS TECHNOLOGY AND DESIGN RULE 9
CMOS fabrication and Layout, CMOS technologies, P -Well process, N -Well process, twin –tub process, MOS layers stick diagrams and Layout diagram, Layout design rules, Latch up in CMOS circuits, CMOS process enhancements, Technology – related CAD issues, Fabrication and packaging.

UNIT III:INVERTERS AND LOGIC GATES 9
NMOS and CMOS Inverters, Inverter ratio, DC and transient characteristics , switching times. Super buffers, Driving large capacitance loads, CMOS logic structures , Transmission gates, Static CMOS design, dynamic CMOS design.

UNIT IV: CIRCUIT CHARACTERISATION AND PERFORMANCE ESTIMATION 9
Resistance estimation, Capacitance estimation, Inductance, switching characteristics, transistor sizing, power dissipation and design margining. Charge sharing .Scaling.

UNIT V:VLSI SYSTEM COMPONENTS CIRCUITS AND SYSTEM LEVEL PHYSICAL DESIGN 9
Multiplexers, Decoders, comparators, priority encoders, Shift registers. Arithmetic circuits – Ripple carry adders, Carry look ahead adders, High-speed adders, Multipliers. Physical design – Delay modeling, cross talk, floor planning, power distribution. Clock distribution. Basics of CMOS testing.

TOTAL: 45 Hours

REFERENCE BOOKS:

Sl.No	Author(s)	Title of the Book	Publisher	Year of Publication
1.	Neil H.E. Weste and Kamran Eshraghian	Principles of CMOS VLSI Design	Pearson Education ASIA, 2nd edition	2000
2.	John P.Uyemura	Introduction to VLSI Circuits and Systems	John Wiley & Sons, Inc.	2002
3.	Eugene D.Fabricius	Introduction to VLSI Design	McGraw Hill International Editions	1990

| 4. | Pucknell | Basic VLSI Design | Prentice Hall of India Publication | 1995 |
| 5. | Wayne Wolf | Modern VLSI Design System on chip | Pearson Education | 2002 |

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19VLB03	ANALOG VLSI CIRCUIT DESIGN	L T P C
		3 0 0 3

COURSE OBJECTIVES:

- To study the concepts of CMOS and BICMOS analog circuits.
- To understand the concepts of A/D convertors and analog integrated sensors.
- To understand the testing concepts in analog VLSI circuits and its statistical modeling.
- To understand the concepts of VLSI interconnects.
- To impart in-depth knowledge about switched capacitors, ADCs and DACs.
- To study the concepts of sampled-data analog filters

COURSE OUTCOMES:

- To be able to know the concepts of CMOS and BICMOS analog circuits.
- To be able to understand the concepts of A/D convertors and analog integrated sensors.
- To be able to understand the testing concepts in analog VLSI circuits and its statistical modeling.
- To be able to analyze VLSI interconnects.
- To be able to impart in-depth knowledge about switched capacitors, ADCs and DACs.
- To be able to know the concepts of sampled-data analog filters

UNIT I: BASIC CMOS CIRCUIT TECHNIQUES, CONTINUOUS TIME AND LOW VOLTAGE SIGNAL PROCESSING 9

Mixed-Signal VLSI Chips - Basic CMOS Circuits – Basic Gain Stage - Gain Boosting Techniques – Super MOS Transistor-Primitive Analog Cells-Linear Voltage-Current Converters –MOS Multipliers and Resistors-CMOS, Bipolar and Low-Voltage Bi CMOS Op-Amp Design-Instrumentation Amplifier Design-Low Voltage Filters.

UNIT II: BASIC BICMOS CIRCUIT TECHNIQUES, CURRENT -MODE SIGNAL PROCESSING AND NEURAL INFORMATION PROCESSING 9

Continuous-Time Signal Processing-Sampled-Data Signal Processing-Switched-Current Data Converters-Practical Considerations in SI Circuits Biologically-Inspired Neural Networks - Floating - Gate, Low-Power Neural Networks-CMOS Technology and Models-Design Methodology-Networks-Contrast Sensitive Silicon Retina.

UNIT III: SAMPLED-DATA ANALOG FILTERS, OVER SAMPLED A/D CONVERTERS AND ANALOG INTEGRATED SENSORS 9

First-order and Second SC Circuits-Bilinear Transformation - Cascade Design-Switched-Capacitor Ladder Filter-Synthesis of Switched-Current Filter- Nyquist rate A/D Converters-Modulators for Over sampled A/D Conversion-First and Second Order and Multibit Sigma-Delta Modulators-Interpolative Modulators –Cascaded Architecture-Decimation Filters ,mechanical,Thermal, Humidity and Magnetic Sensors-Sensor Interfaces.

UNIT IV: DESIGN FOR TESTABILITY AND ANALOG VLSI INTERCONNECTS 9

Fault modeling and Simulation - Testability-Analysis Technique-Ad Hoc Methods and General Guidelines-Scan Techniques-Boundary Scan-Built-in Self Test-Analog Test Buses- Design for Electron -Beam Testability-Physics of Interconnects in VLSI-Scaling of Interconnects-A Model for Estimating Wiring Density-A Configurable Architecture for Prototyping Analog Circuits.

UNIT V: STATISTICAL MODELING AND SIMULATION 9

Review of Statistical Concepts - Statistical Device Modeling- Statistical Circuit Simulation- Automation Analog Circuit Design-automatic Analog Layout-CMOS Transistor Layout- Resistor Layout-Capacitor Layout-Analog Cell Layout-Mixed Analog -Digital Layout.

TOTAL: 45 Hours

REFERENCE BOOKS:

Sl.No	Author(s)	Title of the Book	Publisher	Year of Publication

1.	Mohammed Ismail, Terri Fief	Analog VLSI signal and Information Processing	McGraw- Hill	1994
2.	Malcom R.Haskard, Lan C.May	Analog VLSI Design - NMOS and CMOS	Prentice Hall	1998
3.	Randall L Geiger. Phillip E. Allen Noel K.Strader	VLSI Design Techniques for Analog and Digital Circuits	Mc Graw Hill	1990
4.	Jose E.France, Yannis Tsividis	Design of Analog-Digital VLSI Circuits for Telecommunication and signal Processing	Prentice Hall	1994
5.	Philip Allen & D.Holberg	CMOS Analog Circuit Design	Oxford University Press	2002

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4. www.youtube.com/watch?v=4It_j_Y944o
5. www.youtube.com/watch?v=jC0wMOehKqU

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19VLB04	SOLID STATE DEVICE MODELING AND SIMULATION	L T P C
		3 0 0 3

COURSE OBJECTIVES:

- To know the basic semiconductor physics
- To understand the basic concepts bipolar device modeling
- To know the operation of MOSFET modeling.
- To understand the Operation parameter measurement.
- To study the functions characteristics of optoelectronic device modeling
- To study the various parameter measurements

COURSE OUTCOMES:

- Able to know the fundamentals of semiconductor physics.
- Understand BJT modeling.
- Understand and design MOSFET modeling.
- Analyze optoelectronic device modeling methods
- Able to study the functions characteristics of optoelectronic device modeling
- Able to understand various parameter measurements

UNIT I: SEMICONDUCTOR PHYSICS 9

Quantum Mechanical Concepts, Carrier Concentration, Transport Equation, Band gap, Mobility and Resistivity, Carrier Generation and Recombination, Avalanche Process, Noise Sources-Diodes : Forward and Reverse biased junctions –Reverse bias breakdown – Transient and AC conditions -Static and Dynamic behavior-Small and Large signal models –SPICE model for a Diode –Temperature and Area effects on Diode Model Parameters.

UNIT II:BIPOLAR DEVICE MODELING 9

Transistor Models: BJT –Transistor Action –Minority carrier distribution and Terminal currents - Switching-Eber -Molls and Gummel Poon Model, SPICE modeling -temperature and area effects.

UNIT III:MOSFET MODELING 9

OS Transistor –NMOS, PMOS –MOS Device equations -Threshold Voltage –Second order effects -Temperature Short Channel and Narrow Width Effect, Models for Enhancement, Depletion Type MOSFET, CMOS Models in SPICE.

UNIT IV: PARAMETER MEASUREMENT 9

Bipolar Junction Transistor Parameter –Static Parameter Measurement Techniques – Large signal parameter Measurement Techniques, Gummel Plots, MOSFET: Long and Short Channel Parameters, Measurement of Capacitance.

UNIT V: OPTOELECTRONIC DEVICE MODELING 9

Static and Dynamic Models, Rate Equations, Numerical Technique, Equivalent Circuits, Modeling of LEDs, Laser Diode and Photo detectors.

TOTAL: 45 Hours

REFERENCE BOOKS:

Sl.No	Author(s)	Title of the Book	Publisher	Year of Publication
1.	Ben.G.Streetman	Solid State Devices	Prentice Hall	1997
2.	Giuseppe Massobrio and Paolo Antogentti	Semiconductor Device Modeling with SPICE, Second Edition,	McGraw-Hill Inc, New York	1993
3.	Mohammed Ismail & Terri Fiez	Analog VLSI-Signal & Information Processing 1st Edition	Tata McGraw Hill Publishing Company Ltd	2001

| 4. | Roulston E.J., | Bipolar Semiconductor Devices | Mc-Graw Hill | 1990 |
| 5. | Tor.A.Fijedly | Introduction to Device Modelling and Circuit Simulation | Wiley-interscience | 1997 |

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19VLB05	ASIC DESIGN	L T P C
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COURSE OBJECTIVES:
- To acquire knowledge about various logics of ASICS and CMOS.
- To acquire knowledge about different types of ASICs design.
- To study about various types of Programmable ASICs architectures
- To study about various types of Programmable ASICs interconnects.
- To comprehend the low power design techniques and methodologies.
- To understand the floor planning, placement and routing

COURSE OUTCOMES:
- Analysis the different types of ASICs design.
- Analysis the different Logic cell architecture and interconnects.
- Analysis about different programmable ASIC design software.
- Identification of new developments in SOC
- Identification of developments in low power design.
- To analyze the Flash architecture, Pipelined Architecture

UNIT I: INTRODUCTION TO ASICS, CMOS LOGIC, ASIC LIBRARY DESIGN   9
Types of ASICs - Design flow –CMOS transistors-CMOS Design rules –Combinational logic Cell Sequential logic cell -Transistor as Resistors -Transistor parasitic capacitance –Logical effort -Library cell design –Library architecture-gate array design-standard cell design-data path cell design.

UNIT II : PROGRAMMABLE ASICS, PROGRAMMABLE ASIC LOGIC CELLS AND PROGRAMMABLE ASIC I/O CELLS   9
Anti fuse -Static RAM -EPROM and EEPROM technology -PREP benchmarks -Actel ACT -Xilinx LCA –Altera FLEX -Altera MAX-DC & AC inputs and outputs –clock input-power input -Xilinx I/O blocks.

UNIT III: PROGRAMMABLE ASIC INTERCONNECT, PROGRAMMABLE ASIC DESIGN SOFTWARE AND LOW LEVEL DESIGN ENTRY   9
Actel ACT -Xilinx LCA -Xilinx EPLD -Altera MAX 5000 and 7000 -Altera MAX 9000 -Altera FLEX –Design systems -Logic Synthesis -Half gate ASIC -Low level design language -PLA tools EDIF-CFI design representation.

UNIT IV :ASIC CONSTRUCTION   9
Performance metric, Flash architecture, Pipelined Architecture, Successive approximation architecture, Time interleaved architecture.

UNIT V: FLOOR PLANNING, PLACEMENT AND ROUTING   9
Floor planning –placement-physical design flow-information formats-Routing-Global routing, detailed routing, special routing, circuit extraction and DRC.

TOTAL: 45 Hours

REFERENCE BOOKS:

Sl.No	Author(s)	Title of the Book	Publisher	Year of Publication
1.	M.J.S. Smith	Application Specific Integrated Circuits	Pearson Education	2008
2.	Farzad Nekoogar and Faranak Nekoogar	From ASICs to SOCs: A Practical Approach	Prentice Hall PTR	2003
3.	Wayne Wolf	FPGA - Based System Design	Prentice Hall PTR	2009
4.	Wai-Kai Chen	Memory, Microprocessor, and ASIC	Prentice Hall	2006
5.	Khosrow Golshan	Physical Design Essentials: An Asic Design Implementation Perspective	Prentice Hall	2007

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5. nptel.ac.in/video.php?subjectId=117106092

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19VLB06	DIGITAL CMOS VLSI DESIGN	L T P C
		3 0 0 3

COURSE OBJECTIVES:

- To deal comprehensively with all aspects of transistor level design of all the digital building blocks
- To focus on the transistor level design
- To address all important issues related to size, speed and power consumption.
- To deal with the memory architectures
- To know the interconnect and clocking strategies.
- To understand the design of combinational and sequential CMOS circuits

COURSE OUTCOMES:

- Able to carry out transistor level hand calculation
- Able to design most important building blocks used in digital CMOS VLSI circuits.
- Able to develop strong understanding of the design methodology
- Able to develop tradeoffs of the various circuit choices for each of all the blocks discussed.
- Able to know the interconnect and clocking strategies.
- Able to design combinational and sequential CMOS circuits

UNIT I: MOS TRANSISTOR PRINCIPLES AND CMOS INVERTER   9

MOS(FET) Transistor Characteristic under Static and Dynamic Conditions, (Add)MOS device Design equation, MOS Transistor Secondary Effects, Process Variations, Technology Scaling, CMOS Inverter - Static Characteristic, Dynamic Characteristic, Power, Energy, and Energy Delay parameters,(Add) Tristate inverters.

UNIT II:COMBINATIONAL LOGIC CIRCUITS   9

Propagation Delays, Stick diagram, Layout diagrams, Examples of combinational logic design, Elmore's constant, Dynamic Logic Gates, Pass Transistor Logic, Power Dissipation, Low Power Design principles.

UNIT III:SEQUENTIAL LOGIC CIRCUITS   9

Static Latches and Registers, Dynamic Latches and Registers, Timing Issues, Pipelines, Pulse and sense amplifier based Registers, Nonbistable Sequential Circuits.

UNIT IV:ARITHMETIC BUILDING BLOCKS AND MEMORY ARCHITECTURES   9

Data path circuits, Architectures for Adders, Accumulators, Multipliers, Barrel Shifters, Speed and Area Tradeoffs, Memory Architectures, and Memory control circuits.

**UNIT V:INTERCONNECT AND CLOCKING STRATEGIES**   9

Interconnect Parameters – Capacitance, Resistance, and Inductance, Electrical Wire Models, Timing classification of Digital Systems, Synchronous Design, Self-Timed Circuit Design.

TOTAL: 45 Hours

REFERENCE BOOKS:

Sl.No	Author(s)	Title of the Book	Publisher	Year of Publication
1.	Jan Rabaey, Anantha Chandrakasan, B Nikolic	Digital Integrated Circuits: A Design Perspective	Prentice Hall of India.	2003
2	N.Weste, K. Eshraghian,	Principles of CMOS VLSI Design	Addision Wesley	1993
3.	M J Smith	Application Specific Integrated Circuits	Addisson Wesley	1997
4.	David A. Hodges, HoraceG. Jackson, and Resve A. Saleh	Analysis and Design of Digital Integrated Circuits	McGraw-Hill	2004
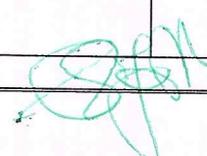
| 5. | Ken Martin | Digital Integrated Circuit Design | Oxford University Press | 2000 |

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19VLB07	CAD FOR VLSI CIRCUITS	L T P C
		3 2 0 4

COURSE OBJECTIVES:

- To introduce the basic CAD algorithm
- To understand the Partitioning
- To study about Placement, Floor Planning
- To learn about Global, Detail routing
- To know the Modeling and synthesis in CAD flow.
- To understand the High level transformations

COURSE OUTCOMES:

- Learn the Fundamentals of basic algorithm in CAD.
- Study the different partitioning algorithm.
- Understand the floor planning and placement algorithm.
- Learn about different routing algorithms.
- Know about modeling and synthesis techniques of CAD.
- Able to analyze the local routing problems

UNIT I: VLSI DESIGN METHODOLOGIES   9

Introduction to VLSI Design methodologies - Review of Data structures and algorithms - Review of VLSI Design automation tools - Algorithmic Graph Theory and Computational Complexity - Tractable and Intractable problems – general purpose methods for combinatorial optimization.

UNIT II:DESIGN RULES   9

Layout Compaction - Design rules - problem formulation - algorithms for constraint graph compaction - placement and partitioning - Circuit representation – Placement algorithms – partitioning.

UNIT III:FLOOR PLANNING   9

Floor planning concepts - shape functions and floor plan sizing - Types of local routing problems - Area routing - channel routing - global routing - algorithms for global routing.

UNIT IV:SIMULATION   9

Simulation - Gate-level modeling and simulation - Switch-level modeling and simulation - Combinational Logic Synthesis - Binary Decision Diagrams – Two Level Logic Synthesis.

UNIT V:MODELLING AND SYNTHESIS   9

High level Synthesis - Hardware models - Internal representation - Allocation - assignment and scheduling - Simple scheduling algorithm – Assignment problem - High level transformations.

TOTAL: 45 Hours

REFERENCE BOOKS:

Sl.No	Author(s)	Title of the Book	Publisher	Year of Publication
1.	S.H. Gerez	Algorithms for VLSI Design Automation	John Wiley & Sons	2002
2.	N.A. Sherwani	Algorithms for VLSI Physical Design Automation	Kluwer Academic Publishers	2002
3.	Giovanni De Micheli	Synthesis and Optimization of Digital Circuits	Tata McGraw Hill	1994
4.	M. Sarrafzadeh and C.K. Wong	An Introduction to VLSI Physical Design	McGraw Hill	1996

| 5. | Samir Palnitkar | Verilog HDL | Sun Microsystems Press A Prentice Hall Title | 2001 |

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19VLB08	LOW POWER VLSI DESIGN	L T P C
		3 0 0 3

COURSE OBJECTIVES:

- To understand different sources of power dissipation in CMOS & MIS structure.
- To understand the different types of low power adders and multipliers
- To focus on synthesis of different level low power transforms.
- To gain knowledge on low power static RAM architecture & the source of power dissipation in SRAM
- To understand the various energy recovery techniques used in low power design
- To understand the Special techniques of low power VLSI design

COURSE OUTCOMES:

- An ability to analyze different source of power dissipation and the factors involved in.
- Able to understand the different techniques involved in low power adders and multipliers
- Understandings of the impact of various low power transform
- An ability to identify and analyze the different techniques involved in low power SRAM.
- Able to understand various energy recovery techniques.
- Able to analyze the adders and multipliers

UNIT I: POWER DISSIPATION   9
Hierarchy of limits of power – Sources of power consumption – Physics of power dissipation in CMOS FET devices – Basic principle of low power design. (Add) Power dissipation in Domino CMOS- Low power VLSI design limits.

UNIT II:POWER OPTIMIZATION   9
Logic level power optimization – Circuit level low power design – circuit techniques for reducing power consumption in adders and multipliers.

UNIT III:DESIGN OF LOW POWER CIRCUITS   9
Computer arithmetic techniques for low power system – reducing power consumption in memories – low power clock, Inter connect and layout design – Advanced techniques –Special techniques.

UNIT IV:POWER ESTIMATION   9
Power Estimation technique – logic power estimation – Simulation power analysis –Probabilistic power analysis, (Add) Modeling of signals- Signal probability calculation.

UNIT V: SYNTHESIS AND SOFTWARE DESIGN   9
Synthesis for low power – Behavioral level transform – software design for low power overlap and digital correction.

TOTAL: 45 Hours

REFERENCE BOOKS:

Sl.No	Author(s)	Title of the Book	Publisher	Year of Publication
1.	Kaushik Roy and S.C.Prasad	Low power CMOS VLSI circuit design	Wiley	2000
2.	Dimitrios Soudris, Christians Pignet, Costas Goutis	Designing CMOS Circuits for Low Power	Kluwer	2002
3.	J.B.Kulo and J.H Lou	J.B.Kulo and J.H Lou	Wiley	1999
4.	A.P.Chandrasekaran and R.W.Broadersen	Low power digital CMOS design	Kluwer	1995

5.	Gary Yeap	Practical low power digital VLSI design	Kluwer	1998

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19VLB09	TESTING OF VLSI CIRCUITS	L T P C
		3 0 0 3

COURSE OBJECTIVES:

- To study basics of testing and fault modeling
- To gain knowledge on digital testing as applied to VLSI design.
- To acquire knowledge on testing of algorithms for digital circuits
- To learn the concept of memory, delay fault and IDDQ testing
- To learn various testing methods for digital circuits.
- To understand the BIST architectures

COURSE OUTCOMES:

- To ensure that, before fabrication, the circuit behavior satisfies the intent of the designer.
- To detect faulty devices, after fabrication
- To know about testing algorithm for digital circuits
- To Implement the concept of memory, delay fault in circuits
- To ensure that, implement the various testing methods for digital circuits.
- Able to Analyze the Self test

UNIT I: BASICS OF TESTING AND FAULT MODELING   9
Introduction- Principle of testing - types of testing - DC and AC parametric tests - fault modeling Stuck-at fault - fault equivalence - fault collapsing - fault dominance - fault simulation.

UNIT II: TESTING AND TEST ABILITY OF COMBINATIONAL CIRCUITS   9
Test generation basics - test generation algorithms - path sensitization - Boolean difference – D-algorithm – PODEM - Testable combinational logic circuit design.

UNIT III: TESTING AND TESTABILITY OF SEQUENTIAL CIRCUITS   9
Testing of sequential circuits as iterative combinational circuits - state table verification - test generation based on circuit structure - Design of testable sequential circuits - Ad Hoc design rules - scan path technique (scan design) - partial scan - Boundary scan.

UNIT IV: MEMORY, DELAY FAULT AND IDDQ TESTING   9
Testable memory design - RAM fault models - test algorithms for RAMs – Delay faults - Delay test- IDDQ testing - testing methods - limitations of IDDQ testing.

UNIT V: BUILT-IN SELF-TEST   9
Test pattern generation of Built-in Self-Test (BIST) - Output response analysis - BIST architectures.

TOTAL: 45 Hours

REFERENCE BOOKS:

Sl.No	Author(s)	Title of the Book	Publisher	Year of Publication
1.	P. K. Lala	Digital Circuit Testing and Testability	Academic Press	2002
2.	M.L. Bushnell and V.D. Agrawal	Essentials of Electronic Testing for Digital, Memory and Mixed-Signal VLSI Circuits	Kluwar Academic Publishers	2004
3.	N.K. Jha and S.G. Gupta	Testing of Digital Systems	Cambridge University Press	2003
4.	Zainalabe Navabi	Digital System Test and Testable Design: Using HDL Models and	Springer	2010

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5.	M. Abramovici, M.A.Breuer and A.D. Friedman	Digital Systems and Testable Design	Jaico Publishing House	2002

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19VLB010	MIXED SIGNAL VLSI DESIGN	L T P C
		3 0 0 3

COURSE OBJECTIVES:

- To understand the types of filters.
- To understand the different techniques of ADC
- To understand the different techniques of DAC
- To understand the different techniques of VHDL
- To understand the different techniques of Verilog
- To understand the Multi -disciplinary model

COURSE OUTCOMES:

- Analyze the types of filters.
- The ability to use DAC techniques for data conversions.
- The ability to use ADC techniques for data conversions.
- The ability to VHDL program , Mixed Signal VLSI Circuits
- Able to Verilog program, Mixed Signal VLSI Circuits
- Able to analyze the waveform Filter functions

UNIT I: INTRODUCTION TO ACTIVE FILTERS (PLL) & SWITCHED CAPACITOR FILTERS   9

Active RC Filters for monolithic filer design: First & Second order filter realizations – universal active filter (KHN) - self tuned filter - programmable filters- Switched capacitor filters: Switched capacitor resistors - amplifiers – comparators - sample & hold circuits – Integrator- Biquad.

UNIT II: CONTINUOUS TIME FILTERS & DIGITAL FILTERS   9

Introduction to Gm - C filters - bipolar trans conductors - CMOS Trans conductors using Triode transistors, active transistors – BiCMOS trans conductors –MOSFET C Filters- Tuning Circuitry -Dynamic range performance - Digital Filters: Sampling–decimation– interpolation – implementation of FIR and IIR filters.

UNIT III: DIGITAL TO ANALOG & ANALOG TO DIGITAL CONVERTERS   9

Non-idealities in the DAC - Types of DAC's: Current switched, Resistive, Charge redistribution (capacitive), Hybrid, segmented DAC's - Techniques for improving linearity - Analog to Digital Converters: quantization errors - non-idealities - types of ADC's: Flash, two step, pipelined, successive approximation, folding ADC's. Sigma Delta Converters: Over sampled converters - over sampling without noise & with noise - implementation imperfections - first order modulator - decimation filters - second order modulator - sigma delta DAC & ADC's

UNIT IV: ANALOG AND MIXED SIGNAL EXTENSIONS TO VHDL   9

Introduction - Language design Course Objectives - Theory of differential algebraic equations -- the 1076 .1 Language - Tolerance groups - Conservative systems - Time and the simulation cycle - A/D and D/A Interaction - Quiescent Point - Frequency domain modeling and examples.

UNIT V: ANALOG EXTENSIONS TO VERILOG   9

Introduction –data types –Expressions-Signals-Analog Behavior-Hierarchical structures-Mixed Signal Interaction. Introduction - Equation construction - solution - waveform Filter functions - simulator - Control Analysis - Multi -disciplinary model.

TOTAL: 45 Hours
REFERENCE BOOKS:

Sl.No	Author(s)	Title of the Book	Publisher	Year of Publication
1.	David A. Johns, Ken Martin	Analog Integrated Circuit Design	John Wiley & Sons	2002
2.	Rudy van de Plassche	Integrated Analog-to-Digital and Digital-to-Analog Converters	Kluwer	1999

3.	Antoniou	Digital Filters Analysis and Design	Tata McGraw Hill	1998
4.	Phillip Allen and Douglas Holmberg	CMOS Analog Circuit Design	Oxford University. Press	2000
5.	BenhardRazavi,	Data Converters	Kluwer Publishers	1999

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4. http:// nptel.ac.in/courses/117108038/38
5. http:// nptel.ac.in/courses/117101106/

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19VLB11 ELECTROMAGNETIC INTERFERENCE AND COMPATIBILITY

L	T	P	C
3	0	0	3

COURSE OBJECTIVES:
- To understand the concepts related to Electromagnetic interference in PCBs learn RF design and circuit board components
- To provide solutions for minimizing EMI in PCBs
- To learn EMI standards in the design of PCBs
- To learn various EMI coupling principles, EMI standards and measurements
- To provide knowledge on EMI control techniques and design procedures to make EMI Compatible PCBs
- Understand the Transient Suppressors

COURSE OUTCOMES:
- Analyze Electromagnetic interference effects in PCBs
- Propose solutions for minimizing EMI in PCBs
- Analyze Electromagnetic environment, EMI coupling
- Able to understand the EMI standards and measurement
- Able to design a EMI Control techniques
- Able to Analyze the Motherboard Design

UNIT I: EMI ENVIRONMENT   9
EMI/EMC concepts and definitions, Sources of EMI, conducted and radiated EMI, Transient EMI, Time domain Vs Frequency domain EMI, Units of measurement parameters, Emission and immunity concepts, ESD.

UNIT II:EMI COUPLING PRINCIPLES   9
Conducted, Radiated and Transient Coupling, Common Impedance Ground Coupling, Radiated Common Mode and Ground Loop Coupling, Radiated Differential Mode Coupling, Near Field Cable to Cable Coupling, Power Mains and Power Supply coupling.

UNIT III:EMI/EMC STANDARDS AND MEASUREMENTS   9
Civilian standards - FCC,CISPR,IEC, EN, Military standards - MIL STD 461D/462, EMI Test Instruments Systems, EMI Shielded Chamber, Open Area Test Site, TEM Cell, Sensors/Injectors/Couplers, Test beds for ESD and EFT, Military Test Method and Procedures.

UNIT IV:EMI CONTROL TECHNIQUES   9
Shielding, Filtering, Grounding, Bonding, Isolation Transformer, Transient Suppressors, Cable Routing, Signal Control, Component Selection and Mounting.

UNIT V :EMC DESIGN OF PCBs   9
PCB Traces Cross Talk, Impedance Control, Power Distribution Decoupling, Zoning, Motherboard Designs and Propagation Delay Performance Models.

TOTAL: 45 Hours

TEXT BOOKS:

Sl.No	Author(s)	Title of the Book	Publisher	Year of Publication
1.	Clayton Paul	Introduction to Electromagnetic Compatibility	Wiley Interscience	2006
2.	Henry W.Ott	Noise Reduction Techniques in Electronic Systems	John Wiley and Sons,NewYork	1988.
3.	V.P.Kodali	Engineering EMC Principles, Measurements and Technologies	IEEE Press, Newyork	2001
4.	Dr Kenneth L Kaiser	The Electromagnetic Compatibility Handbook	CRC Press	2005
5.	Henry W. Ott,	Electromagnetic Compatibility Engineering	John Wiley & Sons	2009

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2.studyvlsidesign.blogspot.com/2014/10/electromagnetic-interference-and.html

3.shodhganga.inflibnet.ac.in/bitstream/10603/28123/10/11_chapter6.pdf

4.https://www.youtube.com/watch?v=krk4_89em48

5.https://www.svce.ac.in/departments/ece/archives/.../EMI%20EMC%20pt%204.ppt

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19VLB12	ADVANCED MOSFET MODELING ALGORITHMS	L T P C
		3 0 0 3

COURSE OBJECTIVES:

- To understand basic device physics
- To understand MOSFET devices
- To understand nano scaled MOSFETS
- To understand noise modeling and process variation
- To understand compact models for circuit simulators
- To understand the BSIM model

COURSE OUTCOMES:

- Able to understand basic device physics
- Able to understand MOSFET devices
- Able to understand nano scaled MOSFETS
- Able to understand noise modeling and process variation
- Able to understand compact models for circuit simulators
- To analyze the Analog and RF application

UNIT I: BASIC DEVICE PHYSICS   9
Intrinsic and extrinsic semiconductors, direct and indirect semiconductors- Electrons and holes in silicon energy bands: electron and hole densities in equilibrium- Fermi Dirac statistics, carrier concentration, ionization of impurities. Carrier transport in silicon: drift current, diffusion current. pn junctions built in potential, electric field, current voltage characteristics.

UNIT II: MOSFET DEVICES   9
MOS capacitors surface potential- structure characteristics, electrostatic potential and charge distribution- threshold voltage- polysilicon work function- interface states and oxide traps. Long channel MOSFETs : threshold voltage, substrate bias and temperature dependence of threshold voltage, drain current model, subthreshold characteristics, channel mobility, capacitances.

UNIT III: NANO SCALED MOSFETs   9
 Scaling of MOSFETs: Short channel MOSFETs – short channel effects, velocity saturation, channel length modulation, DIBL, GIDL. Variability in MOSFETs. Reliability of MOSFETs high field effects, hot carrier degradation, negative bias temperature instability, MOSFET breakdown, high k dielectrics. Non classical MOSFETs : SOI MOSFETs Current voltage equations, fully depleted SOI MOSFETs, partially depleted SOI MOSFETs, Hetero structure MOSFETs, strained channel MOSFETs, Power MOSFETs,SiC MOSFETs- Silicon Nano wires-Carbon Nano tubes.

UNIT IV: NOISE MODELING AND PROCESS VARIATION   9
Noise sources in MOSFET: Flicker noise modeling, Thermal noise modeling- model for accurate distortion analysis- nonlinearities in CMOS devices and modeling- calculation of distortion in analog CMOS circuits. Influence of process variation- modeling of device mismatch for Analog/RF Applications- Benchmark circuits for quality assurance Automation of the tests.

UNIT V: COMPACT MODELS FOR CIRCUIT SIMULATORS   9
Introduction to compact models, SPICE Level 1, 2 and 3 MOS models. BSIM model, EKV model, High frequency models- Parameter extraction of MOSFETs.

TOTAL: 45 Hours

REFERENCE BOOKS:

Sl.No	Author(s)	Title of the Book	Publisher	Year of Publication
1.	Taur and T. H. Ning	Fundamentals of Modern VLSI Devices	Cambridge University Press, Cambridge, United Kingdom	1998

2.	TrondYtterdal, Yuhua Cheng and Tor A. FjeldlyWayne Wolf	Device Modeling for Analog and RF CMOS Circuit Design	John Wiley & Sons Ltd	2003
3.	N. DasGupta and A. DasGupta	Semiconductor Devices – Modeling and Technology	Prentice Hall of India Pvt. Ltd, New Delhi, India	2004
4.	A. B. Bhattacharyya	Compact MOSFET Models for VLSI Design	John Wiley & Sons Inc.	2009
5.	WeidongLiuandChemmingHu	BSIM 4 and MOSFET Modeling for IC simulation	World scientific and Publishing Co. Pte. Ltd	2011

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1. www.fairchildsemi.com/products/discretes/fets/
2. www.mosis.com/pages/Technical/Testdata/submicron-spiceparameters
3. en.wikipedia.org/wiki/Carbon_nanotube
4. www.nxp.com/wcm_documents/models/mos-models/model- 9/aacd96_sel
5. web.cs.mun.ca/~paul/transistors/node3.html

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19VLB13	VLSI DESIGN TECHNIQUES LABORATORY	L T P C
		0 0 2 1

List of Experiments:

1. Design and simulation of combinational circuits using HDL.
2. Design and simulation of Sequential circuits using HDL.
3. Writing Test benches using VHDL/ Verilog.
4. Design and simulation of 8-Bit shift register using HDL.
5. Design and simulation of 4-bit carry save adder, Ripple carry adder using HDL.
6. Design and simulation of 8-bit adder / subtractor using HDL.
7. Design and simulation of Multiplier using HDL
8. Design and simulation of FSM using HDL.
9. **Design and Implementation of Traffic Light Controller using VHDL.**

19VLB14	DIGITAL CMOS VLSI DESIGN LABORATORY	L T P C
		0 0 2 1

List of Experiments:

1. Design and simulate frequency response and noise analysis of any followers
2. Design and simulate operational amplifier performance parameters One stage Op Amps, Two stage Op Amps
3. Design and simulate cascode current mirrors and active current mirrors
4. Design of various routing – local routing, Area routing, Channel routing and global routing.
5. Design and simulation of Gate-level modeling
6. Design and simulation of Switch-level modeling
7. Modeling and synthesis of simple scheduling algorithm
8. Design and implement reducing power consumption in memories
9. Design and simulation of Power Estimation

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PROFESSIONAL ELECTIVE (PE)

19VLC01	SIGNAL INTEGRITY FOR HIGH SPEED DEVICES	L T P C
		3 0 0 3

COURSE OBJECTIVES:

- To learn the fundamental and importance of signal integrity.
- To analyze and minimize cross talk in unbounded conductive media.
- To study about differential signaling
- To study about the different types of Di-Electric materials.
- To learn about differential cross talk and CMOS based transmission line model
- To understand physical transmission line model

COURSE OUTCOMES:

- To learn the fundamental and importance of signal integrity.
- To analyze and minimize cross talk in unbounded conductive media.
- To study about the different types of Di-Electric materials.
- To study about differential signaling
- To learn about differential cross talk and CMOS based transmission line model
- Able to analyze the loosy dielectric and realistic conductors.

UNIT I: FUNDAMENTALS   9

The importance of signal integrity-new realm of bus design-Electromagnetic fundamentals for signal integrity-maxwell equations common vector operators-wave propagations-Electro statics magneto statics-Power flow and the poynting vector-Reflections of electromagnetic waves.

UNIT II :CROSS TALK   9

Introduction -mutual inductance and capacitance-coupled wave equation-coupled line analysis modal analysis-cross talk minimization signal propagation in unbounded conductive media-classic conductor model for transmission model.

UNIT III:DI-ELECTRIC MATERIALS   9

Polarization of Dielectric-Classification of Di electric material-frequency dependent di electric material- Classification of Di electric material fiber-Weave effect-Environmental variation in di electric behaviour Transmission line parameters for loosy dielectric and realistic conductors.

UNIT IV:DIFFERENTIAL SIGNALING   9

DC operating point and Load line-Q point-Bias Stability, Transistor biasing methods: Fixed bias-Collector to basebias-Self biasing, Bias compensation methods, Thermistor and sensistor compensation techniques, thermalrunaway ,thermal stability, FET biasing methods: Self bias-Source bias-Voltage divider bias-Biasing enhancement and depletion MOSFET.

UNIT V: PHYSICAL TRANSMISSION LINE MODEL   9

Introduction- non ideal return paths-Vias-IO design consideration-Push-pull transmitter-CMOS receivers-ESSD protection circuits-On chip Termination.

TOTAL: 45 Hours

REFERENCE BOOKS:

Sl.No	Author(s)	Title of the Book	Publisher	Year of Publication
1.	Stephen H. Hall, Howard L. Heck	Advanced Signal Integrity for High-Speed Digital Designs	Wiley	2009
2.	James Edgar Buchanan	Signal and power integrity in digital systems: TTL, CMOS, and BiCMOS	Hardcover	1996
3.	Hanqiao Zhang Steven , Krooswyk,Jeffrey Ou	High Speed Digital Design: Design of High Speed Interconnects and Signaling	MK	2015

4.	Stephen H. Hall Garrett W. Hall James A. McCall	High-Speed Digital System Design: A Handbook of Interconnect Theory and Design Practices	Kindly Edition	2000
5.	Eric Bogatin	Signal and Power Integrity - Simplified (Prentice Hall Modern Semiconductor Design Series)	Kindly Edition	Second Edition 2009

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4. nptel.ac.in/courses/108108031/module10/Lecture42.pdf
5. https://www.altera.com/content/dam/altera-www/global/en.../pdfs/.../wp_sgnlntgry.pdf

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19VLC02	ADVANCED DIGITAL SYSTEM DESIGN	L T P C
		3 0 0 3

COURSE OBJECTIVES:

- To understand the concepts of advanced Boolean algebra
- To understand the concepts of threshold logic
- To understand the concepts of symmetric functions
- To understand the concepts of sequential logic circuits.
- To study the concepts of Fault Diagnosis and Testability Algorithms.
- To understand the concept of test generation.

COURSE OUTCOMES:

- To apply knowledge of Boolean algebra to the analysis and design of digital logic circuits.
- To acquire the knowledge of threshold logic
- To acquire the knowledge of symmetric functions.
- To view advanced digital design from a hierarchical viewpoint.
- To acquire the knowledge of testability concepts.
- To analyze the Built-in Self Test.

UNIT I: ADVANCED TOPICS IN BOOLEAN ALGEBRA   9

Shannon's expansion theorem, Consensus theorem, Octal designation, Run measure, INHIBIT / INCLUSION / AOI / Driver / Buffer gates, Gate expander, Reed Muller expansion, Synthesis of multiple output combinational logic circuits by product map method, Design of static hazard free and dynamic hazard free logic circuits.

UNIT II: THRESHOLD LOGIC   9

Linear seperability, Unateness, Physical implementation, Dual comparability, Reduced functions, Various theorems in threshold logic, Synthesis of single gate and multigate threshold Network.

UNIT III: SYMMETRIC FUNCTIONS   9

Elementary symmetric functions, Partially symmetric and total ly symmetric functions, McCluskey decomposition method, Unity ratio symmetric ratio functions, Synthesis of symmetric function by contact networks.

UNIT IV: SEQUENTIAL LOGIC CIRCUITS   9

Mealy machine, Moore machine, Trivial / Reversible / Isomorphic sequential machines, State diagrams, State table minimization, Incompletely specified sequential machines, State assignments, Design of synchronous and asynchronous sequential logic circuits working in the fundamental mode and pulse mode, Essential hazards Unger's theorem.

UNIT V: FAULT DIAGNOSIS AND TESTABILITY ALGORITHMS   9

Fault Table Method –Path Sensitization Method –Boolean Difference Method –Kohavi Algorithm –Tolerance Techniques –The Compact Algorithm –Fault in PLA –Test Generation –Masking Cycle –Built-in Self Test.

TOTAL: 45 Hours

REFERENCE BOOKS:

Sl.No	Author(s)	Title of the Book	Publisher	Year of Publication
1.	Charles H.Roth Jr	Fundamentals of Logic Design	Thomson Learning	2004
2	Nripendra N Biswas	Logic Design Theory	Prentice Hall of India	2001
3	Parag K.Lala	Digital system Design using PLD	B S Publications	2003
4	Lucien Ngalamou	Advanced Digital Systems Design with Rapid Prototyping on FPGAs Using	Springer	2012

		VHDL		
5	Kuruvilla Varghese	Digital System Design with PLDs and FPGAs	Prentice Hall	2007

WEB URLs

1. nptel.ac.in/courses/117108040/downloads/Digital%20System%20Design.pdf
2. nptel.ac.in/video.php?subjectId=117105080
3. nptelvideos.in/2012/12/digital-systems-design.html
4. extofvideo.nptel.iitm.ac.in/117106092/lec1.pdf
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19VLC03	SUBMICRON VLSI DESIGN	L T P C
		3 0 0 3

COURSE OBJECTIVES:

- To introduce the concepts of Silicon realization of ASIC
- To introduce the concepts of CMOS devices at deep submicron level.
- To study and apply the deep submicron concepts to CMOS low power devices.
- To study and discuss about RF CMOS transistor sizing
- To study and discuss about RF CMOS transistor sizing limitations.
- To understand the scaling perspectives

COURSE OUTCOMES:

- Able to known the concepts of Silicon realization of ASIC
- Known the concepts of cmos devices at deep submicron level.
- Known the concepts to cmos low power devices.
- Importance of RF CMOS transistor sizing
- RF CMOS transistor sizing limitations.
- Able to analyze the package-Signal propagation

UNIT I: SILICON REALIZATION OF ASIC   9
Introduction-Handcrafted layout implementation-bit-slice layout implementation-Cell based layout implementation-gate array layout implementation - Hierchial design approach-The choice of layout implementation form

UNIT II: LOW POWER DESIGN   9
Sources of CMOS power consumption-technology options for low power-reduction of P-leak by technological measures Reduction of P-dyn by technology measures-reduction of P-dyn by reduced voltage process-design option for low power-computing power Vs chip power-scaling perspectives.

UNIT III : DESIGN FOR RELIABILITY   9
Introduction-latch up in CMOS circuits-Electrostatics discharge-and its protection-Electro migration-Hot carrier degradation design for signal integrity -clock distribution and critical timing issues-clock generation and synchronization in different domain on a chip-the influence of interconnection-design organization.

UNIT IV : DEEP SUB MICRON   9
RF CMOS Transistor downsizing limitations- RFbasic blocks layout implementation Submicron technology and layout dependent effects - input output interfacing, the bonding pad, the pad ring, electrostatic discharge prevention.

UNIT V :CMOS DEVICES   9
Clamp CMOS devices, zener diode-input structure-output structure-pull up-pull down-i/o pad, power clamp-core/pad limitation I/O Pad description using Ibis-Connecting to the package-Signal propagation between integrated circuits.

REFERENCE BOOKS: **TOTAL: 45 Hours**

Sl.No	Author(s)	Title of the Book	Publisher	Year of Publication
1.	Harry J. M. Veendrick	Deep-Submicron Cmos Ics: From Basics to Asics	Thomson Learning	2004
2.	W. Nebel, Jean P. Mermet	Low Power Design in Deep Submicron Electronics	Prentice Hall of India	2001
3.	P.R.Van Der Meer, Arie van Staveren,	Low-Power Deep Sub-Micron CMOS Logic: Sub-threshold Current Reduction	Prentice Hall of India	2003

	Arthur H. M. van Roermund			
4.	Philip E. Madrid	Device Design And Process Window Analysis Of A Deep Submicron CMOS VLSI Technology	Springer	2012
5.	Kuruvilla Varghese	Digital System Design with PLDs and FPGAs	Prentice Hall	2007

WEB URLs :

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2. nptel.ac.in/courses/117101058/downloads/Lec-12.pdf
3. nptel.ac.in/courses/117101105/1
4. nptel.ac.in/courses/117101105/2
5. youtube.com/watch?v=Q3WYZF5wzgU

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19VLC04	VLSI TECHNOLOGY	L P T C
		3 0 0 3

COURSE OBJECTIVES:

- To understand the Fabrication of ICs and purification of Silicon in different technologies.
- To impart in-depth knowledge about Etching and deposition of different layers.
- To understand the different packaging techniques of VLSI devices.
- To understand the fabrication technologies.
- To understand the integration techniques.
- To understand the MOS Memory IC technology

COURSE OUTCOMES:

- The ability to use metallization techniques to create three-dimensional device structures devices.
- The ability to know methodology to fabricate an IC's.
- The ability to observe the implementation techniques in chip designing.
- The ability to learn the application areas of VLSI technologies
- Able to understand the integration techniques.
- Able to analyze the MOS Memory IC technology

UNIT I: CRYSTAL GROWTH, WAFER PREPARATION, EPITAXY ANDOXIDATION   9
Electronic Grade Silicon, Czochralski crystal growing, Silicon Shaping, processing consideration,Vapor phase Epitaxy, Molecular Beam Epitaxy, Epitaxial Evaluation, Growth Mechanism andkinetics, Thin Oxides, Oxidation Techniques and Systems, Oxide properties, Redistribution ofDopants at interface, Oxidation of Poly Silicon, Oxidation induced Defects.

UNIT II:LITHOGRAPHY AND REACTIVE PLASMA ETCHING   9.
Optical Lithography, Electron Lithography, X-Ray Lithography, Ion Lithography, Nano imprint Lithography, Plasma properties, Feature Size control and Anisotropic Etch mechanism, reactive Plasma Etching techniques and Equipments.

UNIT III:DEPOSITION, DIFFUSION AND ION IMPLANTATION   9
Deposition process, Polysilicon, plasma assisted Deposition, Models of Diffusion in Solids, Fick'sone dimensional Diffusion Equation - Measurement techniques - Range theory- Implant equipment –Annealing- Shallow junction, High - energy implantation.

UNIT IV : METALLIZATION AND VLSI PROCESS INTEGRATION   9
Physical Vapour Deposition (PVD) –Patterning- NMOS IC Technology – CMOS IC Technology –BICMOS IC Technology- MOS Memory IC technology - Bipolar IC Technology –Silicon on Insulator Technology–Noise in VLSI Technologies

UNIT V:ANALYTICAL, ASSEMBLY TECHNIQUES AND PACKAGING OF VLSI DEVICES   9
Analytical Beams – Beams Specimen interactions - Chemical methods – Package types – packaging design consideration – VLSI assembly technology – Package fabrication technology. Scanning Probe Techniques-Analysis by diffraction and fluorescence methods

TOTAL: 45 Hours

REFERENCE BOOKS:

Sl.No	Author(s)	Title of the Book	Publisher	Year of Publication
1.	S.M .Sze	VLSI Technology	McGraw Hill	2003
2.	Amar Mukherjee	Introduction to N MOS and CMOS VLSI System Design	PHI	2000
3.	James D Plummer, Michael D. Deal and Peter B. Griffin	Silicon VLSI Technology: Fundamentals Practice and Modeling	PHI	2000
4.	Wai Kai Chen	VLSI Technology	CRC press	2003
5.	Rainer Waser	Nano Electronics and Information Technolgy	Wiley-IEEE Press	2004

WEB URLs :
1. www.google.co.in/search?site=&source=hp&q=S.M+.Sze%2C+VLSI+Technology
2. www.scribd.com/doc/124363987/VLSI-DESIGN-pdf
3. nptel.ac.in/courses/IIT-MADRAS/ Silicon VLSI Technology. pdf
4. nptel.ac.in/courses/111104027/
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19VLC05	DSP INTEGRATED CIRCUITS	L P T C
		3 0 0 3

COURSE OBJECTIVES:

- To study the procedural flow of system design in DSP and Integrated circuit.
- To design FIR and IIR filters for the given specifications.
- To study the architectures for DSP system.
- To learn the design layout for VLSI circuits.
- To understand the concept of DSP Processor Architecture and code optimization.
- To learn the applications of DSP Integrated circuits.

COURSE OUTCOMES:

- To design filter and analysis the concept of finite word length effects.
- To synthesis DSP Architecture and design integrated circuits.
- To learn DSP Processor Architecture.
- The ability to learn the optimization techniques.
- To understand the concept of DSP Processor Architecture and code optimization.
- To learn the applications of DSP Integrated circuits.

UNIT I: DSP SYSTEMS AND MOS TECHNOLOGIES 9

Standard digital signal processors –Application specific IC's for DSP –DSP systems –DSP system design –Integrated circuit design – MOS transistors- MOS logic - VLSI process technologies – Trends in CMOS technologies.

UNIT II:DIGITAL FILTERS AND FINITE WORD LENGTH EFFECTS 9

FIR filters: FIR filter structures, FIR chips - IIR filters structures- Real time filtering – Circular buffering- Adaptive filtering: LMS and RLS Algorithm –Multi-rate filters: Interpolation with an integer factor L, Sampling rate change with a ratio L/M Finite Word Length Effects: Parasitic oscillations - Scaling of signal levels - Round-off noise –Measuring round-off noise.

UNIT III:DSP ARCHITECTURES AND ITS SYNTHESIS 9

DSP system architectures - Standard DSP architecture - Ideal DSP architectures - Multiprocessors and multicomputer - Systolic and Wave front arrays - Shared memory architectures - Mapping of DSP algorithms onto hardware - Implementation based on complex PEs - Shared memory architecture with Bi-serial PEs.

UNITIV:ARITHMETIC UNITS AND INTEGRATED CIRCUIT DESIGN 9

Conventional number system - Redundant Number system - Residue Number System - Bit-parallel and Bit-Serial arithmetic - Basic shift accumulator - Reducing the memory size - Complex multipliers - Improved shift-accumulator - Layout of VLSI circuits - FFT processor - DCT processor and Interpolator as case studies - Cordic algorithm.

UNIT V: TMS320C6X, DSP56XXX PROCESSORS ARCHITECTURE AND CODE OPTIMIZATION 9

CPU Operation – Pipelined CPU- Velocity TI – C64XDSP- Software tools: EVM – DSK Target C6x board – Assembly file – Memory management- Compiler utility- Code initialization – Code composer studio – Interrupt data processing, Code Optimization: Word- wide optimization – Mixing C and assembly- Software pipelining – C64X improvements - Overview on Free scale DSP56XXX Core Architecture. Design of modulo multipliers using RNS-complex multipliers-accumulator.

TOTAL: 45 Hours

REFERENCE BOOKS:

Sl.No	Author(s)	Title of the Book	Publisher	Year of Publication
1.	Lars Wanhammer	DSP Integrated Circuits	Academic press, New York	1999
2	Nasser Kehtarnavaz	DSP System Design Using the TMS320C6000	Wiley Prentice Hall	2001
2	Richard G. Lyons	Understanding Digital Signal Processing 2004.	Prentice Hall	2010

4	John G. Proakis, Dimitris K. Manolakis	Digital Signal Processing: Principles, Algorithms, and Applications.	Kluwer Acedamic Publishers	2006.
5	Mohammed El-Sharkawy	Digital Signal Processing Applications with Motorola's DSP56002Processor,	Prentice Hall	2006

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1. www.annauniv.edu/academic_courses/WSA/.../07.%20VLSI%20Design.pdf
2. www.scribd.com/doc/310875222/1-Digital-Signal-Processing-Introduction
3. www.computer.org/csdl/trans/tc/1985/05/01976588-abs.html
4. www.bitsathy.ac.in/academics/pdf/syllabus/VLSI%20-%202015.pdf
5. nptel.ac.in/courses/IIT-MADRAS/ DSP Integrated Circuits /Pdfs/1_5.pdf

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19VLC06	ARM PROCESSOR AND ITS APPLICATIONS	L T P C
		3 0 0 3

COURSE OBJECTIVES:

- To study the concepts of Architecture and Assembly language programming of ARM Processor.
- To study the concepts of Architectural Support for High level language.
- To understand the memory hierarchy of processors.
- To study the concepts of Architectural support for system Development
- To understand the processors Operating system.
- To learn applications of ARM processor

COURSE OUTCOMES:

- Analysis the different types of Architectures.
- To learn about instruction Set for different architectures.
- To understand and analysis about the Assembly language Program for various industry based.
- The ability to observe the real time applications of operating system Development.
- The ability to observe the real time applications of operating system.
- Able To learn applications of ARM processor.

UNIT I: ARM ARCHITECTURE 9

Abstraction in hardware design – MUO -Acorn RISC Machine – Architecture Inheritance – ARM programming model – ARM Development Tools – 3 and 5 Stage Pipeline ARM Organization – ARM Instruction Execution and Implementation – ARM Co-Processor Interface.

UNIT II:ARM ASSEMBLY LANGUAGE PROGRAMMING 9

ARM Instruction Types – data Transfer, Data Processing and Control Flow Instructions – ARM Instruction set – Co-Processor Instruction.

UNIT III:ARCHITECTURAL SUPPORT FOR HIGH LEVEL LANGUAGE AND MEMORY HIERARCHY 9

Data Types – Abstraction in software design – expressions – Loops – Functions and Procedures –Conditional Statements – use of memory- Memory size and speed – On Chip Memory – Caches Design – an example –Memory management.

UNIT IV: ARCHITECTURAL SUPPORT FOR SYSTEM DEVELOPMENT 9

Physical Vapour Deposition (PVD) –Patterning- NMOS IC Advantaged Microcontroller Bus Architecture – ARM memory Interface – ARM Reference Peripheral Specification– Hardware System Prototyping Tools – Emulator – Debug Architecture

UNIT V:ARCHITECTURAL SUPPORT FOR OPERATING SYSTEM 9

An introduction to Operating systems – ARM system Control Coprocessor – CP15 Protection unit Registers – ARM Protection unit – CP15 MMU Registers – ARM MMU Architecture –Synchronization context Switching input and output. Design of various real time applications using ARM processor

TOTAL: 45 Hours

REFERENCE BOOKS:

Sl.No	Author(s)	Title of the Book	Publisher	Year of Publication
1.	Steve Furber	ARM System on Chip Architecture	Wesley Professional	2000
2	Ricardo Reis	Design of System on a Chip: Devices and Components	Springer	2004
3	Daniel Nenni, Don Dingee,	Mobile Unleashed: The Origin and Evolution of ARM Processors in our Devices	springer	2015
4	Joseph Yiu	The Definitive Guide to the Arm Cortex-M0	Newnes	2011

5	Jason Andrews	Verification of Hardware and Software for ARM System on Chip Design (Embedded Technology) BK and CD-ROM	PHI	2004

WEB URLs

1. www.researchgate.net/.../3282781_ARM_system-on-chip_architecture_2nd_ed
2. www.abebooks.com/9781441954541/Design-System-Chip-Devices-Components.../pl
3. www.pearsonhighered.com/samplechapter/0130338575.pdf
4. www.arm.com/products/processors/instruction-set-architectures/index.php
5. www.computer.org / definitive guide to the arm cortex.pdf

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		Verification of Hardware and Software for ARM System on Chip Design (Embedded Technology) BK and CD-ROM		

WEB URLs :

1. nptel.ac.in/courses/117106093/
2. www.iitb.ac.in/acadpublic/crsedetail.jsp?ccd=EE%20709
3. nptel.ac.in/courses/IIT-MADRAS/Levelsofverification/Pdfs/1_5.pdf
4. onlinecourses.nptel.ac.in/noc15_ec02
5. nptelvideos.in/2012/12/vlsi-design.html

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19VLC08	DESIGN AND ANALYSIS OF ALGORITHMS	L T P C
		3 0 0 3

COURSE OBJECTIVES:

- Learn algorithms for various computing problems
- Analyze the time and space complexity of algorithms.
- Learn the algorithm analysis techniques.
- Become familiar with the different algorithm design techniques.

COURSE OUTCOMES:
- Design algorithms for various computing problems
- Analyze the time and space complexity of algorithms.
- Critically analyze the different algorithm design techniques for a given problem.
- Modify existing algorithms to improve efficiency
- Implementation of coping with the limitations of algorithm power

UNIT I: INTRODUCTION 9

Notion of an Algorithm – Fundamentals of Algorithmic Problem Solving – Important Problem Types – Fundamentals of the Analysis of Algorithm Efficiency – Analysis Framework – Asymptotic Notations and its properties – Mathematical analysis for Recursive and Non-recursive algorithms.

UNIT II: BRUTE FORCE AND DIVIDE-AND-CONQUER 9

Brute Force – Closest-Pair and Convex-Hull Problems-Exhaustive Search – Traveling Salesman Problem – Knapsack Problem – Assignment problem. Divide and conquer methodology – Merge sort – Quick sort – Binary search – Multiplication of Large Integers – Strassen's Matrix Multiplication-Closest-Pair and Convex-Hull Problems.

UNIT III: DYNAMIC PROGRAMMING AND GREEDY TECHNIQUE 9

Computing a Binomial Coefficient – Warshall's and Floyd' algorithm – Optimal Binary Search Trees – Knapsack Problem and Memory functions. Greedy Technique– Prim's algorithm- Kruskal's Algorithm- Dijkstra's Algorithm-Huffman Trees

UNIT IV: ITERATIVE IMPROVEMENT 9

The Simplex Method-The Maximum-Flow Problem – Maximm Matching in Bipartite Graphs- The Stable marriage Problem.

UNIT V: COPING WITH THE LIMITATIONS OF ALGORITHM POWER 9

Limitations of Algorithm Power-Lower-Bound Arguments-Decision Trees-P, NP and NP-Complete Problems–Coping with the Limitations – Backtracking – n-Queens problem – Hamiltonian Circuit Problem – Subset Sum Problem-Branch and Bound – Assignment problem- Knapsack Problem – Traveling Salesman Problem- Approximation Algorithms for NP- Hard Problems-Traveling Salesman Problem- Knapsack problem.

TOTAL: 45 Hours

REFERENCE BOOKS:

Sl.No	Author(s)	Title of the Book	Publisher	Year of Publication
1.	Anany Levitin	Introduction to the Design and Analysis of Algorithms	Third Edition, Pearson Education	2012
2.	Thomas H.Cormen, Charles E.Leiserson, Ronald L. Rivest and Clifford Stein	Introduction to Algorithms	Third Edition, PHI Learning Private Limited	2012
3.	Alfred V. Aho, John E. Hopcroft and Jeffrey D. Ullman	Data Structures and Algorithms	Pearson Education	Reprint 2006

| 4. | Donald E. Knuth | The Art of Computer Programming | Volumes 1& 3 Pearson Education | 2009 |
| 5. | Steven S. Skiena | The Algorithm Design Manual | Springer | Second Edition, 2009 |

WEB URLs :

1. http://nptel.ac.in/courses/112106134/1
2. http://nptel.ac.in/courses/106101060
3. https://www.autonlab.org/tutorials/hillclimb02.pdf
4. https://www.autonlab.org/tutorials/hillclimb02.pdf
5. http:// cse.unl.edu/~ylu/raik283/notes/backup/ch12n.ppt

19VLC09	MEMS AND NEMS	L T P C
		3 0 0 3

COURSE OBJECTIVES:

- To introducing the concepts of micro electro mechanical devices.
- To know the fabrication process of Microsystems.
- To know the design concepts of micro sensors and micro actuators.
- To introducing concepts of quantum mechanics.
- To introducing concepts of nano systems.
- To learn applications of MEMs.

COURSE OUTCOMES:

- Able to introduce the concepts of micro electro mechanical devices.
- Able to know the fabrication process of Microsystems.
- Able to know the design concepts of micro sensors and micro actuators.
- Able to introducing concepts of quantum mechanics.
- Able to introducing concepts of nano systems.
- Able to learn applications of MEMs.

UNIT I: OVERVIEW AND INTRODUCTION 9
New trends in Engineering and Science: Micro and Nanoscale systems Introduction to Design of MEMS and NEMS, Overview of Nano and Microelectromechanical Systems, Applications of Micro and Nanoelectromechanical systems, Microelectromechanical systems, devices and structures Definitions, Materials for MEMS: Silicon, silicon compounds, polymers, metals.

UNIT II :MEMS FABRICATION TECHNOLOGIES 9
Microsystem fabrication processes: Photolithography, Ion Implantation, Diffusion, Oxidation.Thin film depositions: LPCVD, Sputtering, Evaporation, Electroplating; Etching techniques: Dry and wet etching, electrochemical etching; Micromachining: Bulk Micromachining, Surface Micromachining,High Aspect-Ratio (LIGA and LIGA-like) Technology; Packaging: Microsystems packaging, Essential packaging technologies, Selection of packaging materials.

UNIT III: MICRO SENSORS 9
MEMS Sensors: Design of Acoustic wave sensors, resonant sensor, Vibratory gyroscope, Capacitive and Piezo Resistive Pressure sensors- engineering mechanics behind these Microsensors. Case study: Piezo-resistive pressure sensor.

UNIT IV: MICRO ACTUATORS 9
Design of Actuators: Actuation using thermal forces, Actuation using shape memory Alloys, Actuation using piezoelectric crystals, Actuation using Electrostatic forces (Parallel plate, Torsion bar, Comb drive actuators), Micromechanical Motors and pumps. Case study: Comb drive actuators.

UNIT V: NANOSYSTEMS AND QUANTUM MECHANICS 9
Atomic Structures and Quantum Mechanics, Molecular and Nanostructure Dynamics: Shrodinger Equation and Wavefunction Theory, Density Functional Theory, Nanostructures and Molecular Dynamics, Electromagnetic Fields and their quantization, Molecular Wires and Molecular Circuits.

TOTAL: 45 Hours

REFERENCE BOOKS:

Sl.No	Author(s)	Title of the Book	Publisher	Year of Publication
1.	Marc Madou	Fundamentals of Microfabrication	CRC press	1997
2.	Stephen D. Senturia	Micro system Design	Kluwer Academic Publishers	2001
3.	Tai Ran Hsu	MEMS and Microsystems Design and Manufacture	Tata Mcraw Hill	2002

| 4. | Chang Liu | Foundations of MEMS | Pearson education India limited | 2006 |
| 5. | Sergey Edward Lyshevski | MEMS and NEMS: Systems, Devices, and Structures | CRC Press | 2002 |

WEB URLs

1. www.microfabrica.com/capabilitics
2. www.mems-exchange.org/MEMS/fabrication.htm
3. mspde.usc.edu/inspiring/resource/sensor/Microsensors.pdf
4. nptel.ac.in/courses/112108092/module1/lec04.pd
5. iam.khv.ru/articles/Gorkusha/gork12.pdf

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19VLC10	SOFT COMPUTING	L P T C
		3 0 0 3

COURSE OBJECTIVES :

- To Learn Fundamentals of fuzzy logic.
- To Learn Fundamentals of neural networks .
- To Learn Fundamentals of genetic algorithm, which have their roots
- To Learn Fundamentals of Artificial Intelligence.
- Healthy integration of all these techniques has resulted in extending the capabilities of the technologies to more effective and efficient problem solving methodologies.
- To learn applications of soft computing

COURSE OUTCOMES :

- Identify and describe soft computing techniques and their roles in building intelligent machines
- Recognize the feasibility of applying a soft computing methodology for a particular problem
- Apply fuzzy logic and reasoning to handle uncertainty and solve engineering problems
- Apply genetic algorithms to combinatorial optimization problems
- Apply neural networks to pattern classification and regression problems
- Able to learn To learn applications of soft computing

UNIT I: INTRODUCTION TO SOFT COMPUTING   9
Introduction, Fuzzy Computing, Neural Computing, Genetic Algorithms, Associative Memory, Adaptive Resonance Theory, Applications.

UNIT II: FUNDAMENTALS OF NEURAL NETWORKS   9
Introduction, Model of Artificial Neuron, Architectures, Learning Methods, Taxonomy of NN Systems, Single-Layer NN System, Applications. Back Propagation Network Background, Back-Propagation Learning, Back-Propagation Algorithm. Associative Memory : Description, Auto-associative Memory, Bi-directional Hetero-associative Memory. Adaptive Resonance Theory : Recap - supervised, unsupervised, backprop algorithms; Competitive Learning; Stability-Plasticity Dilemma (SPD)

UNIT III : FUZZY SET THEORY   9
Introduction, Fuzzy set : Membership, Operations, Properties; Fuzzy Relations. Fuzzy Systems : Introduction, Fuzzy Logic, Fuzzification, Fuzzy Inference, Fuzzy Rule Based System, Defuzzification

UNIT IV: FUNDAMENTALS OF GENETIC ALGORITHMS   9
Introduction, Encoding, Operators of Genetic Algorithm, Basic Genetic Algorithm.

UNIT V : HYBRID SYSTEMS   9
Integration of Neural Networks, Fuzzy Logic and Genetic Algorithms, GA Based Back Propagation Networks, Fuzzy Back Propagation Networks, Fuzzy Associative Memories, Simplified Fuzzy ARTMAP

TOTAL: 45 Hours

REFERENCE BOOKS:

Sl.No	Author(s)	Title of the Book	Publisher	Year of Publication
1.	S. Rajasekaran and G.A. Vijayalaksmi Pai,	Neural Network, Fuzzy Logic, and Genetic Algorithms - Synthesis and Applications	Prentice Hall	2005
2	Kishan Mehrotra, Chilukuri K. Mohan and Sanjay Ranka	Elements of Artificial Neural Network	MIT Press	1996
3.	Melanie Mitc hell	An Introduction to Genetic Algorithm	MIT Press	1998
4.	David E. Goldberg,	Genetic Algorithms in Search, Optimization, and Machine Learning	Addison-Wesley	1989

| 5. | S. Haykin | Neural Networks | Pearson Education | 2001 |

WEB URLs :

1.users.du.se/~jwe/fuzzy/NFL/F9.PDF
2.www.csee.wvu.edu/~xiawang/courses/cpe520/title.pdf
3.www.mv.helsinki.fi/home/niskanon/zimmermann_review.pdf
4.www.myreaders.info/09_Genetic_Algorithms.pdf
5.www3.nd.edu/~isis/techreports/isis-2001-003.pdf

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19VLC11	VLSI FOR WIRELESS COMMUNICATION	L T P C
		3 0 0 3

COURSE OBJECTIVES:

- To understand the basics of wireless communication.
- To understand the concepts of transceiver architectures.
- To introduce to the students the low power design techniques of VLSI circuits.
- To learn the design and implementation of VLSI circuits for wireless communication systems.
- To learn to design Frequency Synthesizer.
- To Learn applications of wireless communication.

COURSE OUTCOMES:

- Understanding of application of VLSI circuits in wireless communication.
- Knowledge of various architectures used in implementing wireless systems.
- Discussion about design and simulation of low power techniques using software.
- Learn the VLSI design of wireless circuits.
- Able to design Frequency Synthesizers.
- Able to learn applications of wireless communication.

UNIT I: OVERVIEW OF MODULATION SCHEMES 9

Classical Channel - Wireless Channel Description - Path Loss - Channel Model and Envelope Fading - Multipath Fading : Frequency Selective and Fast Fading - Basics of Spread Spectrum and Spread Spectrum Techniques - PN Sequence.

UNIT II: TRANSCEIVER ARCHITECTURE 9

Transceiver Design Constraints - Baseband Subsystem Design - RF Subsystem Design - Super Heterodyne Receiver and Direct Conversion Receiver - Receiver Front-End - Filter Design- Non-Idealities and Design Parameters - Derivation of Noise Figure.

UNIT III: LOW POWER DESIGN TECHNIQUES 9

Source of Power Dissipation - Estimation of Power Dissipation - Reducing Power Dissipation at Device and Circuit Levels - Low Voltage and Low Power Operation - Reducing Power Dissipation at Architecture and Algorithm Levels.

UNIT IV: WIRELESS CIRCUITS 9

VLSI Design of LNA - Wideband and Narrow Band - Impedance Matching - Automatic Gain Control (AGC) Amplifier - Power Amplifier - Active Mixer - Analysis, Conversion Gain, Distortion Analysis - Low Frequency and High Frequency Case, Noise - Passive Mixer - Sampling Mixer and Switching Mixer Analysis of Distortion, Gain and Noise Conversion.

UNIT V : FREQUENCY SYNTHESIZERS 9

VLSI Design Of Frequency Synthesizers (FS) - Parameters Of FS - PLL Based Frequency Synthesizer, Phase Detector/Charge Pump- Dividers- VCO- LC Oscillators- Ring Oscillator- Phase Noise- Loop Filter Description, Design Approaches.

TOTAL: 45 Hours

REFERENCE BOOKS:

Sl.No	Author(s)	Title of the Book	Publisher	Year of Publication
1.	Bosco Leung	VLSI for Wireless Communication	Springer	2011
2.	Elmad N Farag and Mohamed I Elmasry	Mixed Signal VLSI Wireless Design- Circuits and Systems	Kluwer Academic Publishers	2002
3.	Marc Snir	Lower Bounds on VLSI Implementations of Communication Networks	Palala Press	2015
4.	Richard Cole	Lower Bounds on Communication Complexity in VLSI	27th Forgotten Books	2015

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5.	Xiaohua Tian, Thinh M. Le, Yong Lian	Entropy Coders of the H.264/AVC Standard: Algorithms and VLSI Architectures	17th Springer	2010

WEB URLs:

1.nptel.ac.in/courses/117102062/
2.nptel.ac.in/courses/IIT-MADRAS/frequency_synthesizer1/Pdfs/1_5.pdf
3.nptel.ac.in/courses/117101105//
4.freevideolectures.com › VLSI and ASIC Design › IIT Madras/
5.en.wikipedia.org/wiki/Frequency_synthesizer

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19VLC12	RECONFIGURABLE ARCHITECTURES	L T P C
		3 0 0 3

COURSE OBJECTIVES:

- To make the student learn, FPGA fundamentals, design and implementation of circuits in them
- To give basic knowledge of FPGA internals.
- To give basic understanding of tools used.
- Design VHDL and Verilog HDL coding.
- Design and testing of different fault simulations.
- To learn applications of reconfigurable architecture

COURSE OUTCOMES:

- To study architecture of ASIC's
- To study FPGA Technologies and Architecture
- To study Routing for FPGA   .
- Determine the Programmable logic cells.
- Design VHDL and Verilog HDL coding.
- Able to learn applications of reconfigurable architecture

UNIT I: I NTRODUCTION   9
Domain- specific processors , Application specific processors, Reconfigurable Computing Systems-Evolution of Reconfigurable systems –Characteristics of RCS advantages and issues –Fundamental concepts and design steps-Classification of reconfigurable architecture-fine ,coarse ,grain & hybrid Architectures.

UNIT II: FPGA TECHNOLOGIES AND ARCHITECTURE   9
Technology trends –Programming Technology- SRAM programmed FPGA 's - antifuse Programmed FPGA's, Erasable programming logic devices –Alternative FPGA architectures : MUV Vs LUT based logic blocks- CLB Vs LAB VS Slices – fast carry chains-Embedded Ram's – FPGA VS ASIC DESIGN styles.

UNIT III: ROUTING FOR FPGAS   9
General strategy for touting in FPGAS – Routing for row based FPGAS – Segmented channel routing definitions – Algorithm for I segment and K segment routing – Routing for symmetrical FPGAS ,flexibility of FPGA Routing.

UNIT IV: HIGH LEVEL DESIGN   9
FPGA design style: Technology independent optimization – Technology mapping- Placement. High level synthesis of reconfigurable hardware, high – level languages, design tools: Simulation (cycle based, event driven based)-Synthesis(logic / HDL Vs Physically aware)- timing analysis(static Vs dynamic) – Verification physical design tools.

UNIT V : APPLICATION SPECIFIC RCS   9
RCS for FFT algorithms – area efficient architectures – power efficient architectures – low energy reconfigurable single chip DSP system – minimizing the memory requirement for condition flow FFT implementation - memory reduction methods for FFT implementation RCS for embedded cores, image processing.

TOTAL: 45 Hours

REFERENCE BOOKS:

Sl.No	Author(s)	Title of the Book	Publisher	Year of Publication
1.	Stephen M. Trimberger	Field–Programmable Gate Array Technology	Springer	2007
2.	Clive "Max" Maxfield	The Design Warriors Guide to FPGAs: Devices, Tools and Flows	Newnes, Elsevier	2006
3.	Yuke Wang, Yiyan Tang, Yingtao Jiang, Jin-	Noval Memory Reference Reduction Methods for FFT Implementations on DSP Processors	IEEE truncations on signal processing	2007

	Gym Chung			
4.	Russell tessier and Wayne Burleson	Reconfigurable computing for Digital Signal Processing	Journal of VLSI Signal Processing	2001
5.	Marek Gorgon	FPGA Imaging: Reconfigurable Architectures for Image Processing and Analysis	Springer	2015

WEB URLs :

1. www.eit.lth.se/fileadmin/eit/home/scd.vow/theses/Thesis_HenrikSvensson.pdf
2. nptel.ac.in/courses/Webcourse-contents/IIT%20Kharagpur/.../Pdf/Lesson-20.pdf
3. www.eecg.toronto.edu/~jayar/pubs/theses/Brown/StephenBrown.pdf
4. nptel.ac.in/courses/106103019/2
5. www.bitsathy.ac.in/academics/pdf/syllabus/VLSI%20-%202015.pdf

AUDIT COURSES (AC)

19VLE01	ENGLISH FOR RESEARCH PAPER WRITING	L T P C
		2 0 0 0

Course objectives: Students will be able to:

1. Understand that how to improve your writing skills and level of readability

2. Learn about what to write in each section

3. Understand the skills needed when writing a Title

Ensure the good quality of paper at very first-time submission

Syllabus		
Units	**Contents**	**Hours**
1	Planning and Preparation, Word Order, Breaking up long sentences, Structuring Paragraphs and Sentences, Being Concise and Removing Redundancy, Avoiding Ambiguity and Vagueness	4
2	Clarifying Who Did What, Highlighting Your Findings, Hedging and Criticising, Paraphrasing and Plagiarism, Sections of a Paper, Abstracts. Introduction 4 3 Review of the	4
3	Review of the Literature, Methods, Results, Discussion, Conclusions, The Final Check	4
4	key skills are needed when writing a Title, key skills are needed when writing an Abstract, key skills are needed when writing an Introduction, skills needed when writing a Review of the Literature	4
5	skills are needed when writing the Methods, skills needed when writing the Results, skills are needed when writing the Discussion, skills are needed when writing the Conclusions	4
6	skills are needed when writing the Methods, skills needed when writing the Results, skills are needed when writing the Discussion, skills are needed when writing the Conclusions first- time submission	4

Suggested Studies:

1. Goldbort R (2006) Writing for Science, Yale University Press (available on Google Books)

2. Day R (2006) How to Write and Publish a Scientific Paper, Cambridge University Press

3. Highman N (1998), Handbook of Writing for the Mathematical Sciences, SIAM. Highman's book .

4. Adrian Wallwork , English for Writing Research Papers, Springer New York Dordrecht Heidelberg London, 2011

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| 19VLE02	DISASTER MANAGEMENT	L T P C
		2 0 0 0

Course Objectives:-Students will be able to:

1. Learn to demonstrate a critical understanding of key concepts in disaster risk reduction and humanitarian response.

2. Critically evaluate disaster risk reduction and humanitarian response policy and practice from multiple perspectives.

3. Develop an understanding of standards of humanitarian response and practical relevance in specific types of disasters and conflict situations.

4. Critically understand the strengths and weaknesses of disaster management approaches, planning and programming in different countries, particularly their home country or the countries they work.

<table>
<tr><td colspan="3" align="center">Syllabus</td></tr>
<tr><td align="center">Units</td><td align="center">Contents</td><td align="center">Hours</td></tr>
<tr><td align="center">1</td><td>Introduction Disaster: Definition, Factors And Significance; Difference Between Hazard And Disaster; Natural And Manmade Disasters: Difference, Nature, Types And Magnitude.</td><td align="center">4</td></tr>
<tr><td align="center">2</td><td>Repercussions Of Disasters And Hazards: Economic Damage, Loss Of Human And Animal Life, Destruction Of Ecosystem. Natural Disasters: Earthquakes, Volcanisms, Cyclones, Tsunamis, Floods, Droughts And Famines, Landslides And Avalanches, Man-made disaster: Nuclear Reactor Meltdown, Industrial Accidents, Oil Slicks And Spills, Outbreaks Of Disease And Epidemics, War And Conflicts.</td><td align="center">4</td></tr>
<tr><td align="center">3</td><td>Disaster Prone Areas In India Study Of Seismic Zones: Areas Prone To Floods And Droughts, Landslides And Avalanches; Areas Prone To Cyclonic And Coastal Hazards With Special Reference To Tsunami; Post-Disaster Diseases And Epidemics</td><td align="center">4</td></tr>
<tr><td align="center">4</td><td>Disaster Preparedness And Management Preparedness: Monitoring Of Phenomena Triggering A Disaster Or Hazard; Evaluation Of Risk: Application Of Remote Sensing, Data From Meteorological And Other Agencies, Media Reports: Governmental And Community Preparedness.</td><td align="center">4</td></tr>
<tr><td align="center">5</td><td>Risk Assessment Disaster Risk: Concept And Elements, Disaster Risk Reduction, Global And National Disaster Risk Situation. Techniques Of Risk Assessment, Global CoOperation In Risk Assessment And Warning, People's Participation In Risk Assessment. Strategies for Survival.</td><td align="center">4</td></tr>
<tr><td align="center">6</td><td>Disaster Mitigation: Meaning, Concept And Strategies Of Disaster Mitigation, Emerging Trends In Mitigation. Structural Mitigation And Non-Structural Mitigation, Programs Of Disaster Mitigation In India.</td><td align="center">4</td></tr>
</table>
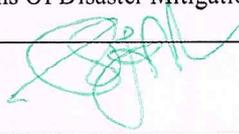
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SUGGESTED READINGS:

1. R. Nishith, Singh AK, "Disaster Management in India: Perspectives, issues and strategies "'New Royal book Company.

2. Sahni, Pardeep Et.Al. (Eds.)," Disaster Mitigation Experiences And Reflections", Prentice Hall Of India, New Delhi.

3. Goel S. L. , Disaster Administration And Management Text And Case Studies" ,Deep &Deep Publication Pvt. Ltd., New Delhi.

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19VLE03	SANSKRIT FOR TECHNICAL KNOWLEDGE	L T P C
		2 0 0 0

Course Objectives :

1. To get a working knowledge in illustrious Sanskrit, the scientific language in the world.

2. Learning of Sanskrit to improve brain functioning.

3. Learning of Sanskrit to develop the logic in mathematics, science & other subjects enhancing the memory power.

4. The engineering scholars equipped with Sanskrit will be able to explore the huge knowledge from ancient literature.

Syllabus		
Units	Contents	Hours
1	Alphabets in Sanskrit, Past/Present/Future Tense, Simple Sentences	8
2	Order Introduction of roots Technical information about Sanskrit Literature	8
3	Technical concepts of Engineering-Electrical, Mechanical, Architecture, Mathematics	8

Suggested reading
1. "Abhyaspustakam" – Dr.Vishwas, Samskrita-Bharti Publication, New Delhi
2. "Teach Yourself Sanskrit" Prathama Deeksha-Vempati Kutumbshastri, Rashtriya Sanskrit Sansthanam, New Delhi Publication
3. "India's Glorious Scientific Tradition" Suresh Soni, Ocean books (P) Ltd., New Delhi.

Course Output
Students will be able to
1. Understanding basic Sanskrit language.
2. Ancient Sanskrit literature about science & technology can be understood.
3. Being a logical language will help to develop logic in students.

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19VLE04	VALUE EDUCATION	L T P C
		2 0 0 0

Course Objectives

Students will be able to

1. Understand value of education and self- development
2. Imbibe good values in students
3. Let the should know about the importance of character

Course Objectives :
1. To get a working knowledge in illustrious Sanskrit, the scientific language in the world.
2. Learning of Sanskrit to improve brain functioning.
3. Learning of Sanskrit to develop the logic in mathematics, science & other subjects enhancing the memory power.
4. The engineering scholars equipped with Sanskrit will be able to explore the huge knowledge from ancient literature.

Syllabus		
Units	Contents	Hours
1	• Values and self-development –Social values and individual attitudes. Work ethics, Indian vision of humanism. • Moral and non- moral valuation. Standards and principles. • Value judgements	4
2	• Importance of cultivation of values. • Sense of duty. Devotion, Self-reliance. Confidence, Concentration. Truthfulness, Cleanliness. • Honesty, Humanity. Power of faith, National Unity. • Patriotism.Love for nature ,Discipline	4
3	• Personality and Behavior Development - Soul and Scientific • attitude. Positive Thinking. Integrity and discipline. • Punctuality, Love and Kindness. • Avoid fault Thinking. • Free from anger, Dignity of labour. • Universal brotherhood and religious tolerance. • True friendship. • Happiness Vs suffering, love for truth. • Aware of self-destructive habits. • Association and Cooperation. • Doing best for saving nature	4
4	• Character and Competence –Holy books vs Blind faith. • Self-management and Good health. • Science of reincarnation. • Equality, Nonviolence ,Humility, Role of Women. • All religions and same message. Mind your Mind, Self-control. • Honesty, Studying effectively	4

Suggested reading

1 Chakroborty, S.K. "Values and Ethics for organizations Theory and practice", Oxford University Press, New Delhi

Course outcomes

Students will be able to

1. Knowledge of self-development
2. Learn the importance of Human values
3. Developing the overall personality

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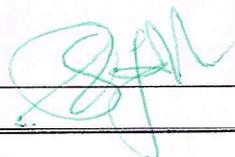| 19VLE05	CONSTITUTION OF INDIA	L T P C
		2 0 0 0

Course Objectives:

Students will be able to:

1. Understand the premises informing the twin themes of liberty and freedom from a civil rights perspective.

2. To address the growth of Indian opinion regarding modern Indian intellectuals' constitutional role and entitlement to civil and economic rights as well as the emergence of nationhood in the early years of Indian nationalism.

3. To address the role of socialism in India after the commencement of the Bolshevik Revolution in

1917 and its impact on the initial drafting of the Indian Constitution.

Syllabus		
Units	**Contents**	**Hours**
1	**History of Making of the Indian Constitution:** History Drafting Committee, (Composition & Working)	4
2	**Philosophy of the Indian Constitution:** Preamble Salient Features	4
3	**Contours of Constitutional Rights & Duties:** Fundamental Rights Right to Equality Right to Freedom Right against Exploitation Right to Freedom of Religion Cultural and Educational Rights Right to Constitutional Remedies Directive Principles of State Policy Fundamental Duties.	4
4	**Organs of Governance:** Parliament Composition	4

|			
		Qualifications and Disqualifications	
		Powers and Functions	
		Executive	
		President	
		Governor	
		Council of Ministers	
		Judiciary, Appointment and Transfer of Judges, Qualifications	
		Powers and Functions	
5		**Local Administration:** District's Administration head: Role and Importance, Municipalities: Introduction, Mayor and role of Elected Representative, CEO of Municipal Corporation. Pachayati raj: Introduction, PRI: Zila Pachayat. Elected officials and their roles, CEO Zila Pachayat: Position and role. Block level: Organizational Hierarchy (Different departments), Village level: Role of Elected and Appointed officials, Importance of grass root democracy	4
6		**Election Commission:** Election Commission: Role and Functioning. Chief Election Commissioner and Election Commissioners. State Election Commission: Role and Functioning. Institute and Bodies for the welfare of SC/ST/OBC and women.	4

Suggested reading
1. The Constitution of India, 1950 (Bare Act), Government Publication.
2. Dr. S. N. Busi, Dr. B. R. Ambedkar framing of Indian Constitution, 1st Edition, 2015.
3. M. P. Jain, Indian Constitution Law, 7th Edn., Lexis Nexis, 2014.
4. D.D. Basu, Introduction to the Constitution of India, Lexis Nexis, 2015.

Course Outcomes:
Students will be able to:
1. Discuss the growth of the demand for civil rights in India for the bulk of Indians before the arrival of Gandhi in Indian politics.
2. Discuss the intellectual origins of the framework of argument that informed the conceptualization of social reforms leading to revolution in India.
3. Discuss the circumstances surrounding the foundation of the Congress Socialist Party [CSP] under the leadership of Jawaharlal Nehru and the eventual failure of the proposal of direct elections through adult suffrage in the Indian Constitution.
4. Discuss the passage of the Hindu Code Bill of 1956.
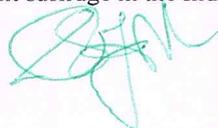
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19VLE06	PEDAGOGY STUDIES	L T P C
		2 0 0 0

Course Objectives:

Students will be able to:

1. Review existing evidence on the review topic to inform programme design and policy making undertaken by the DfID, other agencies and researchers.
2. Identify critical evidence gaps to guide the development.

Syllabus		
Units	**Contents**	**Hours**
1	**Introduction and Methodology:** Aims and rationale, Policy background, Conceptual framework and terminology Theories of learning, Curriculum, Teacher education. Conceptual framework, Research questions. Overview of methodology and Searching.	4
2	Thematic overview: Pedagogical practices are being used by teachers in formal and informal classrooms in developing countries. Curriculum, Teacher education.	4
3	Evidence on the effectiveness of pedagogical practices Methodology for the in depth stage: quality assessment of included studies. How can teacher education (curriculum and practicum) and the school curriculum and guidance materials best support effective pedagogy? Theory of change. Strength and nature of the body of evidence for effective pedagogical practices. Pedagogic theory and pedagogical approaches. Teachers' attitudes and beliefs and Pedagogic strategies.	4
4	Professional development: alignment with classroom practices and follow-up support Peer support Support from the head teacher and the community. Curriculum and assessment	4

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	Barriers to learning: limited resources and large class sizes		
5	**Research gaps and future directions** Research design Contexts Pedagogy Teacher education Curriculum and assessment Dissemination and research impact.		4

Suggested reading
1. Ackers J, Hardman F (2001) Classroom interaction in Kenyan primary schools, Compare, 31 (2):245-261.
2. Agrawal M (2004) Curricular reform in schools: The importance of evaluation, Journal of Curriculum Studies, 36 (3): 361-379.
3. Akyeampong K (2003) Teacher training in Ghana - does it count? Multi-site teacher education research project (MUSTER) country report 1. London: DFID.
4. Akyeampong K, Lussier K, Pryor J, Westbrook J (2013) Improving teaching and learning of basic maths and reading in Africa: Does teacher preparation count? International Journal Educational Development, 33 (3): 272–282.
5. Alexander RJ (2001) Culture and pedagogy: International comparisons in primary education. Oxford and Boston: Blackwell.
6. Chavan M (2003) Read India: A mass scale, rapid, 'learning to read' campaign.
7. www.pratham.org/images/resource%20working%20paper%202.pdf.

Course Outcomes:
Students will be able to understand:
1. What pedagogical practices are being used by teachers in formal and informal classrooms in developing countries?
2. What is the evidence on the effectiveness of these pedagogical practices, in what conditions, and with what population of learners?
3. How can teacher education (curriculum and practicum) and the school curriculum and guidance materials best support effective pedagogy?

19VLE07	STRESS MANAGEMENT BY YOGA	L T P C
		2 0 0 0

Course Objectives
1. To achieve overall health of body and mind
2. To overcome stress

Course Objectives:

Students will be able to:

4. Review existing evidence on the review topic to inform programme design and policy making

undertaken by the DfID, other agencies and researchers.

5. Identify critical evidence gaps to guide the development.

<table>
<tr><td colspan="3" align="center">Syllabus</td></tr>
<tr><td>Units</td><td>Contents</td><td>Hours</td></tr>
<tr><td>1</td><td>Definitions of Eight parts of yog. (Ashtanga)</td><td>8</td></tr>
<tr><td>2</td><td>Yam and Niyam.

Do`s and Don't's in life.

i) Ahinsa, satya, astheya, bramhacharya and aparigraha

ii) Shaucha, santosh, tapa, swadhyay, ishwarpranidhan</td><td>8</td></tr>
<tr><td>3</td><td>Asan and Pranayam

i) Various yog poses and their benefits for mind & body

ii)Regularization of breathing techniques and its effects- Types of

pranayam</td><td>8</td></tr>
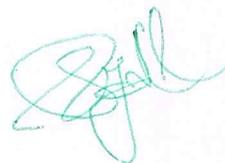</table>

Suggested reading
1. 'Yogic Asanas for Group Tarining-Part-I" : Janardan Swami Yogabhyasi Mandal, Nagpur
2. "Rajayoga or conquering the Internal Nature" by Swami Vivekananda, Advaita Ashrama (Publication Department), Kolkata

Course Outcomes:
Students will be able to:
1. Develop healthy mind in a healthy body thus improving social health also
2. Improve efficiency

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19VLE08   **PERSONALITY DEVELOPMENT THROUGH LIFE ENLIGHTENMENT SKILLS**   **L T P C**
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Course Objectives
1. To learn to achieve the highest goal happily
2. To become a person with stable mind, pleasing personality and determination
3. To awaken wisdom in students

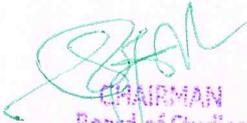| Syllabus		
Units	**Contents**	**Hours**
1	Neetisatakam-Holistic development of personality • Verses- 19,20,21,22 (wisdom) • Verses- 29,31,32 (pride & heroism) • Verses- 26,28,63,65 (virtue) • Verses- 52,53,59 (dont's) • Verses- 71,73,75,78 (do's)	8
2	• Approach to day to day work and duties. • Shrimad Bhagwad Geeta : Chapter 2-Verses 41, 47,48, • Chapter 3-Verses 13, 21, 27, 35, Chapter 6-Verses 5,13,17, • 23, 35, • Chapter 18-Verses 45, 46, 48.	8
3	• Statements of basic knowledge. • Shrimad Bhagwad Geeta: Chapter2-Verses 56, 62, 68 • Chapter 12 -Verses 13, 14, 15, 16,17, 18 • Personality of Role model. Shrimad Bhagwad Geeta: • Chapter2-Verses 17, Chapter 3-Verses 36,37,42, • Chapter 4-Verses 18, 38,39 • Chapter18 – Verses 37,38,63	8

Suggested reading
1. "Srimad Bhagavad Gita" by Swami Swarupananda Advaita Ashram (Publication Department), Kolkata
2. Bhartrihari's Three Satakam (Niti-sringar-vairagya) by P.Gopinath, Rashtriya Sanskrit Sansthanam, New Delhi.

Course Outcomes
Students will be able to
1. Study of Shrimad-Bhagwad-Geeta will help the student in developing his personality and achieve the highest goal in life
2. The person who has studied Geeta will lead the nation and mankind to peace and prosperity
3. Study of Neetishatakam will help in developing versatile personality of students.

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