MUTHAYAMMAL ENGINEERING COLLEGE

(An Autonomous Institution)

(Approved by AICTE, New Delhi, Accredited by NAAC, NBA & Affiliated to Anna University)

Rasipuram - 637 408, Namakkal Dist., Tamil Nadu.

Curriculum/Syllabus

Programme Code : VL

Programme Name : M.E. – VLSI DESIGN

Regulation : R-2016

MUTHAYAMMAL ENGINEERING COLLEGE

(An Autonomous Institution)

(Approved by AICTE, Accredited by NAAC & NBA, Affiliated to Anna University)

Rasipuram - 637 408, Namakkal Dt, Tamil Nadu.

Ph. No.: 04287-220837

Email: principal@mec.edu.in.

MUTHAYAMMAL ENGINEERING COLLEGE

(An Autonomous Institution)

(Approved by AICTE, New Delhi, Accredited by NAAC, NBA & Affiliated to Anna University)

Rasipuram - 637 408, Namakkal Dist., Tamil Nadu.

INSTITUTION VISION & MISSION

INSTITUTION VISION

To be a Centre of Excellence in Engineering, Technology and Management on par with International Standards

INSTITUTION MISSION

- To prepare the students with high professional skills and ethical values
- To impart knowledge through best practices
- To instill a spirit of innovation through Training, Research and Development
- To undertake continuous assessment and remedial measures
- To achieve academic excellence through intellectual, emotional and social stimulation

INSTITUTION MOTTO

Rural upliftment through Technical Education

MUTHAYAMMAL ENGINEERING COLLEGE

(An Autonomous Institution)

(Approved by AICTE, New Delhi, Accredited by NAAC, NBA & Affiliated to Anna University)
Rasipuram - 637 408, Namakkal Dist., Tamil Nadu.

DEPARTMENT VISION & MISSION

DEPARTMENT VISION

To empower the electronics and communication engineering students on basics and advanced technologies in both theoretical and experimental practices with research attitude and ethics

DEPARTMENT MISSION

- To impart need based education in electronics and communication engineering to meet the requirements of academic, industry and society
- To establish the state-of-art laboratories to prepare the students for facing the challenges ahead
- To prepare the students for employment, higher education and research oriented activities

MUTHAYAMMAL ENGINEERING COLLEGE

(An Autonomous Institution)

(Approved by AICTE, New Delhi, Accredited by NAAC, NBA & Affiliated to Anna University)
Rasipuram - 637 408, Namakkal Dist., Tamil Nadu.

DEPARTMENT PROGRAM EDUCATIONAL OBJECTIVES, PROGRAM OUTCOMES & PROGRAM SPECIFIC OUTCOMES

PROGRAM EDUCATIONAL OBJECTIVES

The Electronics and Communication Engineering Graduates should be able to

PEO1: Pursue as an engineer with necessary conceptual, analytical and theoretical knowledge in the domain of electronics and communication engineering

PEO2: Acquire the practical knowledge through basics and advanced laboratories in the field of electronics and communication engineering

PEO3: Demonstrate the leadership skills through entrepreneurship, employment and higher studies and to practice ethical values for the benefit of society and environment

PROGRAM OUTCOMES

1. **Engineering Knowledge:** Apply the knowledge of mathematics, science, engineering fundamentals, and an engineering specialization to the solution of complex engineering problems.
2. **Problem Analysis:** Identify, formulate, review research literature, and analyze complex engineering problems reaching substantiated conclusions using first principles of mathematics, natural sciences, and engineering sciences
3. **Design/Development solutions:** Design solutions for complex engineering problems and design system components or processes that meet the specified needs with appropriate consideration for the public health and safety, and the cultural, societal, and environmental considerations.
4. **Conduct investigations of complex problems:** Use research-based knowledge and research methods including design of experiments, analysis and interpretation of data, and synthesis of the information to provide valid conclusions.
5. **Modern tool usage:** Create, select, and apply appropriate techniques, resources, and modern engineering and IT tools including prediction and modeling to complex engineering activities with an understanding of the limitations.

6. **The engineer and society:** Apply reasoning informed by the contextual knowledge to assess societal, health, safety, legal and cultural issues and the consequent responsibilities relevant to the professional engineering practice.
7. **Environment and sustainability**: Understand the impact of the professional engineering solutions in societal and environmental contexts, and demonstrate the knowledge of, and need for sustainable development.
8. **Ethics:** Apply ethical principles and commit to professional ethics and responsibilities and norms of the engineering practice.
9. **Individual and team work:** Function effectively as an individual and as a member or leader in diverse teams, and in multidisciplinary settings.
10. **Communication:** Communicate effectively on complex engineering activities with the engineering community and with society at large, such as, being able to comprehend and write effective reports and design documentation, make effective presentations, and give and receive clear instructions.
11. **Project management and finance:** Demonstrate knowledge and understanding of the engineering management principles and apply these to one's own work, as a member and leader in a team, to manage projects and in multidisciplinary environments.
12. **Lifelong learning:** Recognize the need for and have the preparation and ability to engage in independent and lifelong learning in the broadest context of technological change.

PROGRAM SPECIFIC OUTCOMES

PSO1: Design and analyze electronic circuits and systems for various applications

PSO2: Apply the acquired knowledge and analytical skills for modeling and simulation of advanced communication systems

PSO3: Ascertain the use of software and hardware tools for developing variety of electronics and communication systems

MUTHAYAMMAL ENGINEERING COLLEGE

(An Autonomous Institution)

(Approved by AICTE, New Delhi, Accredited by NAAC & Affiliated to Anna University)

Rasipuram - 637 408, Namakkal Dist., Tamil Nadu

Estd. 2000

M.E. – VLSI DESIGN

GROUPING OF COURSES

FOUNDATION COURSES (FC):

S.No.	Course Code	Course Title	Category	Contact Hours	Instruction Hours/week			Credit
					L	T	P	C
1.	16VLA01	Advanced Numerical Methods	FC	5	3	2	0	4
2.	16VLA02	Applied Mathematics	FC	5	3	2	0	4
3.	16VLA03	Applied Probability and Statistics	FC	5	3	2	0	4

Professional Core (PC):

S.No.	Course Code	Course Title	Category	Contact Hours	Instruction Hours/week			Credit
					L	T	P	C
1.	16VLB01	VLSI Signal Processing	PC	5	3	2	0	4
2.	16VLB02	VLSI Design Techniques	PC	3	3	0	0	3
3.	16VLB03	Analog VLSI Circuit Design	PC	3	3	0	0	3
4.	16VLB04	Solid State Device Modeling and Simulation	PC	3	3	0	0	3
5.	16VLB05	ASIC Design		3	3	0	0	3
6.	16VLB07	Digital CMOS VLSI Design	PC	5	3	0	0	3
7.	16VLB08	CAD for VLSI Circuits	PC	5	3	2	0	4
8.	16VLB09	Low Power VLSI Design	PC	3	3	0	0	3
9.	16VLB11	Testing of VLSI Circuits	PC	3	3	0	0	3

CHAIRMAN
Board of Studies
Department of Electronics and Communication Engineering
Muthayammal Engineering College (Autonomous)
Rasipuram, Namakkal - 637 40...

10.	16VLB06	VLSI Design Techniques Laboratory	PC	2	0	0	2	1
11.	16VLB10	Digital CMOS VLSI Design Laboratory	PC	2	0	0	2	1

Professional Electives (PE):

S.No.	Course Code	Course Title	Category	Contact Hours	Instruction Hours/week			Credit
					L	T	P	C
1.	16VLC01	Signal Integrity for High Speed Devices	PE	3	3	0	0	3
2.	16VLC02	Advanced Digital System Design	PE	3	3	0	0	3
3.	16VLC03	Submicron VLSI Design	PE	3	3	0	0	3
4.	16VLC04	VLSI Technology	PE	3	3	0	0	3
5.	16VLC05	DSP Integrated Circuits	PE	3	3	0	0	3
6.	16VLC06	ARM Processor and Applications	PE	3	3	0	0	3
7.	16VLC07	Hardware Design Verification Techniques	PE	3	3	0	0	3
8.	16VLC08	Design and Analysis of Algorithms	PE	3	3	0	0	3
9.	16VLC09	MEMS and NEMS	PE	3	3	0	0	3
10.	16VLC10	Soft Computing	PE	3	3	0	0	3
11.	16VLC11	VLSI for Wireless Communication	PE	3	3	0	0	3
12.	16VLC12	Reconfigurable Architectures	PE	3	3	0	0	3
13.	16VLC13	Research Methodology	PE	3	3	0	0	3
14.	16VLC14	RF Integrated Circuit Design	PE	3	3	0	0	3

CHAIRMAN
Board of Studies
Department of Electronics and Communication Engineering
Muthayammal Engineering College (Autonomous)
Rasipuram, Namakkal - 637 4

15.	16VLC15	Electromagnetic Interference and Compatibility	PE	3	3	0	0	3

Employability Enhancement Courses (EEC):

S.No.	Course Code	Course Title	Category	Contact Hours	Instruction Hours/week			Credit
					L	T	P	C
1.	16VLD01	Project Work Phase -I	EEC	12	0	0	12	6
2.	16VLD02	Project Work Phase -II	EEC	24	0	0	24	12

Audit Courses (AC) :

S.No.	Course Code	Course Title	Category	Contact Hours	Instruction Hours/week			Credit
					L	T	P	C
1.	16VLE01	English for Research Paper Writing	AC	2	2	0	0	0
2.	16VLE02	Disaster Management	AC	2	2	0	0	0
3.	16VLE03	Sanskrit for Technical Knowledge	AC	2	2	0	0	0
4.	16VLE04	Value Education	AC	2	2	0	0	0
5.	16VLE05	Constitution of India	AC	2	2	0	0	0
6.	16VLE06	Pedagogy Studies	AC	2	2	0	0	0
7.	16VLE07	Stress Management by Yoga	AC	2	2	0	0	0
8.	16VLE08	Personality Development through Life Enlightenment Skills.	AC	2	2	0	0	0

CHAIRMAN
Board of Studies
Department of Electronics and Communication Engineering
Muthayammal Engineering College (Autonomous)
R.Rasipuram, Namakkal - 637 408.

	MUTHAYAMMAL ENGINEERING COLLEGE (Autonomous) (Approved by AICTE & Affiliated to Anna University), RASIPURAM – 637 408	CURRICULUM PG R - 2016

Department	Electronics and Communication Engineering
Programme	M.E. – VLSI Design

SEMESTER - I

Sl. No.	Course Code	Course Name	Hours/ Week			Credit	Contact Hours
			L	T	P	C	
THEORY							
1.	16VLA02	Applied Mathematics	3	2	0	4	5
2.	16VLB01	VLSI Signal Processing	3	0	0	3	3
3.	16VLB02	VLSI Design Techniques	3	0	2	4	5
4.	16VLB03	Analog VLSI Circuit Design	3	0	0	3	3
5.	16VLB04	Solid State Device Modeling and Simulation	3	0	0	3	3
6.	16VLB05	ASIC Design	3	0	0	3	3
TotalCredits						**20**	

	MUTHAYAMMAL ENGINEERING COLLEGE (Autonomous) (Approved by AICTE & Affiliated to Anna University), RASIPURAM – 637 408	CURRICULUM PG R - 2016

Department	Electronics and Communication Engineering
Programme	M.E. – VLSI Design

SEMESTER - II

Sl. No.	Course Code	Course Name	Hours/ Week			Credit	Contact Hours
			L	T	P	C	
THEORY							
1.	16VLB06	Digital CMOS VLSI Design	3	0	2	4	5
2.	16VLB07	CAD for VLSI Circuits	3	2	0	4	5
3.	16VLB08	Low Power VLSI Design	3	0	0	3	3
4.	16VLC02	Advanced Digital System Design **(Elective I)**	3	0	0	3	3
5.	16VLC04	VLSI Technology **(Elective II)**	3	0	0	3	3
6.	16VLC05	DSP Integrated Circuits **(Elective III)**	3	0	0	3	3
TotalCredits						**20**	

CHAIRMAN
Board of Studies
Department of Electronics and Communication Engineering
Muthayammal Engineering College (Autonomous)
Rasipuram, N...

	MUTHAYAMMAL ENGINEERING COLLEGE (Autonomous) (Approved by AICTE & Affiliated to Anna University), RASIPURAM – 637 408	CURRICULUM PG R - 2016

Department	Electronics and Communication Engineering
Programme	M.E. – VLSI Design

SEMESTER - III

Sl. No.	Course Code	Course Name	Hours/ Week			Credit	Contact Hours
			L	T	P	C	
THEORY							
1.	16VLC09	MEMS and NEMS**(Elective IV)**	3	0	0	3	3
2.	16VLC10	Soft Computing**(Elective V)**	3	0	0	3	3
3.	16VLC11	VLSI for Wireless Communication **(Elective VI)**	3	0	0	3	3
PRACTICAL							
4.	16VLD01	Project Work Phase-I	0	0	12	6	12
TotalCredits						**15**	

	MUTHAYAMMAL ENGINEERING COLLEGE (Autonomous) (Approved by AICTE & Affiliated to Anna University), RASIPURAM – 637 408	CURRICULUM PG R - 2016

Department	Electronics and Communication Engineering
Programme	M.E. – VLSI Design

SEMESTER - IV

Sl. No.	Course Code	Course Name	Hours/ Week			Credit	Contact Hours
			L	T	P	C	
PRACTICAL							
1.	16VLD02	Project Work Phase-II	0	0	24	12	24
TotalCredits						**12**	

CHAIRMAN
Board of Studies
Department of Electronics and Communication Engineering
Muthayammal Engineering College (Autonomous)
Rasipuram, Namakkal - 637 408.

16VLA02 **APPLIED MATHEMATICS** **L T P C**
3 2 0 4

COURSE OBJECTIVES:

- To realize the use of matrix theory techniques in engineering applications and to develop for future applications.
- To analyze and solve the fundamental problem with prescribed or free boundary conditions in simple cases
- Demonstrate knowledge of mathematics and mechanics to construct, analyze and interpret real world problems
- Provide a foundation and motivation for exposure to statistical ideas subsequent to the course.
- To formulate and construct a mathematical model for a linear programming problem in real life situation
- To introduce Fourier series analysis which is central to many applications in engineering

COURSE OUTCOMES :

- Explain geometrical concepts related to orthogonality and least squares solutions and perform calculations related to orthogonality.
- The variation calculus makes access to mastering in a wide rangeof classical results of variational calculus. Students get up apply results in technical problem solutions
- The students will have a basic knowledge of the main fields of mathematics and mechanics, including differential equations, elasticity theory, fluid mechanics.
- The students will have an exposure of various distribution functions and help in acquiring skills in handling situations involving more than one variable
- The knowledge gained on this course helps the students to do engineering optimization.
- Demonstrate an understanding of the basic concepts of Fourier series analysis

UNIT I : MATRIX THEORY **9+6**

The Cholesky decomposition - Generalized Eigen vectors, Canonical basis - QR factorization - Least squares method - Singular value decomposition.

UNIT II : CALCULUS OF VARIATIONS **9+6**

Concept of variation and its properties – Euler's equation – Functional dependant on first and higher order derivatives – Functionals dependant on functions of several independent variables – Variational problems with moving boundaries – problems with constraints - Direct methods: Ritz and Kantorovich methods.

UNIT III: ONE DIMENSIONAL RANDOM VARIABLES **9+6**

Random variables - Probability function – moments – moment generating functions and their properties – Binomial, Poisson, Geometric, Uniform, Exponential, Gamma and Normal distributions – Function of a Random Variable.

UNIT IV: LINEAR PROGRAMMING **9+6**

Formulation – Graphical solution – Simplex method – Two phase method - Transportation and Assignment Models

UNIT V: FOURIER SERIES AND EIGEN VALUE PROBLEMS **9+6**

Fourier Trigonometric series: Periodic function as power signals – Convergence of series – Even and odd function: cosine and sine series -- Non-periodic function: Extension to other intervals - Power signals: Exponential Fourier series – Parseval's theorem and power spectrum – Eigen value problems and orthogonal functions – Regular Sturm-Liouville systems – Generalized Fourier series.

TOTAL: 45 + 30 Hours

CHAIRMAN
Board of Studies
Department of Electronics and Communication Engineering
Muthayammal Engineering College (Autonomous)
Rasipuram, Namakkal - 637 408.

REFERENCE BOOKS:

Sl.No	Author(s)	Title of the Book	Publisher	Year of Publication
1.	Mital.K.V. Mohan and Chander	Optimization Methods in Operations Research and Systems Analysis, 4th Edition	New Age International Publishers	2016
2.	Stark. H., and Woods. J.W.	Probability and Random Processes with Applications to Signal Processing, 4th Edition	Pearson Education, Asia	2014
3.	HamdyATaha	Operations Research, 9th Edition (Asia)	Pearson Education, Asia	2014
4.	Gupta, A.S.	Calculus of Variations with Applications	Prentice Hall of India Pvt. Ltd., New Delhi	2011
5.	Richard Bronson	Matrix Operation, Schaum's outline series, 2nd Edition	McGraw Hill	2011

WEB URLs

1. http://nptel.ac.in/courses/111108066/ http://www.cs.utexas.edu/~pingali/CS378/2011sp/lectures/chol4.pdf
2. http://www.math.uni-leipzig.de/~miersemann/variabook.pdf
3. http://nptel.ac.in/courses/IIT-MADRAS/Principles_of_Communication1/Pdfs/1_5.pdf
4. http://nptel.ac.in/courses/111104027/
5. http://nptel.ac.in/courses/111106046/

CHAIRMAN
Board of Studies
Department of Electronics and Communication Engineering
Muthayammal Engineering College (Autonomous)
Rasipuram, Namakkal - 637 408.

16VLB01 **VLSI SIGNAL PROCESSING** **L T P C**
3 0 0 3

COURSE OBJECTIVES:

- To understand the various VLSI architectures for digital signal processing
- To know the methods of critical path reduction.
- To know the techniques of critical path and algorithmic strength reduction in the filter structures.
- To study the performance parameters, viz. area, speed and power
- To carry out HDL simulation of various DSP algorithms.
- To understand synchronous ,asynchronous pipelining

COURSE OUTCOMES:

- To be able to design architectures for DSP algorithms.
- To be able to optimize design in terms of area, speed and power
- To be able to design recursive and adaptive filters.
- To be able to incorporate pipeline based architectures in the design
- To be able to carry out HDL simulation of various DSP algorithms
- To be able to analyze synchronous, asynchronous pipelining

UNIT I: INTRODUCTION 9
Overview of DSP – FPGA Technology – DSP Technology requirements – Design Implementation.

UNIT II: METHODS OF CRITICAL PATH REDUCTION 9
Binary Adders – Binary Multipliers – Multiply-Accumulator (MAC) and sum of product (SOP) –Pipelining and parallel processing – retiming – unfolding – systolic architecture design.

UNIT III: ALGORITHMIC STRENGTH REDUCTION METHODS AND RECURSIVE FILTER DESIGN 9
Fast convolution-pipelined and parallel processing of recursive and adaptive filters – fast IIR filters design.

UNIT IV: DESIGN OF PIPELINED DIGITAL FILTERS 9
Designing FIR filters – Digital lattice filter structures – bit level arithmetic architecture – redundantarithmetic – scaling and round-off noise.

UNIT V: SYNCHRONOUS, ASYNCHRONOUS PIPELINING AND PROGRAMMABLE DSP 9
Numeric strength reduction – synchronous – wave and asynchronous pipelines – low power design –programmable DSPs – DSP architectural features/alternatives for high performance and low power.

TOTAL: 45Hours

REFERENCE BOOKS:

Sl.No	Author(s)	Title of the Book	Publisher	Year of Publication
1.	KeshabK.Parhi	VLSI Digital Signal Processing Systems, Design and Implementation	John Wiley	2007
2.	U. Meyer – Baese	Digital Signal Processing with Field Programmable Arrays	Springer, Second Edition,	2007

CHAIRMAN
Board of Studies
Department of Electronics and Communication Engineering
Muthayammal Engineering College (Autonomous)
Rasipuram, Namakkal - 637 408.

3.	S.Y.Kuang, H.J. White house, T. Kailath	VLSI and Modern Signal Processing	Prentice Hall	1995
4.	Gary Yeap	Practical Low Power Digital VLSI Design	Kluwer Academic Publishers	1998
5.	Mohammed Ismail and Terri Fiez	Analog VLSI Signal and Information Processing	Mc Graw-Hill	1994

WEB URLs :

1. nptel.kmeacollege.ac.in/syllabus/117101006/
2. www.smdp2vlsi.gov.in/smdp2vlsi/publicationIEP-vlsi-dsp-design-iikgp-n.jsp
3. nptel.ac.in/courses/117106087
4. www.ee.ucla.edu/~ingrid/ee213a/lectures/lectures.html
5. www.ee.iitm.ac.in/videolectures/doku.php?id=ee658_2008:start

CHAIRMAN
Board of Studies
Department of Electronics and Communication Engineering
Muthayammal Engineering College (Autonomous)
Rasipuram, Namakkal - 637 408.

16VLB02 VLSI DESIGN TECHNIQUES

L	T	P	C
3	0	2	4

COURSE OBJECTIVES:

- To understand the concepts of MOS transistors operations and their AC and DC characteristics.
- To know the fabrication process of cmos technology and its layout design rules
- To understand the latch up problem in cmos circuits.
- To study the concepts of cmos invertors and their sizing methods
- To know the concepts of power estimation and delay calculations in cmos circuits.
- To study the concepts of digital VLSI circuits

COURSE OUTCOMES:

- To be able to understand the concepts of MOS transistors operations and their AC and DC characteristics.
- To be able to know the fabrication process of cmos technology and its layout design rules
- To be able to understand the latch up problem in cmos circuits.
- To be able to know the concepts of cmos invertors and their sizing methods
- To be able to know the concepts of power estimation and delay calculations in cmos circuits.
- To be able to design digital VLSI circuits

UNIT I: MOS TRANSISTOR THEORY 9

NMOS and PMOS transistors, CMOS logic, MOS transistor theory – Introduction, Enhancementmode transistor action, Ideal I-V characteristics, DC transfer characteristics, Threshold voltage-Body effect- Design equations-Second order effects. MOS models and small signal ACcharacteristics, Simple MOS capacitance Models, Detailed MOS gate capacitance model, Detailed MOS Diffusion capacitance mode.

UNIT II: CMOS TECHNOLOGY AND DESIGN RULE 9

CMOS fabrication and Layout, CMOS technologies, P -Well process, N -Well process, twin –tubprocess, MOS layers stick diagrams and Layout diagram, Layout design rules, Latch up in CMOS circuits, CMOS process enhancements, Technology – related CAD issues, Fabrication and packaging.

UNIT III:INVERTERS AND LOGIC GATES 9

NMOS and CMOS Inverters, Inverter ratio, DC and transient characteristics , switching times,Super buffers, Driving large capacitance loads, CMOS logic structures , Transmission gates,Static CMOS design, dynamic CMOS design.

UNIT IV: CIRCUIT CHARACTERISATION AND PERFORMANCE ESTIMATION 9

Resistance estimation, Capacitance estimation, Inductance, switching characteristics, transistorsizing, power dissipation and design margining. Charge sharing .Scaling.

UNIT V:VLSI SYSTEM COMPONENTS CIRCUITS AND SYSTEM LEVELPHYSICAL DESIGN 9

Multiplexers, Decoders, comparators, priority encoders, Shift registers. Arithmetic circuits – Ripple carry adders, Carry look ahead adders, High-speed adders, Multipliers. Physical design – Delay modeling, cross talk, floor planning, power distribution. Clock distribution. Basics of CMOS testing.

TOTAL: 45 Hours

List of Experiments:

1. Design and simulation of combinational circuits using HDL.
2. Design and simulation of Sequential circuits using HDL.
3. Writing Test benches using VHDL/ Verilog.
4. Design and simulation of 8-Bit shift register using HDL.
5. Design and simulation of 4-bit carry save adder, Ripple carry adder using HDL.

CHAIRMAN
Board of Studies
Department of Electronics and Communication Engineering
Muthayammal Engineering College (Autonomous)
Rasipuram, Namakkal - 637 408.

6. Design and simulation of 8-bit adder / subtractor using HDL.
7. Design and simulation of Multiplier using HDL
8. Design and simulation of FSM using HDL.
9. Design and Implementation of Traffic Light Controller using VHDL.

REFERENCE BOOKS:

Sl.No	Author(s)	Title of the Book	Publisher	Year of Publication
1.	Neil H.E. Weste and Kamran Eshraghian	Principles of CMOS VLSI Design	Pearson Education ASIA, 2nd edition	2000
2.	John P.Uyemura	Introduction to VLSI Circuits and Systems	John Wiley & Sons, Inc.	2002
3.	Eugene D.Fabricius	Introduction to VLSI Design	McGraw Hill International Editions	1990
4.	Pucknell	Basic VLSI Design	Prentice Hall of India Publication	1995
5.	Wayne Wolf	Modern VLSI Design System on chip	Pearson Education	2002

WEB URLs :

1. www.nptelvideos.in/2012/12/digital-vlsi-system-design.html
2. nptel.ac.in/courses/117106092
3. www.egr.msu.edu/classes/ece410/mason/files/Ch2.pdf
4. www.ee.ucla.edu/~ingrid/ee213a/lectures/lectures.html
5. www.ee.iitm.ac.in/videolectures/doku.php?id=ee658_2008:start

CHAIRMAN
Board of Studies
Department of Electronics and Communication Engineering
Muthayammal Engineering College (Autonomous)
Rasipuram, Namakkal - 637 408.

16VLB03 ANALOG VLSI CIRCUIT DESIGN

L	T	P	C
3	0	0	3

COURSE OBJECTIVES:

- To study the concepts of CMOS and BICMOS analog circuits.
- To understand the concepts of A/D convertors and analog integrated sensors.
- To understand the testing concepts in analog VLSI circuits and its statistical modeling.
- To understand the concepts of VLSI interconnects.
- To impart in-depth knowledge about switched capacitors, ADCs and DACs.
- To study the concepts ofsampled-data analog filters

COURSE OUTCOMES:

- To be able to know the concepts of CMOS and BICMOS analog circuits.
- To be able to understand the concepts of A/D convertors and analog integrated sensors.
- To be able to understand the testing concepts in analog VLSI circuits and its statistical modeling.
- To be able to analyze VLSI interconnects.
- To be able to impart in-depth knowledge about switched capacitors, ADCs and DACs.
- To be able to know the concepts of sampled-data analog filters

UNIT I: BASIC CMOS CIRCUIT TECHNIQUES, CONTINUOUS TIME AND LOW VOLTAGE SIGNAL PROCESSING 9

Mixed-Signal VLSI Chips - Basic CMOS Circuits – Basic Gain Stage - Gain Boosting Techniques – Super MOS Transistor-Primitive Analog Cells-Linear Voltage-Current Converters –MOS Multipliers and Resistors-CMOS, Bipolar and Low-Voltage Bi CMOS Op- Amp Design-Instrumentation Amplifier Design-Low Voltage Filters.

UNIT II: BASIC BICMOS CIRCUIT TECHNIQUES, CURRENT -MODE SIGNAL PROCESSING AND NEURAL INFORMATION PROCESSING 9

Continuous-Time Signal Processing-Sampled-Data Signal Processing-Switched-CurrentData Converters-Practical Considerations in SI Circuits Biologically-Inspired Neural Networks - Floating - Gate. Low-Power Neural Networks-CMOS Technology and Models-Design Methodology-Networks-Contrast Sensitive Silicon Retina.

UNIT III: SAMPLED-DATA ANALOG FILTERS, OVER SAMPLED A/D CONVERTERS AND ANALOG INTEGRATED SENSORS 9

First-order and Second SC Circuits-Bilinear Transformation - Cascade Design-Switched-Capacitor Ladder Filter-Synthesis of Switched-Current Filter- Nyquist rate A/D Converters-Modulators for Over sampled A/D Conversion-First and Second Order and Multibit Sigma-Delta Modulators-Interpolative Modulators –Cascaded Architecture-Decimation Filters ,mechanical,Thermal, Humidity and Magnetic Sensors-Sensor Interfaces.

UNIT IV: DESIGN FOR TESTABILITY AND ANALOG VLSI INTERCONNECTS 9

Fault modeling and Simulation - Testability-Analysis Technique-Ad Hoc Methods andGeneral Guidelines-Scan Techniques-Boundary Scan-Built-in Self Test-Analog Test Buses-Design for Electron -Beam Testability-Physics of Interconnects in VLSI-Scaling ofInterconnects-A Model for Estimating Wiring Density-A Configurable Architecture forPrototyping Analog Circuits.

UNIT V: STATISTICAL MODELING AND SIMULATION 9

Review of Statistical Concepts - Statistical Device Modeling- Statistical Circuit Simulation-Automation Analog Circuit Design-automatic Analog Layout-CMOS Transistor Layout-Resistor Layout-Capacitor Layout-Analog Cell Layout-Mixed Analog -Digital Layout.

TOTAL: 45 Hours

CHAIRMAN
Board of Studies
Department of Electronics and Communication Engineering
Muthayammal Engineering College (Autonomous)
Rasipuram, Namakkal - 637 408.

REFERENCE BOOKS:

Sl.No	Author(s)	Title of the Book	Publisher	Year of Publication
1.	Mohammed Ismail, Terri Fief	Analog VLSI signal and Information Processing	McGraw- Hill	1994
2.	Malcom R.Haskard, Lan C.May	Analog VLSI Design - NMOS and CMOS	Prentice Hall	1998
3.	Randall L Geiger, Phillip E. Allen Noel K.Strader	VLSI Design Techniques for Analog and Digital Circuits	Mc Graw Hill	1990
4.	Jose E.France, YannisTsividis	Design of Analog-Digital VLSI Circuits for Telecommunication and signal Processing	Prentice Hall	1994
5.	Philip Allen &D.Holberg	CMOS Analog Circuit Design	Oxford University Press	2002

WEB URLs :

1. www.nptel.ac.in/courses/117101105/
2. www.youtube.com/watch?v=dKNzHqLEtYM
3. www.satishkashyap.com/2012/.../iit-video-lectures-on-analog-vlsi.html
4. www.youtube.com/watch?v=4It_j_Y944o
5. www.youtube.com/watch?v=jC0wMOehKqU

CHAIRMAN
Board of Studies
Department of Electronics and Communication Engineering
Muthayammal Engineering College (Autonomous)
Rasipuram, Namakkal - 637 408.

16VLB04 SOLID STATE DEVICE MODELING AND SIMULATION

L	T	P	C
3	0	0	3

COURSE OBJECTIVES:

- To know the basic semiconductor physics
- To understand the basic concepts bipolar device modeling
- To know the operation of MOSFET modeling.
- To understand the Operation parameter measurement.
- To study the functions characteristics of optoelectronic device modeling
- To study the various parameter measurements

COURSE OUTCOMES:

- Able to know the fundamentals of semiconductor physics.
- Understand BJT modeling.
- Understand and design MOSFET modeling.
- Analyze optoelectronic device modeling methods
- Able to study the functions characteristics of optoelectronic device modeling
- Able to understand various parameter measurements

UNIT I: SEMICONDUCTOR PHYSICS 9

Quantum Mechanical Concepts, Carrier Concentration, Transport Equation, Band gap, Mobility and Resistivity, Carrier Generation and Recombination, Avalanche Process, Noise Sources-Diodes : Forward and Reverse biased junctions –Reverse bias breakdown –Transient and AC conditions -Static and Dynamic behavior-Small and Large signal models –SPICE model for a Diode –Temperature and Area effects on Diode Model Parameters.

UNIT II:BIPOLAR DEVICE MODELING 9

Transistor Models: BJT –Transistor Action –Minority carrier distribution and Terminal currents - Switching-Eber -Molls and Gummel Poon Model, SPICE modeling -temperature and area effects.

UNIT III:MOSFET MODELING 9

OS Transistor –NMOS, PMOS –MOS Device equations -Threshold Voltage –Second order effects -Temperature Short Channel and Narrow Width Effect, Models for Enhancement, Depletion Type MOSFET, CMOS Models in SPICE.

UNIT IV: PARAMETER MEASUREMENT 9

Bipolar Junction Transistor Parameter –Static Parameter Measurement Techniques –Large signal parameter Measurement Techniques, Gummel Plots, MOSFET: Long and Short Channel Parameters, Measurement of Capacitance.

UNIT V: OPTOELECTRONIC DEVICE MODELING 9

Static and Dynamic Models, Rate Equations, Numerical Technique, Equivalent Circuits, Modeling of LEDs, Laser Diode and Photo detectors.

TOTAL: 45Hours

CHAIRMAN
Board of Studies
Department of Electronics and Communication Engineering
Muthayammal Engineering College (Autonomous)
Rasipuram, Namakkal - 637 408.

REFERENCE BOOKS:

Sl.No	Author(s)	Title of the Book	Publisher	Year of Publication
1.	Ben.G.Streetman	Solid State Devices	Prentice Hall	1997
2.	Giuseppe Massobrio and Paolo Antogentti	Semiconductor Device Modeling with SPICE, Second Edition,	McGraw-Hill Inc, New York	1993
3.	Mohammed Ismail & Terri Fiez	Analog VLSI-Signal & Information Processing 1st Edition	Tata McGraw Hill Publishing Company Ltd	2001
4.	Roulston E.J.,	Bipolar Semiconductor Devices	Mc-Graw Hill	1990
5.	Tor.A.Fijedly	Introduction to Device Modelling and Circuit Simulation	Wiley-interscience	1997

WEB URLs :

1. http://*nptel.ac.in/courses/115102025/*
2. http://*nptel.ac.in/courses/117103063/11*
3. http://*nptel.ac.in/courses/117103063/21*
4. http://*nptel.ac.in/courses/115102014/downloads/module3.pdf*
5. http://*nptel.ac.in/courses/113104012/*

CHAIRMAN
Board of Studies
Department of Electronics and Communication Engineering
Muthayammal Engineering College (Autonomous)
Rasipuram, Namakkal - 637 408.

16VLB05 **ASIC DESIGN** **L T P C**
3 0 0 3

COURSE OBJECTIVES:

- To acquire knowledge about various logics of ASICS and CMOS.
- To acquire knowledge about different types of ASICs design.
- To study about various types of Programmable ASICs architectures
- To study about various types of Programmable ASICs interconnects.
- To comprehend the low power design techniques and methodologies.
- To understand the floor planning, placement and routing

COURSE OUTCOMES:

- Analysis the different types of ASICs design.
- Analysis the different Logic cell architecture and interconnects.
- Analysis about different programmable ASIC design software.
- Identification of new developments in SOC
- Identification of developments in low power design.
- To analyze theFlash architecture, Pipelined Architecture

UNIT I: INTRODUCTION TO ASICS, CMOS LOGIC, ASIC LIBRARY DESIGN 9

Types of ASICs - Design flow –CMOS transistors-CMOS Design rules –Combinational logic Cell Sequential logic cell -Transistor as Resistors -Transistor parasitic capacitance –Logical effort -Library cell design –Library architecture-gate array design-standard cell design-data path cell design.

UNIT II : PROGRAMMABLE ASICS, PROGRAMMABLE ASIC LOGIC CELLS AND PROGRAMMABLE ASIC I/O CELLS 9

Anti fuse -Static RAM -EPROM and EEPROM technology -PREP benchmarks -Actel ACT -Xilinx LCA –Altera FLEX -Altera MAX-DC & AC inputs and outputs –clock input-power input -Xilinx I/O blocks.

UNIT III: PROGRAMMABLE ASIC INTERCONNECT, PROGRAMMABLE ASIC DESIGN SOFTWARE AND LOW LEVEL DESIGN ENTRY 9

Actel ACT -Xilinx LCA -Xilinx EPLD -Altera MAX 5000 and 7000 -Altera MAX 9000 -Altera FLEX –Design systems -Logic Synthesis -Half gate ASIC -Low level design language -PLA tools EDIF-CFI design representation.

UNIT IV :ASIC CONSTRUCTION 9

Performance metric, Flash architecture, Pipelined Architecture, Successive approximation architecture, Time interleaved architecture.

UNIT V: FLOOR PLANNING, PLACEMENT AND ROUTING 9

Floor planning –placement-physical design flow-information formats-Routing-Global routing, detailed routing, special routing, circuit extraction and DRC.

TOTAL: 45 Hours

REFERENCE BOOKS:

Sl.No	Author(s)	Title of the Book	Publisher	Year of Publication
1.	M.J.S. Smith	Application Specific Integrated Circuits	Pearson Education	2008
2.	FarzadNekoogar and FaranakNekoogar	From ASICs to SOCs: A Practical Approach	Prentice Hall PTR	2003
3.	Wayne Wolf	FPGA - Based System Design	Prentice Hall PTR	2009

CHAIRMAN
Board of Studies
Department of Electronics and Communication Engineering
Muthayammal Engineering College (Autonomous)
Rasipuram, Namakkal - 637 408.

4.	Wai-Kai Chen	Memory, Microprocessor, and ASIC	Prentice Hall	2006
5.	KhosrowGolshan	Physical Design Essentials: An Asic Design Implementation Perspective	Prentice Hall	2007

WEB URLs :

1. nptel.ac.in/courses/117106092/2
2. youtube.com/watch?v=9SnR3M3CIm4
3. youtube.com/watch?v=Y8FvvzcocT4
4. nptel.ac.in/courses/117106093/
5. nptel.ac.in/video.php?subjectId=117106092

Board of Studies
Department of Electronics and Communication Engineering
Muthayammal Engineering College (Autonomous)
Rasipuram, Namakkal - 637 408.

16VLB06 DIGITAL CMOS VLSI DESIGN

L	T	P	C
3	0	2	4

COURSE OBJECTIVES:

- To deal comprehensively with all aspects of transistor level design of all the digital building blocks
- To focus on the transistor level design
- To address all important issues related to size, speed and power consumption.
- To deal with the memory architectures
- To know the interconnect and clocking strategies.
- To understand the design of combinational and sequential CMOS circuits

COURSE OUTCOMES:

- Able to carry out transistor level hand calculation
- Able to design most important building blocks used in digital CMOS VLSI circuits.
- Able to develop strong understanding of the design methodology
- Able to develop tradeoffs of the various circuit choices for each of all the blocks discussed.
- Able to know the interconnect and clocking strategies.
- Able to design combinational and sequential CMOS circuits

UNIT I: MOS TRANSISTOR PRINCIPLES AND CMOS INVERTER 9

MOS(FET) Transistor Characteristic under Static and Dynamic Conditions, (Add)MOS device Design equation, MOS Transistor Secondary Effects, Process Variations, Technology Scaling, CMOS Inverter - Static Characteristic, Dynamic Characteristic, Power, Energy, and Energy Delay parameters,(Add) Tristate inverters.

UNIT II:COMBINATIONAL LOGIC CIRCUITS 9

Propagation Delays, Stick diagram, Layout diagrams, Examples of combinational logic design, Elmore's constant, Dynamic Logic Gates, Pass Transistor Logic, Power Dissipation, Low Power Design principles.

UNIT III:SEQUENTIAL LOGIC CIRCUITS 9

Static Latches and Registers, Dynamic Latches and Registers, Timing Issues, Pipelines, Pulse and sense amplifier based Registers, Nonbistable Sequential Circuits.

UNIT IV:ARITHMETIC BUILDING BLOCKS AND MEMORY ARCHITECTURES 9

Data path circuits, Architectures for Adders, Accumulators, Multipliers, Barrel Shifters, Speed and Area Tradeoffs, Memory Architectures, and Memory control circuits.

UNIT V:INTERCONNECT AND CLOCKING STRATEGIES 9

Interconnect Parameters – Capacitance, Resistance, and Inductance, Electrical Wire Models, Timing classification of Digital Systems, Synchronous Design, Self-Timed Circuit Design.

TOTAL: 45Hours

List of Experiments:

1. Design and simulate frequency response and noise analysis of any followers
2. Design and simulate operational amplifier performance parameters One stage Op Amps, Two stage Op Amps
3. Design and simulate cascode current mirrors and active current mirrors
4. Design of various routing – local routing, Area routing, Channel routing and global routing.

CHAIRMAN
Board of Studies
Department of Electronics and Communication Engineering
Muthayammal Engineering College (Autonomous)
Rasipuram, Namakkal - 637 408.

5. Design and simulation of Gate-level modeling
6. Design and simulation of Switch-level modeling
7. Modeling and synthesis of simple scheduling algorithm
8. Design and implement reducing power consumption in memories
9. Design and simulation of Power Estimation

REFERENCE BOOKS:

Sl.No	Author(s)	Title of the Book	Publisher	Year of Publication
1.	Jan Rabaey, AnanthaChandrakasan, B Nikolic	Digital Integrated Circuits: A Design Perspective	Prentice Hall of India.	2003
2	N.Weste, K. Eshraghian,	Principles of CMOS VLSI Design	Addision Wesley	1993
3.	M J Smith	Application Specific Integrated Circuits	Addisson Wesley	1997
4.	David A. Hodges, HoraceG. Jackson, and Resve A. Saleh	Analysis and Design of Digital Integrated Circuits	McGraw-Hill	2004
5.	Ken Martin	Digital Integrated Circuit Design	Oxford University Press	2000

WEB URLs :

1. *nptel.ac.in/courses/117101105*
2. *nptel.ac.in/courses/117106093*
3. *nptel.ac.in/downloads/117101105/*
4. www.nptelvideos.in/2012/12/vlsi-design.html
5. www.nptelvideos.in/2012/12/digital-vlsi-system-design.html

CHAIRMAN
Board of Studies
Department of Electronics and Communication Engineering
Muthayammal Engineering College (Autonomous)
Rasipuram, Namakkal - 637 408.

16VLB07 CAD FOR VLSI CIRCUITS

L	T	P	C
3	2	0	4

COURSE OBJECTIVES:

- To introduce the basic CAD algorithm
- To understand the Partitioning
- To study about Placement, Floor Planning
- To learn about Global, Detail routing
- To know the Modeling and synthesis in CAD flow.
- To understand theHigh level transformations

COURSE OUTCOMES:

- Learn the Fundamentals of basic algorithm in CAD.
- Study the different partitioning algorithm.
- Understand the floor planning and placement algorithm.
- Learn about different routing algorithms.
- Know about modeling and synthesis techniques of CAD.
- Able to analyze thelocal routing problems

UNIT I: VLSI DESIGN METHODOLOGIES 9

Introduction to VLSI Design methodologies - Review of Data structures and algorithms - Review of VLSI Design automation tools - Algorithmic Graph Theory and Computational Complexity - Tractable and Intractable problems – general purpose methods for combinatorial optimization.

UNIT II:DESIGN RULES 9

Layout Compaction - Design rules - problem formulation - algorithms for constraint graph compaction - placement and partitioning - Circuit representation – Placement algorithms – partitioning.

UNIT III:FLOOR PLANNING 9

Floor planning concepts - shape functions and floor plan sizing - Types of local routing problems - Area routing - channel routing - global routing - algorithms for global routing.

UNIT IV:SIMULATION 9

Simulation - Gate-level modeling and simulation - Switch-level modeling and simulation - Combinational Logic Synthesis - Binary Decision Diagrams – Two Level Logic Synthesis.

UNIT V:MODELLING AND SYNTHESIS 9

High level Synthesis - Hardware models - Internal representation - Allocation - assignment and scheduling - Simple scheduling algorithm – Assignment problem - High level transformations.

TOTAL: 45Hours

REFERENCE BOOKS:

Sl.No	Author(s)	Title of the Book	Publisher	Year of Publication
1.	S.H. Gerez	Algorithms for VLSI Design Automation	John Wiley & Sons	2002
2.	N.A. Sherwani	Algorithms for VLSI Physical Design Automation	Kluwer Academic Publishers	2002

CHAIRMAN
Board of Studies
Department of Electronics and Communication Engineering
Muthayammal Engineering College (Autonomous)
Rasipuram, Namakkal - 637 408.

3.	Giovanni De Micheli	Synthesis and Optimization of Digital Circuits	Tata McGraw Hill	1994
4.	M. Sarrafzadeh and C.K. Wong	An Introduction to VLSI Physical Design	McGraw Hill	1996
5.	Samir Palnitkar	Verilog HDL	Sun Microsystems Press A Prentice Hall Title	2001

WEB URLs:

1. http://*nptel.ac.in/courses/106103016*
2. http:// *www.ee.ncu.edu.tw/~jfli/vlsi21/lecture/ch01.pdf*
3. http://*nptel.ac.in/courses/Webcourse-contents/IIT.../VLSI%20Design/TOC-I13.html*
4. http:// *textofvideo.nptel.iitm.ac.in/106105083/lec17.pdf*
5. http:// *textofvideo.nptel.iitm.ac.in/112102101/lec1.pdf*

CHAIRMAN
Board of Studies
Department of Electronics and Communication Engineering
Muthayammal Engineering College (Autonomous)
Rasipuram, Namakkal - 637 4...

16VLB08 LOW POWER VLSI DESIGN

L	T	P	C
3	0	0	3

COURSE OBJECTIVES:

- To understand different sources of power dissipation in CMOS & MIS structure.
- To understand the different types of low power adders and multipliers
- To focus on synthesis of different level low power transforms.
- To gain knowledge on low power static RAM architecture & the source of power dissipation in SRAM
- To understand the various energy recovery techniques used in low power design
- To understand the Special techniques of low power VLSI design

COURSE OUTCOMES:

- An ability to analyze different source of power dissipation and the factors involved in.
- Able to understand the different techniques involved in low power adders and multipliers
- Understandings of the impact of various low power transform
- An ability to identify and analyze the different techniques involved in low power SRAM.
- Able to understand various energy recovery techniques.
- Able to analyze the adders and multipliers

UNIT I: POWER DISSIPATION 9

Hierarchy of limits of power – Sources of power consumption – Physics of power dissipation in CMOS FET devices – Basic principle of low power design. (Add) Power dissipation in Domino CMOS- Low power VLSI design limits.

UNIT II:POWER OPTIMIZATION 9

Logic level power optimization – Circuit level low power design – circuit techniques for reducing power consumption in adders and multipliers.

UNIT III:DESIGN OF LOW POWER CIRCUITS 9

Computer arithmetic techniques for low power system – reducing power consumption in memories – low power clock, Inter connect and layout design – Advanced techniques –Special techniques.

UNIT IV:POWER ESTIMATION 9

Power Estimation technique – logic power estimation – Simulation power analysis –Probabilistic power analysis, (Add) Modeling of signals- Signal probability calculation.

UNIT V: SYNTHESIS AND SOFTWARE DESIGN 9

Synthesis for low power – Behavioral level transform – software design for low power overlap and digital correction.

TOTAL: 45 Hours

REFERENCE BOOKS:

Sl.No	Author(s)	Title of the Book	Publisher	Year of Publication
1.	Kaushik Roy and S.C.Prasad	Low power CMOS VLSI circuit design	Wiley	2000
2.	DimitriosSoudris, Christians Pignet, Costas Goutis	Designing CMOS Circuits for Low Power	Kluwer	2002

CHAIRMAN
Board of Studies
Department of Electronics and Communication Engineering
Muthayammal Engineering College (Autonomous)
Rasipuram, Namakkal - 637 408.

3.	J.B.Kulo and J.H Lou	J.B.Kulo and J.H Lou	Wiley	1999
4.	A.P.Chandrasekaran and R.W.Broadersen	Low power digital CMOS design	Kluwer	1995
5.	Gary Yeap	Practical low power digital VLSI design	Kluwer	1998

WEB URLs:

1. nptel.ac.in/courses/111108066/
2. *nptel.ac.in/courses/106105034/36*
3. *nptel.ac.in/syllabus/106105034/*
4. www.nptelvideos.in/2012/11/low-power-vlsi-circuits-systems.html
5. *textofvideo.nptel.iitm.ac.in/106105034/lec1.pdf*

CHAIRMAN
Board of Studies
Department of Electronics and Communication Engineering
Muthayammal Engineering College (Autonomous)
Rasipuram, Namakkal - 637 408.

16VLC02 ADVANCED DIGITAL SYSTEM DESIGN

L	T	P	C
3	0	0	3

COURSE OBJECTIVES:

- To understand the concepts of advanced Boolean algebra
- To understand the concepts of threshold logic
- To understand the concepts of symmetric functions
- To understand the concepts of sequential logic circuits.
- To study the concepts of Fault Diagnosis and Testability Algorithms.
- To understand the concept of test generation.

COURSE OUTCOMES:

- To apply knowledge of Boolean algebra to the analysis and design of digital logic circuits.
- To acquire the knowledge of threshold logic
- To acquire the knowledge of symmetric functions.
- To view advanced digital design from a hierarchical viewpoint.
- To acquire the knowledge of testability concepts.
- To analyze the Built-in Self Test.

UNIT I: ADVANCED TOPICS IN BOOLEAN ALGEBRA 9

Shannon's expansion theorem, Consensus theorem, Octal designation, Run measure, INHIBIT / INCLUSION / AOI / Driver / Buffer gates, Gate expander, Reed Muller expansion, Synthesis of multiple output combinational logic circuits by product map method, Design of static hazard free and dynamic hazard free logic circuits.

UNIT II: THRESHOLD LOGIC 9

Linear seperability, Unateness, Physical implementation, Dual comparability, Reduced functions, Various theorems in threshold logic, Synthesis of single gate and multigate threshold Network.

UNIT III: SYMMETRIC FUNCTIONS 9

Elementary symmetric functions, Partially symmetric and total ly symmetric functions, McCluskey decomposition method, Unity ratio symmetric ratio functions, Synthesis of symmetric function by contact networks.

UNIT IV: SEQUENTIAL LOGIC CIRCUITS 9

Mealy machine, Moore machine, Trivial / Reversible / Isomorphic sequential machines, State diagrams, State table minimization, Incompletely specified sequential machines, State assignments, Design of synchronous and asynchronous sequential logic circuits working in the fundamental mode and pulse mode, Essential hazards Unger's theorem.

UNIT V: FAULT DIAGNOSIS AND TESTABILITY ALGORITHMS 9

Fault Table Method –Path Sensitization Method –Boolean Difference Method –Kohavi Algorithm –Tolerance Techniques –The Compact Algorithm –Fault in PLA –Test Generation –Masking Cycle –Built-in Self Test.

TOTAL: 45 Hours

REFERENCE BOOKS:

Sl.No	Author(s)	Title of the Book	Publisher	Year of Publication
1.	Charles H.Roth Jr	Fundamentals of Logic Design	Thomson Learning	2004

CHAIRMAN
Board of Studies
Department of Electronics and Communication Engineering
Muthayammal Engineering College (Autonomous)
Rasipuram, Namakkal - 637 408.

2	Nripendra N Biswas	Logic Design Theory	Prentice Hall of India	2001
3	Parag K.Lala	Digital system Design using PLD	B S Publications	2003
4	Lucien Ngalamou	Advanced Digital Systems Design with Rapid Prototyping on FPGAs Using VHDL	Springer	2012
5	Kuruvilla Varghese	Digital System Design with PLDs and FPGAs	Prentice Hall	2007

WEB URLs

1. nptel.ac.in/courses/117108040/downloads/Digital%20System%20Design.pdf
2. nptel.ac.in/video.php?subjectId=117105080
3. nptelvideos.in/2012/12/digital-systems-design.html
4. extofvideo.nptel.iitm.ac.in/117106092/lec1.pdf
5. youtube.com/watch?v=CL3ups78jrs

CHAIRMAN
Board of Studies
Department of Electronics and Communication Engineering
Muthayammal Engineering College (Autonomous)
Rasipuram, Namakkal - 637 408.

16VLC04 VLSI TECHNOLOGY

L	P	T	C
3	0	0	3

COURSE OBJECTIVES:

- To understand the Fabrication of ICs and purification of Silicon in different technologies.
- To impart in-depth knowledge about Etching and deposition of different layers.
- To understand the different packaging techniques of VLSI devices.
- To understand the fabrication technologies.
- To understand the integration techniques.
- To understand the MOS Memory IC technology

COURSE OUTCOMES:

- The ability to use metallization techniques to create three-dimensional device structures devices.
- The ability to know methodology to fabricate an IC's.
- The ability to observe the implementation techniques in chip designing.
- The ability to learn the application areas of VLSI technologies
- Able to understand the integration techniques.
- Able to analyze the MOS Memory IC technology

UNIT I: CRYSTAL GROWTH, WAFER PREPARATION, EPITAXY ANDOXIDATION 9

Electronic Grade Silicon, Czochralski crystal growing, Silicon Shaping, processing consideration,Vapor phase Epitaxy, Molecular Beam Epitaxy, Epitaxial Evaluation, Growth Mechanism andkinetics, Thin Oxides, Oxidation Techniques and Systems, Oxide properties, Redistribution ofDopants at interface, Oxidation of Poly Silicon, Oxidation induced Defects.

UNIT II:LITHOGRAPHY AND REACTIVE PLASMA ETCHING 9

Optical Lithography, Electron Lithography, X-Ray Lithography, Ion Lithography, Nano imprintLithography, Plasma properties, Feature Size control and Anisotropic Etch mechanism, reactivePlasma Etching techniques and Equipments.

UNIT III:DEPOSITION, DIFFUSION AND ION IMPLANTATION 9

Deposition process, Polysilicon, plasma assisted Deposition, Models of Diffusion in Solids, Fick'sone dimensional Diffusion Equation - Measurement techniques - Range theory- Implant equipment –Annealing- Shallow junction, High - energy implantation.

UNIT IV : METALLIZATION AND VLSI PROCESS INTEGRATION

9Physical Vapour Deposition (PVD) –Patterning- NMOS IC Technology – CMOS IC Technology – BICMOS IC Technology- MOS Memory IC technology - Bipolar IC Technology –Silicon onInsulator Technology– Noise in VLSI Technologies

UNIT V:ANALYTICAL, ASSEMBLY TECHNIQUES AND PACKAGING OF VLSI DEVICES 9

Analytical Beams – Beams Specimen interactions - Chemical methods – Package types – packagingdesign consideration – VLSI assembly technology – Package fabrication technology.Scanning Probe Techniques-Analysis by diffraction and fluorescence methods

TOTAL: 45 Hours

CHAIRMAN
Board of Studies
Department of Electronics and Communication Engineering
Muthayammal Engineering College (Autonomous)
Rasipuram, Namakkal - 637 408.

REFERENCE BOOKS:

Sl.No	Author(s)	Title of the Book	Publisher	Year of Publication
1.	S.M .Sze	VLSI Technology	McGraw Hill	2003
2.	Amar Mukherjee	Introduction to N MOS and CMOS VLSI System Design	PHI	2000
3.	James D Plummer, Michael D. Deal and Peter B. Griffin	Silicon VLSI Technology: Fundamentals Practice and Modeling	PHI	2000
4.	Wai Kai Chen	VLSI Technology	CRC press	2003
5.	Rainer Waser	Nano Electronics and Information Technolgy	Wiley-IEEE Press	2004

WEB URLs :

1. www.google.co.in/search?site=&source=hp&q=S.M+.Sze%2C+VLSI+Technology
2. www.scribd.com/doc/124363987/VLSI-DESIGN-pdf
3. nptel.ac.in/courses/IIT-MADRAS/Silicon VLSI Technology.pdf
4. nptel.ac.in/courses/111104027/
5. nptel.ac.in/courses/111106087/

CHAIRMAN
Board of Studies
Department of Electronics and Communication Engineering
Muthayammal Engineering College (Autonomous)
Rasipuram, Namakkal - 637 408.

16VLC05DSP INTEGRATED CIRCUITS

L	P	T	C
3	0	0	3

COURSE OBJECTIVES:

- To study the procedural flow of system design in DSP and Integrated circuit.
- To design FIR and IIR filters for the given specifications.
- To study the architectures for DSP system.
- To learn the design layout for VLSI circuits.
- To understand the concept of DSP Processor Architecture and code optimization.
- To learn the applications of DSP Integrated circuits.

COURSE OUTCOMES:

- To design filter and analysis the concept of finite word length effects.
- To synthesis DSP Architecture and design integrated circuits.
- To learn DSP Processor Architecture.
- The ability to learn the optimization techniques.
- To understand the concept of DSP Processor Architecture and code optimization.
- To learn the applications of DSP Integrated circuits.

UNIT I: DSP SYSTEMS AND MOS TECHNOLOGIES 9

Standard digital signal processors –Application specific IC's for DSP –DSP systems –DSP system design – Integrated circuit design – MOS transistors- MOS logic - VLSI process technologies – Trends in CMOS technologies.

UNIT II:DIGITAL FILTERS AND FINITE WORD LENGTH EFFECTS 9

FIR filters:FIR filter structures, FIR chips - IIR filters structures- Real time filtering – Circular buffering- Adaptive filtering: LMS and RLS Algorithm –Multi-rate filters: Interpolation with an integer factor L, Sampling rate change with a ratio L/M Finite Word Length Effects:Parasitic oscillations - Scaling of signal levels - Round-off noise – Measuring round-off noise.

UNIT III:DSP ARCHITECTURES AND ITS SYNTHESIS 9

DSP system architectures - Standard DSP architecture - Ideal DSP architectures - Multiprocessors and multicomputer - Systolic and Wave front arrays - Shared memory architectures - Mapping of DSP algorithms onto hardware - Implementation based on complex PEs - Shared memory architecture with Bi-serial PEs.

UNITIV:ARITHMETIC UNITS AND INTEGRATED CIRCUIT DESIGN 9

Conventional number system - Redundant Number system - Residue Number System - Bit-parallel and Bit-Serial arithmetic - Basic shift accumulator - Reducing the memory size - Complex multipliers - Improved shift-accumulator - Layout of VLSI circuits - FFT processor - DCT processor and Interpolator as case studies - Cordic algorithm.

UNIT V: TMS320C6X, DSP56XXX PROCESSORS ARCHITECTURE AND CODE OPTIMIZATION 9

CPU Operation – Pipelined CPU- Velocity TI – C64XDSP- Software tools: EVM – DSK Target C6x board – Assembly file – Memory management- Compiler utility- Code initialization – Code composer studio – Interrupt data processing, Code Optimization: Word- wide optimization – Mixing C and assembly- Software pipelining – C64X improvements - Overview on Free scale DSP56XXX Core Architecture. Design of modulo multipliers using RNS-complex multipliers-accumulator.

TOTAL: 45 Hours

CHAIRMAN
Board of Studies
Department of Electronics and Communication Engineering
Muthayammal Engineering College (Autonomous)
Rasipuram, Namakkal - 637 408.

REFERENCE BOOKS:

Sl.No	Author(s)	Title of the Book	Publisher	Year of Publication
1.	Lars Wanhammer	DSP Integrated Circuits	Academic press, New York	1999
2	Nasser Kehtarnavaz	DSP System Design Using the TMS320C6000	Wiley Prentice Hall	2001
	Richard G. Lyons	Understanding Digital Signal Processing 2004.	Prentice Hall	2010
	John G. Proakis, Dimitris K. Manolakis	Digital Signal Processing: Principles, Algorithms, and Applications.	Kluwer Acedamic Publishers	2006.
	Mohammed El-Sharkawy	Digital Signal Processing Applications with Motorola's DSP56002Processor,	Prentice Hall	2006

WEB URLs

1. www.annauniv.edu/academic_courses/WSA/.../07.%20VLSI%20Design.pdf
2. www.scribd.com/doc/310875222/1-Digital-Signal-Processing-Introduction
3. *www.computer.org/csdl/trans/tc/1985/05/01676588-abs.html*
4. *www.bitsathy.ac.in/academics/pdf/syllabus/VLSI%20-%202015.pdf*
5. nptel.ac.in/courses/IIT-MADRAS/ DSP Integrated Circuits /Pdfs/1_5.pdf

CHAIRMAN
Board of Studies
Department of Electronics and Communication Engineering
Muthayammal Engineering College (Autonomous)
Rasipuram, Namakkal - 637 408.

16VLC09	MEMS AND NEMS	L	T	P	C
		3	0	0	3

COURSE OBJECTIVES:

- To introducing the concepts of micro electro mechanical devices.
- To know the fabrication process of Microsystems.
- To know the design concepts of micro sensors and micro actuators.
- To introducing concepts of quantum mechanics.
- To introducing concepts of nano systems.
- To learn applications of MEMs.

COURSE OUTCOMES:

- Able to introduce the concepts of micro electro mechanical devices.
- Able to know the fabrication process of Microsystems.
- Able to know the design concepts of micro sensors and micro actuators.
- Able to introducing concepts of quantum mechanics.
- Able to introducing concepts of nano systems.
- Able to learn applications of MEMs.

UNIT I: OVERVIEW AND INTRODUCTION 9

New trends in Engineering and Science: Micro and Nanoscale systems Introduction to Design of MEMS and NEMS, Overview of Nano and Microelectromechanical Systems, Applications of Micro and Nanoelectromechanical systems, Microelectromechanical systems, devices and structures Definitions, Materials for MEMS: Silicon, silicon compounds, polymers, metals.

UNIT II :MEMS FABRICATION TECHNOLOGIES 9

Microsystem fabrication processes: Photolithography, Ion Implantation, Diffusion, Oxidation.Thin film depositions: LPCVD, Sputtering, Evaporation, Electroplating; Etching techniques: Dry and wet etching, electrochemical etching; Micromachining: Bulk Micromachining, Surface Micromachining,High Aspect-Ratio (LIGA and LIGA-like) Technology; Packaging: Microsystems packaging, Essential packaging technologies, Selection of packaging materials.

UNIT III: MICRO SENSORS 9

MEMS Sensors: Design of Acoustic wave sensors, resonant sensor, Vibratory gyroscope, Capacitive and Piezo Resistive Pressure sensors- engineering mechanics behind these Microsensors. Case study: Piezo-resistive pressure sensor.

UNIT IV: MICRO ACTUATORS 9

Design of Actuators: Actuation using thermal forces, Actuation using shape memory Alloys, Actuation using piezoelectric crystals, Actuation using Electrostatic forces (Parallel plate, Torsion bar, Comb drive actuators), Micromechanical Motors and pumps. Case study: Comb drive actuators.

UNIT V: NANOSYSTEMS AND QUANTUM MECHANICS 9

Atomic Structures and Quantum Mechanics, Molecular and Nanostructure Dynamics: Shrodinger Equation and Wavefunction Theory, Density Functional Theory, Nanostructures and Molecular Dynamics, Electromagnetic Fields and their quantization, Molecular Wires and Molecular Circuits.

TOTAL: 45 Hours

CHAIRMAN
Board of Studies
Muthayammal Engineering College (Autonomous)
Rasipuram, Namakkal - 637 408.

REFERENCE BOOKS:

Sl.No	Author(s)	Title of the Book	Publisher	Year of Publication
1.	Marc Madou	Fundamentals of Microfabrication	CRC press	1997
2.	Stephen D. Senturia	Micro system Design	Kluwer Academic Publishers	2001
3.	Tai Ran Hsu	MEMS and Microsystems Design and Manufacture	Tata Mcraw Hill	2002
4.	Chang Liu	Foundations of MEMS	Pearson education India limited	2006
5.	Sergey Edward Lyshevski	MEMS and NEMS: Systems, Devices, and Structures	CRC Press	2002

WEB URLs

1. *www.microfabrica.com/capabilities*
2. *www.mems-exchange.org/MEMS/fabrication.htm*
3. *mspde.usc.edu/inspiring/resource/sensor/Microsensors.pdf*
4. *nptel.ac.in/courses/112108092/module1/lec04.pd*
5. *iam.khv.ru/articles/Gorkusha/gork12.pdf*

CHAIRMAN
Board of Studies
Department of Electronics and Communication Engineering
Muthayammal Engineering College (Autonomous)
Rasipuram, Namakkal - 637 408.

16VLC10 SOFT COMPUTING

L	P	T	C
3	0	0	3

COURSE OBJECTIVES :

- To Learn Fundamentals of fuzzy logic.
- To Learn Fundamentals of neural networks .
- To Learn Fundamentals of genetic algorithm, which have their roots
- To Learn Fundamentals of Artificial Intelligence.
- Healthy integration of all these techniques has resulted in extending the capabilities of the technologies to more effective and efficient problem solving methodologies.
- To learn applications of soft computing

COURSE OUTCOMES :

- Identify and describe soft computing techniques and their roles in building intelligent machines
- Recognize the feasibility of applying a soft computing methodology for a particular problem
- Apply fuzzy logic and reasoning to handle uncertainty and solve engineering problems
- Apply genetic algorithms to combinatorial optimization problems
- Apply neural networks to pattern classification and regression problems
- Able to learn To learn applications of soft computing

UNIT I: INTRODUCTION TO SOFT COMPUTING 9

Introduction, Fuzzy Computing, Neural Computing, Genetic Algorithms, Associative Memory, Adaptive Resonance Theory, Applications.

UNIT II: FUNDAMENTALS OF NEURAL NETWORKS 9

Introduction, Model of Artificial Neuron, Architectures, Learning Methods, Taxonomy of NN Systems, Single-Layer NN System, Applications. Back Propagation Network Background, Back-Propagation Learning, Back-Propagation Algorithm. Associative Memory : Description, Auto-associative Memory, Bi-directional Hetero-associative Memory. Adaptive Resonance Theory : Recap - supervised, unsupervised, backprop algorithms; Competitive Learning; Stability-Plasticity Dilemma (SPD)

UNIT III :FUZZY SET THEORY 9

Introduction, Fuzzy set : Membership, Operations, Properties; Fuzzy Relations. Fuzzy Systems : Introduction, Fuzzy Logic, Fuzzification, Fuzzy Inference, Fuzzy Rule Based System, Defuzzification

UNIT IV:FUNDAMENTALS OF GENETIC ALGORITHMS 9

Introduction, Encoding, Operators of Genetic Algorithm, Basic Genetic Algorithm.

UNIT V : HYBRID SYSTEMS 9

Integration of Neural Networks, Fuzzy Logic and Genetic Algorithms, GA Based Back Propagation Networks, Fuzzy Back Propagation Networks, Fuzzy Associative Memories, Simplified Fuzzy ARTMAP

TOTAL: 45 Hours

REFERENCE BOOKS:

Sl.No	Author(s)	Title of the Book	Publisher	Year of Publication
1.	S. Rajasekaran and G.A. VijayalaksmiPai,	Neural Network, Fuzzy Logic, and Genetic Algorithms - Synthesis and Applications	Prentice Hall	2005

CHAIRMAN
Board of Studies
Department of Electronics and Communication Engineering
Muthayammal Engineering College (Autonomous)
Rasipuram, Namakkal - 637 408.

2	KishanMehrotra, Chilukuri K. Mohan and Sanjay Ranka	Elements of Artificial Neural Network	MIT Press	1996
3.	Melanie Mitc hell	An Introduction to Genetic Algorithm	MIT Press	1998
4.	David E. Goldberg,	Genetic Algorithms in Search, Optimization, and Machine Learning	Addison-Wesley	1989
5.	S. Haykin	Neural Networks	Pearson Education	2001

WEB URLs :

1.users.du.se/~jwe/fuzzy/NFL/F9.PDF
2.www.csee.wvu.edu/~xiawang/courses/cpe520/title.pdf
3.www.mv.helsinki.fi/home/niskanen/zimmermann_review.pdf
4.www.myreaders.info/09_Genetic_Algorithms.pdf
5.www3.nd.edu/~isis/techreports/isis-2001-003.pdf

CHAIRMAN
Board of Studies
Department of Electronics and Communication Engineering
Muthayammal Engineering College (Autonomous)
Rasipuram, Namakkal - 637 408.

16VLC11 VLSI FOR WIRELESS COMMUNICATION

L	T	P	C
3	0	0	3

COURSE OBJECTIVES:

- To understand the basics of wireless communication.
- To understand the concepts of transceiver architectures.
- To introduce to the students the low power design techniques of VLSI circuits.
- To learn the design and implementation of VLSI circuits for wireless communication systems.
- To learn to design Frequency Synthesizer.
- To Learn applications of wireless communication.

COURSE OUTCOMES:

- Understanding of application of VLSI circuits in wireless communication.
- Knowledge of various architectures used in implementing wireless systems.
- Discussion about design and simulation of low power techniques using software.
- Learn the VLSI design of wireless circuits.
- Able to design Frequency Synthesizers.
- Able to learn applications of wireless communication.

UNIT I: OVERVIEW OF MODULATION SCHEMES 9

Classical Channel - Wireless Channel Description - Path Loss - Channel Model and Envelope Fading - Multipath Fading : Frequency Selective and Fast Fading - Basics of Spread Spectrum and Spread Spectrum Techniques - PN Sequence.

UNIT II: TRANSCEIVER ARCHITECTURE 9

Transceiver Design Constraints - Baseband Subsystem Design - RF Subsystem Design - Super Heterodyne Receiver and Direct Conversion Receiver - Receiver Front-End - Filter Design- Non-Idealities and Design Parameters - Derivation of Noise Figure.

UNIT III: LOW POWER DESIGN TECHNIQUES 9

Source of Power Dissipation - Estimation of Power Dissipation - Reducing Power Dissipation at Device and Circuit Levels - Low Voltage and Low Power Operation - Reducing Power Dissipation at Architecture and Algorithm Levels.

UNIT IV: WIRELESS CIRCUITS 9

VLSI Design of LNA - Wideband and Narrow Band - Impedance Matching - Automatic Gain Control (AGC) Amplifier - Power Amplifier - Active Mixer - Analysis, Conversion Gain, Distortion Analysis - Low Frequency and High Frequency Case, Noise - Passive Mixer - Sampling Mixer and Switching Mixer Analysis of Distortion, Gain and Noise Conversion.

UNIT V :FREQUENCY SYNTHESIZERS 9

VLSI Design Of Frequency Synthesizers (FS) - Parameters Of FS - PLL Based Frequency Synthesizer, Phase Detector/Charge Pump- Dividers- VCO- LC Oscillators- Ring Oscillator- Phase Noise- Loop Filter Description, Design Approaches.

TOTAL: 45 Hours

CHAIRMAN
Board of Studies
Department of Electronics and Communication Engineering
Muthayammal Engineering College (Autonomous)
Rasipuram, Namakkal - 637 408.