IEEE Nanotechnology Council Madras Section

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Muthayammal Engineering College

(An Autonomous Institution)

Rasipuram - 637408, Namakkal DT, Tamilnadu

Department of Electronics and Communication Engineering

Cordially invite you to a webinar on

Emerging Device Technology for meeting post 2020 requirements in Digital Interconnect World: FinFETs, TFETs and NC-FETs

Dr. SUDEB DASGUPTA

Head of the Department

Department of ECE

Indian Institute of Technology, Roorkee

Date: 09th June 2020, Tuesday

Time: 11.00 am to 12.00 noon

About the Presentation

FinFET technology has emerged as a major milestone in the field of nano-electronics after the announcement by leading semiconductor industry to use the tri-gate transistors commercially in the 22 nm. In order to keep pace with Intel and TSMC,10 nm and 14 nm FinFET process nodes have rapidly emerging as preferred choice for digital applications. In this presentation, we focus on the novel device architecture abbreviated as dual-k spacer FinFET that intelligently uses the high permittivity spacer targeting for high-performance device-circuit co-design and its immunity to random statistical and structural variations. This webinar deals with Tunnel FETs and NC FET as these are the two most promising candidate for replacements of bulk device in coming decades. These devices can be used for circuit applications which will also be shown in the talk.

About the Speaker

Dr. S. Dasgupta, is presently working as Head of Department of Electronics and Communication Engineering at Indian Institute of Technology, Roorkee. He received his PhD degree in Electronics Engineering from IIT-BHU, Varanasi in 2000. He has authored more than 250 research papers in peer reviewed international journals and conferences. He is also heading the Technology Innovation Hub at IIT Roorkee a sponsored project for development of technology products under NM-ICPS. He was awarded with Erasmus Mundus Fellowship of European Union in the year 2010 to work in the area of RDF at Politecnico Di Torino, Italy. He is the recipient of prestigious IUSSTF to work in the area of SRAM testing at University of Wisconsin at Madison, USA in the year 2011-12. He was also awarded with DAAD Fellowship to work on Analog Design using Reconfigurable Logic at TU, Dresden, Germany in the year 2013. He has been nominated for INAE Young Engineer Award. He is a reviewer of various IEEE Transactions. He is a member of IEEE, EDS, ISTE and Associate Member of Institute of Nanotechnology, UK.

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