MUTHAYAMMAL ENGINEERING COLLEGE

(An Autonomous Institution)

(Approved by AICTE, New Delhi, Accredited by NAAC & Affiliated to Anna University)
Rasipuram - 637 408, Namakkal Dist., Tamil Nadu.

Department of Electronics and Communication Engineering
Question Bank - Academic Year (2021-22)

Course Code & Course Name : 19ECC12_& VLSI CIRCUIT DESIGN

Name of the Faculty : Mrs.S.PUNITHA

Year/Sem/Sec : III / V / C

Unit-I: MOS Transistor Theory

Part-A (2 Marks)

1. Give the variety of Integrated Circuits.
2. Give the basic process for IC fabrication
3. What are the various Silicon wafer Preparation?
4. Different types of oxidation.
5. What is the transistors CMOS technology provides?
6. What are the different layers in MOS?
7. What is Enhancement mode transistor?
8. What is Depletion mode Device?
9. When the channel is said to be pinched –off?
10. Give the different types of CMOS process.

Part-B (16 Marks)

1.	i) Derive the drain current of MOS device in different operating regions.	(8)
	ii) With neat diagram formulate the n-well and channel formation in CMOS process.	(8)
2.	i) Explain the operation of PMOS Enhancement and depletion mode.	(8)
	ii) Explain the operation of NMOS Enhancement and depletion mode.	(8)
3.	i) With neat diagram and describe the operation of NMOS transistor.	(8)
	ii) With neat diagram and describe the operation of PMOS transistor	(8)
4.	i) Describe the formation of p well with neat sketch.	(8)
	ii) Describe the formation of twin tub with neat sketch.	(8)
5.	i) Illustrate with necessary diagrams of SOI.	(10)
	ii) Describe the advantage of BiCMOS over CMOS technology	(6)

Unit-II : IC AND DIFFERENTIAL AMPLIFIERS

Part-A (2 Marks)

1. What is the need for demarcation line?
2. Define propagation delay of CMOS inverter.
3. Mention the different types of scaling technique.
4. Why NMOS transistor is selected as pull down transistor?
5. List the lambda based design rules used for layout.
6. What is stick diagram? Sketch the stick diagram for 2 input NAND gate.
7. Define hot carrier effect.
8. Draw the DC transfer characteristics of CMOS inverter.
9. Define body effect and write the threshold equation including the body
10. Design a 3 input NAND gate.

Part-B (16 Marks)

1. i) Describe the CMOS inverter and derive the DC characteristics. (10)

   ii) Illustrate the operation of noise margin with neat sketch. (6)

2. i) Draw the stick diagram and layout diagram using the function $Y = \overline{(A \cdot B \cdot C).D}$ of CMOS compound gate (8)

   ii) Label the necessary stick diagram and layout for the design of NAD and NOR gates (8)

3. Summarize the following: (8)

   i) CMOS process enhancements (8)

   ii) Layout design rules.

4. i) With necessary illustrations explain the layout design rules and draw the layout diagram for four input NAND and NOR gate. (10+6)

   ii) How to calculate the area of capacitance with example.

5. i) Explain in detail about the need of scaling, scaling principles and effect of scaling on MOSFET device parameters. (10+6)

   ii) How to calculate the sheet resistance with example.

Unit-III : SUBSYSTEM DESIGN & LAYOUT

Part-A (2 Marks)

1. Give Elmore delay expression for propagation delay of an inverter.
2. Why single phase dynamic logic structure cannot be cascaded? Justify.
3. What is a pull up and pull down device?
4. List the various power losses or power dissipation in CMOS circuits.
5. List the drawbacks of ratioed circuits.

6. Draw the pseudo nMOS inverter.
7. Draw the circuit diagram of a CMOS bistable element and its time domain behavior.
8. Write a note on CMOS transmission gate logic.
9. Give the different symbols for transmission gate.
10. What does local skew, global skew, useful skew mean?

Part-B (16 Marks)

1. Discuss briefly the principle and operation of the following along with its advantages.
   i) Pass Transistor logic (8)
   ii) Complementary Pass Transistor Logic (8)
2. i) Identify the design issues in dynamic CMOS (8)
   ii) Recall the factors that should be considered while designing Dynamic CMOS. (8)
3. Explain the operation of the following along with necessary diagrams
   i) Dynamic CMOS Domino (8)
   ii) NP Domino logic with necessary diagrams. (8)
4. i) Examine the characteristics of Pseudo-NMOS Circuits with the help of Inverter, NAND and NOR Gates. (8+8)
   ii) Evaluate the different methods of reducing static and dynamic power dissipation in CMOS circuits and Explain in briefly.
5. Write short notes on:
   i)Ratioed Circuits (4)
   ii)Dynamic CMOS Circuits (4)
   iii) Keepers (4)
   iv) Multiple Ouput Dynamic Logic (4)

UNIT IV - PROGRAMMABLE LOGIC DEVICES

PART – A (2 Marks)

1. What are feed through cells? State their uses?
2. State the features of full custom design.
3 What is an interconnect?
4 Define manufacturing lead time.
5 Define flexible blocks and standard cell.
6 List advantage of CBIC.
7 What is a primitive cell?

8 Give the different types of ASIC.

9 What is the full screen ASIC design?

10 What are feed through cells? State their uses?

Part-B (16 Marks)

1	i) Explain full custom and semi custom design or various types of ASIC.	(8)
	ii) Illustrate the concept of PAL.	(8)
2	i) Explain standard cell based design.	(8)
	ii) Illustrate the concept of PLA.	(8)
3.	i) Explain cell libraries.	(8)
	ii) Describe Finite State Machine design using PLA	(8)
4.	i) Explain FPGA building block architecture.	(8)
	ii) Describe standard cell design.	(8)
5.	i) Explain interconnect routing procedure.	(10)
	ii) Explain ASIC design flow.	(6)

Unit-V : VERILOG HDL DESIGN PROGRAMMING

Part-A (2 Marks)

1. What are identifiers?
2. What are the value sets in Verilog?
3. Give the different arithmetic operators?
4. Give the different bitwise operators.
5. What are gate primitives.
6. Give the two blocks in behavioral modeling.
7. What are the types of conditional statements?
8. Give the different bitwise operators
9. What is metastability and list the steps to prevent it ?
10. What is the difference between module and instance?

Part-B (16 Marks)

1.	i)Write a Verilog program for 3 to 8 decoder in gate level description	(8)
	ii) Explain various features of structural level modeling.	(8)
2.	i) Explain briefly about various levels of design description.	(8)
	ii) Write a brief note on test bench.	(8)
3.	i) Explain briefly about gate level modeling.	(8)
	ii)What are the procedural assignment statements?	(8)
4.	i) Explain the various timing control constructs available in Verilog HDL.	(8)

ii) Write a Verilog program to simulate a 4 bit ripple carry adder . (8)

5. i) Write a verilog program for 3:8 decoder. (8)

ii) Explain the syntax of conditional statements in Verilog HDL with examples. (8)

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Course Faculty **HoD**