MUTHAYAMMAL ENGINEERING COLLEGE

(An Autonomous Institution)

(Approved by AICTE, New Delhi, Accredited by NAAC & Affiliated to Anna University)
Rasipuram - 637 408, Namakkal Dist., Tamil Nadu.

Department of Electronics and Communication Engineering
Question Bank - Academic Year (2021-22)

Course Code & Course Name : 19ECE24 & Computer Architecture and Organization

Name of the Faculty : A.Nivetha

Year/Sem/Sec : III/V/A,B & C

Unit-I: Introduction

Part-A (2 Marks)

1. What is computer? List the major component s of a computer system.
2. Explain (i) ENIAC (II)UNIVAC.
3. Write down the basic performance equation?
4. Write the features of the third generation of computers.
5. Consider three processors P1, P2 and P3 executing the same instruction set. They have clock rates of 3GHz, 2.5GHz, and 4GHz respectively and CPI of 1.5, 1.0, and 2.2 respectively. Which processor has the highest performance expressed in instructions per second? If the processors each executes a program in 10 seconds, find the number of cycles and number of instructions in each processor.
6. What are the various ways of representing signed integers in the system?
7. Differentiate direct and indirect addressing modes.
8. What are the important factors that determine a computer's performance? Give its significance.
9. Give an example each of zero- address, one-address, two-address and three address instructions.
10. Give the IEEE standard double precision floating point format.

Part-B (16 Marks)

1.(i) (Describe the organization of a processor with the general register organization. (8)

(ii) Give the different instruction formats of a CPU in general. (8)

2. What is the need for addressing in a computer? Explain in detail about various addressing modes with suitable examples. (16)
3. Explain the representations of floating-point numbers in detail. (16)

4.(i) Elaborate Von Newmann computer architecture with neat diagram. (8)

(ii) Demonstrate fixed point data representation. (8)

5. Discuss the important measures of the performance of a computer and drive the basic performance equation and using this equation explain how the performance of a system can be improved. (16)

Unit-II : Data Path Design

Part-A (2 Marks)

1. Define data path in a CPU.
2. What are the 2 ways to detect overflow in an n-bit adder?
3. What are the overflow / underflow conditions for addition and subtraction?
4. What is booth algorithm? What are the two attractive features of Booth algorithm?
5. What is the purpose of guard bits used in floating point operations? what are the ways to truncate the guard bits?
6. Write IEEE standard for floating point format.
7. What are the exceptions encountered in FP operation?
8. Give advanced features of ALU.
9. What is a coprocessor?
10. Give the Booth's recoding and bit-pair recoding of the number 10001111010001010.

Part-B (16 Marks)

1.(i) Describe the Booth's algorithm for multiplication of signed two's complement numbers and its hardware implementation. (10)

(ii) Multiply the following signed numbers using Booth algorithm. A =(-34)10=(1011110)2 and B=(22)10=(0010110)2 where B is multiplicand and A is multiplier. (6)

2.(i) Draw and explain the flowchart of floating-point addition and subtraction process. (10)

(ii) Add the number (0.75)10 and (-0.275)10 in binary using the floating-point addition algorithm. (6)

3. Discuss in detail about non-restoring division algorithm in detail with diagram and examples. (16)
4. Describe the types of ALU with neat diagrams. (16)
5. Describe the Robertson's algorithm for multiplication of numbers and its hardware implementation. (16)

Unit-III : Control Design

Part-A (2 Marks)

1. Distinguish between hardwired control and micro programmed control.
2. Define pipeline's performance /cost ratio and speed up performance.
3. Write the sequence of control steps required for 3 bus structure for the following instruction : Add R4,R5,R6.
4. Compare horizontal and vertical format.
5. What is a pipeline control? Name the four steps in pipelining.
6. What is data hazard in pipelining? What are the solutions?
7. Draw the structure of two stage instruction pipeline.
8. What is pipelining and what are the advantages of pipelining?
9. Distinguish between static and dynamic branch prediction approaches.

10. What are superscalar processors?

Part-B (16 Marks)

1.	Explain the various design methods of hardwired control unit. or Give the organization of a typical hardwired control unit and explain the function performed by the various blocks. Discuss the data flow for a sample instruction.	(16)
2.	Explain in detail the working principle of a micro programmed control unit. Explain the operation of this control unit with a typical set of micro instructions.	(16)
3.(i)	Explain the function of a 6-segment pipeline and draw a space diagram for a six-segment pipeline showing the time it takes to process eight tasks.	(8)
(ii)	Discuss a 4-stage instruction pipeline and show how its performance is improved over sequential execution.	(8)
4.	Discuss various hazards that might arise in a pipeline. What are the remedies commonly adapted to overcome/minimize these hazards?	(16)
5.(i)	Describe the concept of pipelining. Compare it with sequential processing. Draw needed diagrams.	(8)
(ii)	What are superscalar processors? Explain the typical structure of a superscalar processor.	(8)

Unit-IV : Memory Organization

Part-A (2 Marks)

1. What is the function of a TLB (translation look-aside buffer)?
2. Define locality of reference. What are its types?
3. Define Average Memory Access Time for a computer system with two levels of caches.
4. List the difference between static RAM and dynamic RAM.
5. What is cache?
6. What is cache coherency and how is it eliminated?
7. What is write back and write through caches?
8. Define miss rate? Define miss penalty.
9. What is associate memory?
10. Define the term LRU and LFU.

Part-B (16 Marks)

1.(i)	Explain the concept memory hierarchy and the need of cache memory.	(8)
(ii)	Explain in detail internal organization of memory chip.	(8)
2.(i)	Discuss any six ways of improving the cache performance.	(8)
(ii)	Illustrate cache memory read and write operation.	(8)
3.(i)	Explain the concept of virtual memory with any one virtual memory management technique.	(8)
(ii)	Describe in detail about the memory mapping between virtual and main memory with an example.	(8)
4.	Describe in detail about associative memory. Or Give the basic cell of an associative memory and explain its operation. Show how associative memories can be constructed	(16)

using this basic cell.

5. Discuss the different mapping techniques used in cache memories and their relative merits and demerits. Compare the schemes in terms of cost and performance. (16)

Unit-V : System Organization

Part-A (2 Marks)

1. What is a non-maskable interrupt? What is the action performed on receipt of NMI?
2. Brief reliability and MTTF.
3. How does bus arbitration typically work?
4. What is DMA operation? State its advantages.
5. What is the advantage of using interrupt-initiated data transfer over transfer under program control without interrupt?
6. What is priority interrupt?
7. What is vectored interrupt?
8. What is program controlled I/O?
9. When the privilege exception arises?
10. Compare memory mapped I/O and I/O mapped I/O.

Part-B (16 Marks)

1.(i) Explain with block diagram the DMA transfer in a computer system. (8)

(ii) Draw the typical block diagram of a DMA controller and explain how it is used for data transfer between memory and peripherals. (8)

2.(i) Describe in detail about IOP organization. (8)

(ii) Give brief account on fault tolerance. (8)

3.(i) Explain the use of vectored interrupt in processors. Why is priority handling desired in interrupt controllers? How do the different priority schemes work? (10)

(ii) What are handshaking signals and what are the sequences of events during an input operation using handshake scheme? (6)

4.(i) Explain the difference between CISC and RISC processors. (8)

(ii) With a neat diagram describe the implementation of distributed arbitration. (8)

5.(i) What are the different input and output signals of a DMA controller? Why are the read and write control signals are bidirectional? Under what condition and for what purpose they are used as inputs and outputs? (10)

(ii) Discuss the DMA driven data transfer technique. (6)

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