MUTHAYAMMAL ENGINEERING COLLEGE

(An Autonomous Institution)

(Approved by AICTE, New Delhi, Accredited by NAAC & Affiliated to Anna University)
Rasipuram - 637 408, Namakkal Dist., Tamil Nadu.

Estd. 2000

Department of Biomedical Engineering
Question Bank - Academic Year (2021-22)

Course Code & Course Name : 19BMC03& Digital Electronics

Unit-I: BASIC CONCEPTS OF DIGITAL SYSTEMS AND LOGIC FAMILIES

Part-A (2 Marks)

1. Prove that x + xy = x
2. Convert 736_8 into an equivalent binary number.
3. Given the two binary numbers X = 1010100 and Y = 1000011, perform the subtraction Y - X using 2s complements.
4. Which gates are called as the universal gates? What are its advantages?
5. How to represent a positive and negative sign in computers
6. State Duality principle
7. State DeMorgan's theorem
8. List out the advantages and disadvantages of K-map method
9. Give the steps to convert gray code to binary code.
10. Convert Y=A+BC'+AB+A'BC into canonical form.

Part-B (16 Marks)

1. State the postulates of Boolean algebra and Find a Min SOP for f = b'c'd + bcd + acd' + a'b'c + a'bc'd (16)
2. Find an expression for the following function using Quine McCluscky method F= ∑m (0, 2, 3,5,7,9,11,13,14,16,18,24,26,28,30) and Draw the logical circuit of the minimal expression. (16)
3. Simplify the Boolean function F(A,B,C,D) = ∏ M (1,3,7,11,15) + ∏d (0,2,5) .if don'tcare conditions are not taken care, What is the simplified Boolean function .What are your comments on it? Implement both circuits (16)

4.(i). Find the F(A,B,C,D) = ∑m(1,4,6,10) + ∑d (0,11) using K-Map method and Draw the logical circuit of the minimal expression. (8)

(ii). Find the F(W,X,Y,Z) =∑m (1,4,6,7,8,9,10,11,15) using K-Map method and Draw the logical circuit of the minimal expression. (8)

5. Simplify the following function using tabulation method Y(a.b,c,d) = ∑m (0,1,2,5,6,8,9,10) +∑d(7,14) and implement logical gates. (16)

Unit-II: COMBINATIONAL CIRCUITS

Part-A (2 Marks)

1. Define Combinational circuit.
2. Design procedure for combinational circuits.
3. Write the logic equation for half adder.
4. Draw the half sub tractor.
5. Illustrate 4 bit Binary parallel adder?
6. What do you mean by comparator?
7. Define Multiplexing.
8. Write the application for parity checker and parity generator.
9. What is decoder?
10. Difference between decoder and demux.

Part-B (16 Marks)

1.(i).	Design a 2 bit magnitude comparator	(8)
(ii).	Explain the working of carry look ahead adder	(8)
2.(i).	Realize a BCD to Excess 3 code conversion circuit starting from its truth table	(8)
(ii).	Design a full Adder using 2-half adder	(8)
3.(i).	Design a 1X4 De-multiplexer circuit	(8)
(ii).	Implement the following Boolean function F= $\sum$m (0,3,5,8,9,10,12,14). Using 8:1 Mux	(8)
4.(i).	Explain in detail about parity generator and parity cheker	(8)
(ii).	Translates from Excess 3 to BCD 8421 code.	(8)
5.(i).	Design Encoder and implement logical diagram.	(8)
(ii).	Implement the following Boolean function using Mux F(a.b,c,d) = $\sum$m (0,1,3,4,8,9,15)	(8)

Unit-III: SEQUENTIAL CIRCUITS

Part-A (2 Marks)

1. Give the comparison between combinational circuits and sequential circuits.
2. Define race around condition.
3. Write the excitation table for SR FF.
4. Define rise time.
5. Short notes on skew and clock skew.
6. Write the characteristic equation of JK FF.
7. How the lock-out condition can be avoided?
8. How many filp flops are needed for a mod 60 counter?

9. What is shift register? and its types.
10. What is the use of ring counter?

Part-B (16 Marks)

1.(i). Write the characteristic table and characteristic equation of SR and D Filp flop. (8)

(ii). Explain the characteristic table and characteristic equation of JK and T Filp flop. (8)

2.(i). Explain the working of BCD Ripple Counter with the help of state diagram and logic diagram. (8)

(ii). Design mod-10 synchronous counter using JK Flip Flops. (8)

3.(i). Explain the shift registers and its types. (8)

(ii). Explain the universal shift registers. (8)

4.(i). With neat diagram explain master / slave JK-flip flops. (8)

(ii). Summarize the design procedure for Synchronous Sequential circuit. (8)

5.(i). Design a Ring counter and explain in detail. (8)

(ii). Design a Johnson counter and explain in detail. (8)

Unit-IV: SYNCHRONOUS AND ASYNCHRONOUS SEQUENTIAL CIRCUITS

Part-A (2 Marks)

1. Distinguish between synchronous sequential circuits asynchronous sequential circuits.
2. Distinguish mealy and moore models.
3. Define state assignment.
4. Short notes on state reduction.
5. What is meant by excitation table?
6. State the types of sequential circuits.
7. What is meant by Race?
8. Distinguish between fundamental mode and pulse mode operation of asynchronous sequential circuits.
9. What is Hazards? and its types.
10. How to eliminate the hazard?

Part-B (16 Marks)

1. An asynchronous sequential circuit is described by the following excitation and function. $X=(Y_1Z_1'W2)X+(Y_1'Z_1W_2')$ $S=X'$

(a) Draw the logic diagram of the circuit (4)

(b) Derive the transition table & output map (4)

(c) Describe the behavior of the circuit (4)

(b) Explain the fundamental & pulse mod asynchronous sequential circuit. (4)

2.(i).	Explain Essential, Static and Dynamic hazards in digital circuit. Given Hazards free realization for following Boolean function. $F(I,J,K,L)=\Sigma(1,3,4,5,6,7,9,11,15)$	(8)
(ii).	Explain in detail Race Free State assignment.	(8)
3.(i).	Summarize the design procedure for asynchronous sequential circuit	(8)
(ii).	Give examples for cirtical race & cycle and explain.	(8)
4.(i).	Write short notes on hazards and its types.	(8)
(ii).	What is the objective of state assignment in asynchronous circuit? Give hazard – free realization for the following Boolean function $f(A,B,C,D) = M(0,2,6,7,8,10,12)$	(8)
5.(i).	Design a synchronous sequential sequence 0,1,2,3,4,5,6,0.	(8)
(ii).	Explain Hazards free combinational circuits.	(8)

Unit-V: LOGIC FAMILIES AND PROGRAMMABLE DEVICES

Part-A (2 Marks)

1. What are the types of logic families?
2. Draw the CMOS inverter circuit?
3. What is mean by PLDs?
4. Mention the applications of PLA.
5. List the applications of PAL.
6. Write the applications of FPGA.
7. Define Fan in.
8. State Fan out.
9. How the Propagation delay occurs.
10. State Tristate gate.

Part-B (16 Marks)

1.	Design a BCD to Excess-3 code converter and implement using suitable PLA.	(16)
2.	Implement the following Boolean functions using PAL	
	$W(A,B,C,D) = \sum m(0,2,6,7,8,9,12,13)$	(4)
	$X(A,B,C,D) = \sum m(0,2,6,7,8,9,12,13,14)$	(4)
	$Y(A,B,C,D) = \sum m(2,3,8,9,10,12,13)$	(4)
	$Z(A,B,C,D) = \sum m(1,3,4,6,9,12,14)$	(4)
3.	Explain the working of 2 input TTL totem-pole NAND gate circuit.	(16)
4.(i)	Draw the schematic and explain the operation of a CMOS inverter.	(8)
(ii)	Explain the Architecture of FPGA	(8)
5.	Explain the structures of PLA and PAL	(16)

Course Faculty **HoD**