MUTHAYAMMAL ENGINEERING COLLEGE

(An Autonomous Institution)

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Rasipuram - 637 408, Namakkal Dist., Tamil Nadu.

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IQAC

MUST KNOW CONCEPTS

MKC

MCA

2021-22

Course Code & Course Name : **21CAB01 & Computer Organization and Architecture**

Year/Sem/Sec : **I / I / -**

S.No.	Term	Notation (Symbol)	Concept / Definition / Meaning / Units / Equation / Expression	Units
Unit-I : Digital Fundamentals				
1.	Computer Architecture	--	It is concerned with the structure and behavior of the computer.	I
2.	Computer Organization	--	It describes the function and design of the various units of digital computer that store and process information.	I
3.	Number System	--	It is defined as a system of writing to express numbers.	I
4.	Decimal number system	--	Composed of ten symbols (0, 1, 2, 3, 4, 5, 6, 7, 8, 9) known as Base 10 system.	I
5.	Binary number system	--	Composed of two symbols (0,1) also called as Base 2 system.	I
6.	Octal number system	--	Composed of eight symbols (0,1,2,3,4,5,6,7) also known as the Base 8 System.	I
7.	Hexadecimal number system	--	Composed of 16 symbols (digits 0-9 & letters A,B,C,D,E,F) known as Base 16 system.	I
8.	Boolean Algebra	--	Used to simplify the design the logic circuits and involves lengthy mathematical operations.	I
9.	Boolean Function	--	Algebraic expression formed using constant, binary variables and basic logic operation symbols.	I
10.	Demorgan's First Theorem	--	States that complement of a product is equal to be sum of the complements.	I
11.	Demorgan's Second Theorem	--	States that complement of a sum equal to product of the complements.	I
12.	Sum of Product	--	Logical sum of two or more logical product terms is called sum of product.	I
13.	Product of Sum	--	Logical product of two or more logical sum terms is called product of sum.	I

14.	Minterm	--	A product term containing all k-variables of function in either complemented or uncomplemented form.	I
15.	Maxterm	--	A sum term containing all k-variables of function in either complemented or uncomplemented form.	I
16.	Karnaugh map	--	Technique provides a systematic method for simplifying and manipulating switching expressions.	I
17.	Quine-McCluskey Method	--	Tabular method that employs a systematic, step by step procedure to produce a simplified form for function with any no. of variables.	I
18.	Logic Gates	--	It is an electronic circuit which makes logical decisions.	I
19.	AND gate	--	An electronic circuit that gives a high output (1) only if all its inputs are high. A dot (.) is used to show the AND operation.	I
20.	OR gate	--	An electronic circuit that gives a high output (1) if one or more of its inputs are high. A plus (+) is used to show the OR operation.	I
21.	NOT gate	--	An electronic circuit that produces an inverted version of the input at its output. It is also known as an inverter.	I
22.	NAND gate	--	Gate which is equal to an AND gate followed by a NOT gate. The outputs of all NAND gates are high if any of the inputs are low.	I
23.	NOR gate	--	Gate which is equal to an OR gate followed by a NOT gate. The outputs of all NOR gates are low if any of the inputs are high.	I
24.	Exclusive OR gate	--	An XOR gate implements an exclusive OR, i.e., a true output result occurs if one – and only one – of the gate's inputs is true.	I
25.	Exclusive NOR Gate	--	It is a digital logic gate whose function is the logical complement of the exclusive OR gate (XOR gate). It means the output of the XOR gate is inverted in the XNOR gate.	I
Unit-II : Combinational and Sequential Circuits				
26.	Combinational Circuit	--	The circuit output at any time depends only on the input values at that time.	II
27.	Sequential Circuit	--	The output at any time depends on the present input values as well as the past output values.	II

28.	Half adder	--	The logic circuit that performs the addition of two bits is a half adder.	II
29.	Full adder	--	The circuit that Performs the addition of three bits is a full adder.	II
30.	Half Subtractor	--	It is a combinational circuit which is used to perform subtraction of two bits.	II
31.	Full Subtractor	--	It is a combinational circuit that performs subtraction involving three bits.	II
32.	Encoder	--	It is a combinational logic circuit that converts an active input signal into a coded output signal. Perform inverse operation of decoder.	II
33.	Decoder	--	It is a combinational logic circuit that converts a coded output signal into active output signal. Perform inverse operation of encoder.	II
34.	Multiplexer	--	A digital Multiplexer (data selector) is a combinational circuit that selects binary information from one of many input lines and directs it to a single output	II
35.	Demultiplexer	--	A Demultiplexer (data distributor) is a combinational circuit that receives the information on a single line and transmits this information on one of 2nd possible output lines.	II
36.	Magnitude Comparator	--	It is a special combinational circuit that compares the magnitude of two binary numbers.	II
37.	Synchronous sequential circuit	--	In synchronous sequential circuits, signals can affect the memory elements only at discrete instant of time.	II
38.	Asynchronous sequential circuit	--	In asynchronous sequential circuits change in input signals can affect memory element at any instant of time.	II
39.	Flip flop	--	The basic unit for storage is flip flop. A flip-flop maintains its output state either at 1 or 0 until directed by an input signal to change its state.	II
40.	Present state	--	The information stored in the memory elements at any given time defines the present state of the sequential circuit.	II
41.	Next State	--	The present state and the external inputs determine the outputs and the next state of the sequential circuit.	II
42.	D flip-flop	--	In D flip-flop, during the occurrence of clock pulse if D=1, the output Q is set and if D=0, the output is reset.	II
43.	Master-Slave Flip-flop	--	It consists of two flip-flops where one circuit serves as a master and the other as a slave.	II
44.	Race Around Condition	--	In JK flip-flop output is fed back to the	II

			input. if both J and K are high then output toggles continuously.	
45.	Edge Triggering		It is a type of triggering that allows a circuit to become active at the positive edge or the negative edge of the clock signal.	II
46.	Level Triggering	--	It is a type of triggering that allows a circuit to become active when the clock pulse is on a particular level.	II
47.	Binary Counter	--	A sequential circuit consisting of a set of flip flops connected in a suitable manner to count the sequence of input pulses presented to it in digital form.	II
48.	Asynchronous counter	--	In asynchronous counter, each flip flop is triggered by the output from the previous flip flop which limits its speed of operation.	II
49.	Synchronous counter	--	In synchronous counter, the clock input of the flip-flops are all clocked together at the same time with the same clock signal.	II
50.	Shift Register	--	It is a type of digital circuit using a cascade of flip flops where the output of one flip-flop is connected to the input of the next.	II
Unit-III : Basic Structure of Computers				
51.	Control Unit	--	Acts as the nerve center, that coordinates all the computer operations. It issues timing signals that governs the data transfer.	III
52.	Cache Memory	--	A small memory between CPU and main memory is called cache. The speed is equal to the CPU.	III
53.	ROM (Read Only Memory)	--	It is a non-volatile memory that contains permanent data.	III
54.	RAM (Random Access Memory)	--	It is a volatile memory that contains temporary data that can be accessed at high speed.	III
55.	Interrupt	--	An interrupt is a request from an I/O device for service by the processor.	III
56.	Bus	--	A group of lines that serves as a connecting path for several devices is called a bus.	III
57.	Execution Time	--	Response time also called execution time. The total time required for the computer to complete a task.	III
58.	CPI (Clock Cycles Per Instruction)	--	The term Clock Cycles Per Instruction, which is the average number of clock cycles each instruction takes to execute.	III

59.	Processor Time	--	The periods during which the processor is active is called processor time of a program.	III
60.	MIPS(Million Instruction Per Second)	--	The rate at which the instructions are executed at a given time.	III
61.	Throughput Rate	--	The rate at which the total amount of work done at a given time.	III
62.	Program	--	It is a set of instructions that specify the operations, operands and the sequence by which processing has to occur.	III
63.	Instruction Code	--	It is a group of bits that instruct the computer to perform a specific operation.	III
64.	Operation Code	--	It is a group of bits that define operations as add, subtract, multiply, shift and complement etc.	III
65.	Straight-line Sequencing	--	The CPU control circuitry automatically proceed to fetch and execute instruction, one at a time in the order of the increasing addresses.	III
66.	Addressing Modes	--	The different ways in which the location of an operand is specified in an instruction.	III
67.	Immediate Addressing	--	The operand is given explicitly in the instruction.	III
68.	Direct Addressing	--	Effective address of the operand is given in the address field of the instruction.	III
69.	Indirect Addressing	--	It tells the processor where to go to find the address of the operand.	III
70.	Index Addressing	--	The effective address of an operand is generated by adding a constant value to the contents of a register.	III
71.	Pointer	--	The register or memory location that contains the address of an operand.	III
72.	Pipelining	--	Several instructions are performed simultaneously to reduce the overall processing time, the processing called instruction pipelining.	III
73.	RTN(Register Transfer Notation)	--	It is way to specify the behavior of digital synchronous circuit.	III
74.	RISC (Reduced Instruction Set Computer)	--	It is a microprocessor designed to perform a smaller number of computer instruction operate at high speed.	III
75.	CISC (Complex Instruction Set Computer)	--	It supplies a large number of complex instructions at the assembly language level.	III
Unit-IV : Processor Design				
76.	CPU (Central Processing Unit)	--	Brain of the processor. Executes instructions along with the computation required to determine addressing.	IV

77.	Data Buffer	--	Bidirectional device that holds outgoing data until memory bus is ready for it.	IV
78.	I/O Ports	--	These ports represent the device interfaces that have been incorporated into the processor's hardware.	IV
79.	Front Side Bus(FSB)	--	It is an electrical pathway on a computer's motherboard, which connects the various hardware components.	IV
80.	ALU (Arithmetic and Logic Unit)	--	It is a collection of logic circuits designed to perform arithmetic and logic operations.	IV
81.	Data path		The registers, the ALU and the interconnecting bus are collectively referred to as the data path.	IV
82.	Processor Clock	--	All operations and data transfers within the processor take place within time periods defined by the processor clock.	IV
83.	Instruction Decoder	--	It receives the instruction from memory interprets the value to see what instruction is to be performed.	IV
84.	Registers	--	Used to store data, address and flags that are in use by the CPU.	IV
85.	Clock Speed	--	It is the rate at which a processor can complete a processing cycle measured in Mega or Gigahertz.	IV
86.	Multiphase Clocking	--	Data transfers may use both the rising and falling edges of the clock.	IV
87.	Register File	--	All general purpose registers are combined into a single block called register file.	IV
88.	Control Word	--	It is a word whose individual bits represent the various control signal.	IV
89.	Hardwired Control	--	It can be defined as sequential logic circuit that generates specific sequences of control signal in response to externally supplied instruction.	IV
90.	Micro programmed Control	--	A micro programmed control unit is built around a storage unit is called a control store where all the control signals are stored in a program like format.	IV
91.	Parallelism in Microinstruction.	--	The ability to represent maximum number of micro operations in a single microinstruction.	IV
92.	Structural Hazard	--	It occurs when two activities require the same resource simultaneously.	IV
93.	Pipeline Hazard	--	Any condition that causes the pipeline to stall is called hazard. They are also called as stalls or bubbles.	IV

94.	Data Hazard	--	Any condition in which either the source or the destination operands of an instruction are not available at the time.	IV
95.	Instruction or Control Hazard	--	The pipeline may be stalled because of a delay in the availability of an instruction.	IV
96.	Side Effect	--	When a location other than one explicitly named in an instruction as a destination instruction is said to have a side effect.	IV
97.	Branch Penalty	--	The time lost as a result of a branch instruction is often referred to as branch penalty.	IV
98.	Branch Folding	--	When the instruction fetch unit executes the branch instruction concurrently with the execution of the other instruction, then this technique is called branch folding.	IV
99.	Delayed Branching	--	The instructions in the delay slots are always fetched and they are arranged such that they are fully executed whether or not branch is taken.	IV
100.	Super Scalar Processor	--	The processor which is capable of achieving an instruction execution throughput of more than one instruction per cycle.	IV
Unit-V :Memory, I/O System and Parallel Processing				
101.	Virtual Memory	--	It permits the user to write a large programs as if the user has large main memory equal to that of the size of the auxiliary memory.	V
102.	Virtual Address	--	In virtual memory, the binary addresses that the processor issues for either instructions or data called virtual or logical addresses.	V
103.	Memory Latency	--	The term memory latency is used to refer to the amount of time it takes to transfer a word of data to or from the memory.	V
104.	Static Memories	--	Memories that consist of circuits capable of retaining their state as long as power is applied are known as static memories.	V
105.	Memory Access Time	--	It is the time taken by the memory to supply the contents of a location, from the time, it receives “READ”.	V
106.	Memory Cycle Time	--	It is defined as the minimum time delay required between the initiation of two successive memory operations.	V

107.	Hit Ratio	--	The performance of cache memory is frequently measured in terms of a quantity called hit ratio.	V
108.	Hit	--	When the CPU refers to memory and finds the word in cache, it is said to produce a hit.	V
109.	Miss	--	If the word is not found in cache, then it is in main memory and it counts as a miss.	V
110.	Page Fault	--	It is an event that occurs when an accessed page is not present in main memory.	V
111.	Associative or Content Addressable Memory	--	A memory unit accessed by contents.	V
112.	Locality of Reference	--	Many instructions in localized areas of the program are executed repeatedly during some time period.	V
113.	Associative Mapping	--	The tag bits of an address received from the processor are compared to the tag bits of each block.This is called the associative mapping.	V
114.	Least Recently Used(LRU)Block	--	When a block is to be overwritten, it is sensible to overwrite the one that has gone the longest time without being referenced. This block is called the Least recently Used (LRU) block.	V
115.	Physical Address	--	Physical address is an address in main memory.	V
116.	System Space	--	It is convenient to assemble the operating system routines into the virtual address space, called the system space.	V
117.	User Space	--	It is separated from the virtual space in which the user application programs reside is called the user space.	V
118.	Programmed I/O	--	Data transfer to and from peripherals may be handled using this mode.	V
119.	Interrupt Initiated I/O	--	This mode uses an interrupt facility and special commands to inform the interface to issue the interrupt command.	V
120.	Direct Memory Access. (DMA)	--	A modest increase in hardware enables an IO device to transfer a block of information to or from memory without CPU intervention.	V
121.	DMA Controller	--	The I/O device interface control circuit that is used for direct memory access is known as DMA controller.	V

122.	Interrupt	--	It is an event that causes the execution of one program to be suspended and the execution of another program to begin.	V
123.	Vectored Interrupts.	--	In order to reduce the overhead involved in the polling process, a device requesting an interrupt may identify itself directly to the CPU.	V
124.	I/O Interface	--	It provides a method for transferring binary information between internal storage, such as memory and CPU registers, and external I/O devices.	V
125.	Memory Mapped I/O	--	In Memory mapped I/O, there is no specific input or output instructions. The CPU can manipulate I/O data residing in interface registers.	V
Placement Questions				
126.	Page Frame	--	An area in the main memory that can hold one page is called page frame.	
127.	Snooping Cache	--	It is the process where individual caches monitor address lines for accesses to memory locations that they have cached.	
128.	Wait State	--	It means that the computer processor experiences a delay when accessing a device or an external memory that is slow in its response.	
129.	RAID (Redundant Array of Independent Disks)	--	It refers to the hard drives connected and set up in ways to help accelerate or protect the performance of a computer's disk storage.	
130.	Direct Mapping	--	Direct mapping, the RAM is used to store data and some of the data is stored in the Cache.	
131.	MESI	--	MESI stands for the four states of the cache blocks, which are Modified, Exclusive, Shared and Invalid.	
132.	Software Interrupts	--	It can occur only during the execution of an instruction. They can be used by a programmer to cause interrupts.	
133.	Snooping Protocol	--	It maintains cache coherency in symmetric multiprocessing environments.	
134.	Horizontal Micro Code	--	It contains the control signal without any intermediary. It contains a lot of signals and hence due to that the number of bits also increases.	
135.	Chopping	--	It is a simple way to truncate or remove the guard bits and make no changes in the retained bits.	
136.	Branch Prediction	--	It is a technique for reducing the branch penalty associated with conditional branches is to attempt to predict whether	

			or not a particular branch will be taken.	
137.	Exceptions	--	Exceptions are also known as interrupt. An unscheduled event that disrupts program execution.	
138.	Word Line	--	Memory cells are usually organized in the form of an array. Each row of cells constitutes a memory word, and all cells of a row are connected to a common line called word line.	
139.	Memory Bandwidth	--	If the performance measure is defined in terms of the number of bits or bytes that can be transferred in one second, then the measure is called memory bandwidth.	
140.	Double-data-rate SDRAM	--	If a device transfer data on both edges of the clock, their bandwidth is essentially doubled for long burst transfers. Such devices are called (DDR SDRAM) double-data-rate SDRAM.	
141.	SCSI	--	Small computer system interface can be used for all kinds of devices including RAID storage subsystems and optical disks for large- volume storage applications.	
142.	I/O Channel	--	It is actually a special purpose processor, also called peripheral processor. The main processor initiates a transfer by passing the required information in the input output channel.	
143.	Data Striping	--	A single large file is stored in several separate disk units by breaking the file up into a number of smaller pieces and storing these pieces on different disks.	
144.	Program Counter (PC) Register	--	It keeps track of the execution of the program. It contains the memory address of the instruction currently being executed.	
145.	Translation-Look aside Buffer (TLB)	--	It is a cache that keeps track of recently used address mappings to try to avoid an access to the page table.	
146.	Rotational Latency	--	Also called rotational delay, is the time required for the desired sector of a disk to rotate under the read/write head, usually assumed to be half the rotation time.	
147.	Direct-mapped Cache	--	It is a cache structure in which each memory location is mapped to exactly one location in the cache.	
148.	MAR (Memory Address Register)	--	It is used to hold the address of the location to or from which data are to be transferred.	

149.	MDR(Memory Data Register)	--	It contains the data to be written into or read out of the addressed location.	
150.	Instruction Register (IR)	--	Instruction Register (IR) contains the instruction being executed.	

Faculty Prepared **Signature**

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