MUTHAYAMMAL ENGINEERING COLLEGE

(An Autonomous Institution)

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Rasipuram - 637 408, Namakkal Dist., Tamil Nadu

MKC

ECE

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Must Know Concepts (MKC)

Course Code & Course Name	19ECC12 – VLSI CIRCUIT DESIGN
Year/Sem/Sec	III / V /A,B & C

UNIT I MOS TRANSISTOR THEORY

S.No	Term	Notation (Symbol)	Concept/Definition/Meaning/Units/Equation/ Expression	Units
1	VLSI	-	An integrated circuit (IC) by combining thousands of transistors into a single chip.	-
2	FET	-	To control the conductivity of a particular channel in a semiconductor material.	-
3	Enhancement Mode	-	The device that is normally cut-off with zero gate bias..	-
4	Depletion Mode	-	The Device that conduct with zero gate bias.	-
5	different layers in MOS transistors	-	Drain , Source & Gate	-
6	Channel pinched –off	-	If a large Vds is applied this voltage with deplete the Inversion layer .This This causes pinch off.	-
7	BiCMOS Technology	-	It is the combination of Bipolar technology & CMOS technology	-
8	pull down device	-	To pull the output voltage to the lower supply voltage usually 0V.	-
9	pull up device	-	To pull the output voltage to the upper supply voltage usually VDD.	-
10	Stick Diagram	-	To convey information through the use of color code. Also it is the cartoon of a chip layout.	-
11	Uses of Stick diagram	-	It can be drawn much easier and faster than a complex layout. These are especially important tools for layout built from large cells.	-
12	Threshold voltage	-	To create a conducting path between the source and drain terminals.	-
13	NMOS		Transistors are turned on or off by the movement of electrons.	-
14	PMOS	-	Transistors are turned on or off by the movement of holes.	-
15	Semiconductor	-	Semiconductors are materials which have a conductivity between conductors and nonconductors or insulators.	-

16	CMOS	-	CMOS in which both n-channel MOS and p-channel MOS are fabricated in the same IC. .	-
17	Twin tub	-	Provides the basis for separate optimization of p type and n type transistors.	-
18	SOI	-	Fabrication of silicon semiconductor devices in a layered silicon–insulator–silicon substrate.	-
19	BiCMOS	-	BiCMOS is a technology that integrates bipolar and CMOS together.	-
20	Channel	-	The current flow between source and drain in FET.	-
21	Body effect	-	The voltage difference between the substrate and the source of MOS transistor.	-
22	Gate	-	The width of the channel is controlled by the voltage on an electrode.	-
23	Source	-	The charge carriers enter the channel at source	-
24	Drain	-	The charge carriers exit via the drain	-
25	IC	-	It can hold anywhere from hundreds to millions of transistors, resistors, and capacitors.	-
26	Cutoff region	-	This is the region in which transistor tends to behave as an open switch	-
27	Linear	-	Linear region is a part of the active region of a transistor.	-
28	Saturation	-	This is the region in which transistor tends to behave as a closed switch.	-
29	Aspect ratio	-	The ratio of width and length of gate.	-
UNIT II MOS CIRCUITS AND DESIGN				
30	Channel length modulation	-	Shortening of the length of the i nverted channel region with increase in drain bias.	-
31	Mobility variation	-	carriers drift in the substrate material	-
32	Noise margin	-	To determine allowable noise voltage on the input of a gate.	-
33	Scaling	-	The dimensions of MOSFETs, is commonly referred to as scaling.	-
34	Delay	-	Time between trigger on any pin and the change in signal level of the same.	-
35	Sheet resistance	-	Measure of resistance of thin films that are nominally uniform in thickness.	-
36	Need for design rules	-	To build reliably financial circuits in as small an area as possible. They represent a compromise between performance and yield.	-
37	Lambda layout design rules	-	minimum feature sizes and minimum allowable feature separations are started in terms of a λ	-
38	Types of layout design rules	-	a) Lambda design rules b) Micro rules	-
39	Various issues in Technology CAD	-	a. Design Rule Checking (DRC) b. Circuit Extraction	-

40	Device modeling	-	SPICE provides a wide variety of MOS transistor models with various tradeoffs .	-
41	Power dissipation	-	The rate at which energy is taken from the source (Vdd) and converted into heat .	-
42	T_{PHL} and T_{PLH} in terms of C_{load}.	-	T_{PHL} =0.69 X RnC_l T_{PLH}=0.69 X RpC_l	-
43	Transistor sizing problem	-	Delay of combinational circuit can be controlled by varying the sizes of transistors.	-
44	Elmore delay	-	It estimates the delay of a RC ladder and a supply multiplied by the capacitor on the node.	-
45	DRC(Design Rule Checking)	-	To determine if chip layout satisfies a number of rules as defined by the semiconductor manufacturer.	-
46	Design rules	-	It is the communication link between the designer specifying requirements and the fabricator.	-
47	Moore's law	-	Moore's law states that the number of transistor would double every 18 months.	-
48	Variety of Integrated Circuits	-	More Specialized Circuits Application Specific Integrated Circuits(ASICs) Systems-On-Chips	-
49	Oxidation	-	Oxidation of silicon is achieved by heating silicon wafers in an oxidizing atmosphere	-
50	Diffusion	-	To introduce impurity atoms (dopants) into silicon to change its resistivity.	-
51	Advantages of CVSL family	-	All the logic is performed with nMOS transistors, thus reducing the input capacitors.	-
52	Ratioed logic	-	A ratioed logic which uses a grounded pMOS load is referred to as a pseudo-nMOS gate.	-
		UNIT III	**SUBSYSTEM DESIGN & LAYOUT**	
53	Dynamic CMOS logic	-	The temporary storage of signal values on the capacitance high impedance nodes.	-
54	Static power dissipation	-	Due the leakage current through normally off the transistor is called static power dissipation	-
55	Dynamic power dissipation	-	Due to circuit switching to charge and discharge the output load capacitance at a particular node .	-
56	short circuit power dissipation	-	During switching, both NMOS and PMOS transistors will conduct simultaneously	-
57	CMOS Domino logic	-	CMOS-based evolution of the dynamic logic techniques based on either PMOS or NMOS transistors.	-
58	Pass transistor	-	It reduces the count of transistors used to make different logic gates, by eliminating redundant transistors	-
59	Transmission gate	-	Electronic element that will selectively block or pass a signal level from the input to the output.	-
60	Static CMOS logic	-	The output is always strongly driven due to it always being connected to either VCC or GND	-
61	Dynamic CMOS logic	-	In dynamic CMOS output is taken across a capacitor .Output is not always connected to supply or gnd.	-

62	Combinational logic	-	The output is a pure function of the present input only.	-
63	Sequential logic	-	The output depends not only on the present value of its input signals.	-
64	Two phase clocking	-	Clock signals distributed on 2 wires, each with non-overlapping pulses.	-
65	Latch	-	Latch is level-triggered (outputs can change as soon as the inputs changes) .	-
66	Flip flop	-	Flip-Flop is edge triggered (only changes state when a control signal goes from high to low or low to high).	-
67	Clock skew	-	The clock signal arrives at different components at different times.	-
68	Multiplexer	-	It is a device allowing one or more low-speed input signals to be selected, combined and transmitted at a higher speed .	-
69	Metastability	-	Metastability is an unknown state it is neither zero nor one.	-
70	Synchronizers	-	Synchronizers are used to reduce metastability and ensure synchronization between asynchronous input and synchronous system.	-
71	Pipelining	-	It is a designing technique used to increase the operation of data paths in digital processor.	-
72	clock jitter	-	True periodicity of a presumably periodic signal, often in relation to a reference clock signal.	-
73	Register	-	A register is usually realized as several flip-flops with common control signals that control the movement of data to and from the register.	-
74	Counter	-	The output of the counter can be used to count the number of pulses.	-
75	Latch up	-	Short circuit formed between power and ground rails in an IC leading to high current and damage to the IC.	-
UNIT IV PROGRAMMABLE LOGIC DEVICES				
76	FPGA	-	It is a programmable logic device that supports implementation of relatively large logic circuits.	-
77	types of gate arrays in ASIC	-	Channeled gate arrays Channel less gate arrays Structured gate arrays	-
78	Full custom	-	logic cells, circuits or layout specifically for one ASIC	-
79	Semi custom	-	Standard cell libraries are themselves designed using full-custom design techniques.	-
80	cell-based ASIC (CBIC)	-	The standard cell areas also called flexible blocks in a CBIC are built of rows of standard cells	-
81	Macros	-	The logic cells in a gate-array are often called macros.	-
82	programmable Interconnects	-	In a PAL, the device is programmed by changing the characteristics if the switching element	-
83	programmable logic array	-	The PLA has programmable connections for both AND and OR arrays.	-

84	programmable logic plane	-	PROM array that allows the signals present on the devices pins to be routed to an output logic macro cell.	-
85	manufacturing lead time	-	It is defined as the time it takes to make an IC not including the design time.	-
86	primitive cell	-	The predefined pattern of transistor on a gate array is the base array.	-
87	anti fuse	-	On application of appropriate programming voltages, the anti fuse is changed permanently to a low resistance structure.	-
88	standard cell design	-	A standard cell is group of transistor and interconnects structures, which provides a Boolean logic function or a storage function.	-
89	Synthesis	-	The process of mathematically transforming the ASIC's register-transfer level (RTL) description into a technology-dependent net list.	-
90	Placement	-	The placer tool assigns locations for each gate in the net list.	-
91	PAL	-	A device has a programmable AND array and fixed connections for the OR array.	-
92	PROM	-	The PROM has a fixed AND array and programmable connections for the output OR gates array.	-
93	CPLD	-	A CPLD contains a bunch of PLD blocks whose inputs and outputs are connected together by a global interconnection matrix.	-
94	Connection boxes	-	Connection boxes, which are a set of programmable links that can connect input and output pins of the CLBs.	-
95	Switch boxes	-	Set of programmable links that can connect wire segments in the horizontal and vertical channels	-
96	Programmable I/O	-	It can be configured either as input buffers, output buffers or input/output buffers.	-
97	PLD	-	Programmable Logic Devices consist of a large array of AND gates and OR gates that can be programmed to achieve specific logic functions.	-
98	FSM	-	A finite state machine may be any model implemented through software or hardware to simplify a complex problem.	-
99	Moore model	-	A state machine which uses only Entry Actions, so that its output depends on the state, is called a Moore model.	-
100	Mealy model	-	A state machine which uses only Input Actions, so that the output depends on the state and also on inputs, is called a Mealy model.	-
UNIT V VERILOG HDL DES IGN PROGRAMMING				
101	Verilog	-	It can be used to model a digital system at many levels of abstraction anging from the algorithmic level to the switch level.	-
102	modeling used in Verilog	-	1. Gate-level modeling 2. Data-flow modeling 3. Switch-level modeling 4. Behavioral modeling	-

103	structural gate-level modeling	-	Gate-level modeling is based on using primitive logic gates and specifying how they are wired together.	-
104	Switch-level modeling	-	Verilog allows switch-level modeling that is based on the behavior of MOSFETs.	-
105	Identifiers	-	Identifiers are names of modules, variables and other objects that we can reference in the design.	-
106	value sets in Verilog	-	Verilog supports four levels for the values needed to describe hardware referred to as value sets.	-
107	Condition in hardware circuits	-	0 Logic zero, false condition 1 Logic one, true condition X Unknown logic value Z High impedance, floating state•	-
108	arithmetic operators	-	* Multiply Two / Divide Two + Add Two - Subtract Two % Modulus Two ** Power (exponent) Two	-
109	Bitwise operator	-	~ Bitwise negation One & Bitwise and Two | Bitwise or Two ^ Bitwise xor Two ^~ or ~^ Bitwise xnor Two ~& Bitwise nand Two ~| Bitwise nor Two	-
110	Gate primitives	-	Primitive logic function keyword provides the basics for structural modeling at gate level.	-
111	blocks in behavioral modeling	-	1. initial block 2. always block	-
112	initial block	-	An initial block executes once in the simulation and is used to set up initial conditions and step-by-step data flow.	-
113	always block	-	An always block executes in a loop and repeats during the simulation.	-
114	conditional statements	-	1. No else statement 2. One else statement 3. Nested if-else-if	-
115	No else statement	-	if ([expression]) true – statement;	-
116	One else statement	-	if ([expression]) true – statement; else false-statement;	-
117	Nested if-else-if	-	: if ([expression1]) true statement 1; else if ([expression2]) true-statement 2; else if ([expression3]) true-statement 3; else default-statement;	-
118	Dataflow modeling	-	Dataflow modeling uses a number of operators that act on operands to produce the desired results.	-

119	Module	-	A module can be an element or Collection of lower level design blocks.	-
120	Instance	-	When a module is invoked, Verilog creates a unique object from the template. Each object has its own name, variables, parameters and I/O interfaces. These objects are called as instances.	-
121	Nets	-	Nets represents connections between hardware elements.	-
122	Data type registers	-	Registers represent data storage elements. They retain value until another value is placed on to them.	-
123	Vectors	-	Register and net data types can be declared as vectors i.e single element that is multiple bit wide.	-
124	Arrays	-	Reg, net, integer, real, real time, time data types can be declared as arrays. Arrays are multiple elements that are 1-bit or n-bits wide.	-
125	Top-down design methodology	-	In top-down methodology, first the top level block is defined and the necessary sub blocks are identified to build the top level block.	-
PLACEMENT QUESTIONS				
1	Why does the vlsi circuit use mosfets instead of bjts?	-	Compared to BJTs, MOSFETs can be made very small as they occupy very small silicon area on IC chip and are relatively simple in terms of manufacturing.	-
2	various factors on which threshold voltage depends	-	The Vt depends on the voltage connected to the Body terminal. It also depends on the temperature.	-
3	steps involved in preventing the metastability	-	Proper synchronizers are used that can be two stage or three stage whenever the data comes from the asynchronous domain.	-
4	different types of skews used in VLSI	-	Global skew Local skew Useful skew	-
5	Chain Reordering	-	Tool available that automate the reordering of the chain to reduce the congestion that is produced at the first stage.	-
6	advantages of IC	-	Size is less High Speed Less Power Dissipation	-
7	“timescale 1 ns/ 1 ps” signifies	-	In Verilog code, the unit of time is 1 ns and the accuracy/precision will be upto 1ps.	-
8	SCR	-	It is a type of rectifier that is controlled by a logical gate signal. It is a 4 layered, 3-terminal device.	-
9	Slack	-	Time delay difference from the expected delay to the actual delay in a particular path.	-

10	Defparam	-	Parameter values can be configured in any module instance in the design.	-
11	LEF	-	It is an ASCII format from cadence design to describe standard cell library.	-
12	DEF	-	It is an ASCII format from cadence design to describe design related information.	-
13	Various yield losses	-	Functional yield losses and Parametric yield losses	-
14	Virtual clock definition	-	To model the I/O timing specification	-
15	MTBF? What it signifies?	-	•MTBF-Mean Time Before Failure •Average time to next failure	-
16	Is verilog/VHDL is a concurrent or sequential language?	-	Verilog and VHDL both are concurrent languages. Any hardware descriptive language is concurrent in nature.	-
17	Cross talk can be avoided by	-	a. Decreasing the spacing between the metal layers b. Shielding the nets c. Using lower metal layers d. Using long nets	-
18	What is the goal of CTS?	-	a. Minimum IR Drop b. Minimum EM c. Minimum Skew d. Minimum Slack	-
19	What is SDC constraint file contains?	-	Clock definitions Timing exception-multicycle path, false path Input and Output delay	-
20	How to find total chip power?	-	Total chip power=standard cell power consumption, Macro power consumption pad power consumption.	-
21	What are the problems faced related to timing?	-	Prelayout: Setup, Max transition, max capacitance, Post layout: Hold	-
22	How did you resolve the setup and hold problem?	-	Setup: upsize the cells Hold: insert buffers	-
23	significance of negative slack	-	negative slack==> there is setup voilation==> deisgn can fail	-
24	track assignment	-	Second stage of the routing wherein particular metal tracks (or layers) are assigned to the signal nets.	-
25	clock trees	-	Distribution of clock from the clock source to the sync pin of the registers.	-

LABORATORY QUESTIONS				
1	Intrinsic Semiconductor	-	The pure Silicon is known as Intrinsic Semiconductor.	-
2	Extrinsic Semiconductor	-	When impurity is added with pure Silicon, its electrical properties are varied.	-
3	different MOS layers	-	• n-diffusion• p-diffusion• Polysilicon• Metal	-
4	Epitaxy	-	Epitaxy means arranging atoms in single crystal fashion upon a single crystal substrate	-
5	processes involved in photo lithography	-	(1) Masking process (2) Photo etching process	-
6	Purpose of masking in fabrication of IC	-	Masking is used to identify the location in which Ion-Implantation should not take place	-
7	materials used for masking	-	Photo resist, Si02, SiN, Poly Silicon.	-
8	diffusion process	-	Diffusion is a process in which impurities are diffused into the Silicon chip at 1000 ˚C temperature	-
9	Ion-Implantation process	-	It is process in which the Si material is doped with an impurity by making the accelerated impurity atoms to strike the Si layer at high temperature.	-
10	Isolation	-	It is a process used to provide electrical isolation between different components and interconnections.	-
11	Channel-stop Implantation	-	In n-well fabrication, n-well is protected with the resist material. Then Boron is implanted except n-well. The above said process is done using photo resist mask.	-
12	LOCOS	-	LOCOS mean Local Oxidation of Silicon. This is one type of oxide construction	-
13	LDD	-	LDD means Lightly Doped Drain Structures. It is used for implantation of n- region in n-well process.	-
14	steps involved in BiCMOS process	-	Additional masks defining P base region• N Collector area• Buried Sub collector (SCCD)• Processing steps in CMOS process	-
15	Silicide	-	The combination of Silicon and tantaleum is known as Silicide. It is used as gate material in Polysilicon Interconnect.	-

16	Types of Inter connect	-	1. Metal Inter connect 2. PolySilicon Inter connect 3. Local Interconnect.	-
17	demarcation line	-	Demarcation line is an imaginary line used in stick diagram, to separate p-MOS and n-MOS transistors.	-
18	LVS	-	LVS means Layout Versus Schematic. It checks layout against schematic diagram. It is very important to verify layout.	-
19	software used for VLSI design	-	Microwind, Tanner, Hspice, Pspice, Mentor graphics, Xilinx etc…	-
20	RTL	-	RTL stands for Register Transfer Level. It is a high-level hardware description language (HDL)used for defining digital circuits.	-
21	Simulation	-	to verify the functionality of the circuit. a)Functional Simulation: study of ckt's operation b) Timing Simulation :study including estimated delays.	-
22	Synthesis	-	VHDL or VERILOG description to a set of primitives or components(as inFPGA'S) to fit into the target technology.	-
23	Testing	-	A manufacturing step that ensures that the physical device , manufactured from the synthesized design.	-
24	Verification	-	To ensure that the synthesized design, when manufactured, will perform the given I/O function	-
25	how binary number can give a signal?	-	Binary number consists of either 0 or 1, number 1 represents the ON state and number 0 represents OFF state.	-

Faculty Prepared	**HoD**
1. **Dr.U.Saravanakumar/Mrs.P.Subhasundari** 2. **Dr.R.Praveena** 3. **Mrs.S.Punitha**	