MUTHAYAMMAL ENGINEERING COLLEGE

(An Autonomous Institution)

(Approved by AICTE, New Delhi, Accredited by NAAC & Affiliated to Anna University)
Rasipuram - 637 408, Namakkal Dist., Tamil Nadu

Estd. 2000

IQAC

MUST KNOW CONCEPTS

MKC

ECE

2021-2022

Course Code & Course Name : 19ECC07 & Microcontroller Based System Design.

Year/Sem : II/IV

S.No	Term	Notation (Symbol)	Concept/Definition/Meaning/ Units/Equation/Expression	Units
UNIT-I : 8051 MICROCONTROLLER				
1.	Microprocessor	µP	Fetches,decodes and executes instructions.	No units
2.	Microcontroller	µC	Perform one task and execute one specific application.	No units
3.	Microcomputer	-	Computing system designed using a microprocessor as its CPU.	No units
4.	Peripheral Devices	-	Ancillary device used to put information into and get information out of the computer.	No units
5.	Memory	-	ROM permanently storing programs and RAM temporary storage.	No units
6.	Buses		The input, output devices and memory devices are connected to the CPU by groups of lines.	No units
7.	Serial Output Data	SOD	Output line the microprocessor sends output serial data.	No units
8.	Serial Input Data	SID	Input line the microprocessor accepts serial data.	No units
9.	RESET OUT	-	It indicates that the CPU is being reset.	No units
10.	Return	RET	Return is used at the end of a subroutine.	No units
11.	HOLD	-	Requesting the use of the address and data Buses.	No units
12.	Hold Acknowledgement	HLDA	CPU received the Hold request and will relinquish the buses in the next clock cycle.	No units
13.	Accumulator	A	Store 8-bit data and perform arithmetic, logical operations.	No units
14.	Addressing mode	-	Microprocessor identifies the operands for the instruction.	No units

15.	Stack Pointer	SP	Hold the memory address of the next instruction to be executed.	No units
16.	Program Counter	PC	16-bit register which holds the address of the top of stack.	No units
17.	Simplex	-	The data are transmitted in only one direction.	No units
18.	Baud rate	-	The rate at which bits are transmitted.	Bits/sec
19.	Direct Memory Access	DMA	Transfer data to and from a memory subsystem, for high speed data transfer.	No units
20.	Interrupt	-	External signal that causes a microprocessor to jump to a specific subroutine	No units
21.	Two key lock out	-	In key board, If two keys are pressed simultaneously, the first key only recognized.	No units
22.	TRAP	-	Non-maskable, transfer the content of main memory to back up memory.	No units
23.	N key roll over	-	Stores the codes of simultaneous keys pressed in the internal buffer	No units
24.	Assembly Language Program	ALP	The program written with alphanumeric characters.	No units
25.	Mnemonics	-	The program makes use of symbolic opcodes.	No units
UNIT-II :8051 MICROCONTROLLER INTERFACING.				
26.	Program	-	Set of instructions arranged in a sequence to do specific task.	No units
27.	Label	-	Represent the address of an instructions.	No units
28.	Tri-state logic	-	High, Low, High impedance state.	No units
29.	Maskable interrupts	-	An interrupt that can be turned off by the programmer.	No units
30.	Loop	-	Changes the sequence of execution and perform task again.	No units
31.	Indexing	-	Allows programmer to point data stored in sequential memory locations one by one.	No units
32.	Central Processing Unit	CPU	Brain of microcontrollers reading user's programs and executing the expected task .	No units
33.	Data point register	DPTR	16 bit addressing register fetch any 8 bit data from the data memory space.	No units
34.	Program status word	PSW	Keeps current status of the arithmetic, logic operations in different bits.	No units
35.	Timers	-	Timers are used to generate a time delay.	No units

36.	Counters	-	Count events happening outside the microcontroller.	No units
37.	Serial Communication	-	The data is sent one bit at a time from sender to receiver.	No units
38.	Non-Maskable interrupts	-	An interrupt which can be never be turned off.	No units
39.	Set Interrupt Mask	SIM	Used to mask the hardware interrupts.	No units
40.	Read Interrupt Mask	RIM	Used to check whether the interrupt is Masked or not.	No units
41.	Reduced Instruction Set Computer.	RISC	Reduce the execution time by simplifying the instruction set .	No units
42.	Complex Instruction Set Computer	CISC	Minimize no of instructions per program, ignoring the number of cycles per instruction.	No units
43.	Interrupt Enable Register	IE	Holds the programmable bits that enable or disable the interrupts.	No units
44.	Synchronous Transmission	-	Receiver and transmitter work in same speed and could be synchronized.	No units
45.	Interrupt Mask Register	IMR	Stores bits which mask the interrupt lines to be matched.	No units
46.	Cascade Buffer	-	Expand the no of interrupt levels by cascading two or more 8259.	No units
47.	Macros	-	Small routines to replace strings in the program.	No units
48.	Constants Declared	-	Constants are declared in the same way as variables.	No units
49.	Loader	-	Copies program to computer's main memory at load time and begins the program execution at execution time.	No units
50.	Linker	-	Join together several object files into one large object file.	No units
UNIT-III :PIC MICROCONTROLLER				
51.	ASSUME	-	Assigns a logical segment to a physical segment at any given time.	No units
52.	ALIGN	-	Assembler to align the next segment at an address divisible by specified divisor.	No units
53.	Variable	-	Identifier that is associated with first byte of data item.	No units
54.	Pipelining	-	Fetching the next instructions while the current instruction executes.	No units
55.	Non Maskable Interrupt	NMI	Edge triggered input, which causes a type 2 interrupt, Maskable internally by software and transition from low to high.	No units
56.	Effective Address	-	Access a memory location it sends an	No units

			offset value to the BIU.	
57.	Assemble Time	-	Time required to translate assembly code to object code.	No units
58.	String Addressing	-	String instructions to address the source and destination operand/data.	No units
59.	Encapsulation	-	Protect the chip and the inter connect technology to connect the chip electrically to the printed circuit.	No units
60.	Single bit instructions	-	Instructions that are used for single bit operation.	No units
61.	Watch Dog Timer	-	Protect an application in case the controlling microcontroller begins to run execute randomly.	No units
62.	Nesting of Interrupts	-	Interrupts are re-enabled inside an interrupt handler.	No units
63.	Stepper motor	-	Obtain an accurate position control of rotating shafts.	No units
64.	Key bouncing	-	Microprocessor must wait until the key reach to a steady state.	No units
65.	Conversion Time	-	Total time required to convert an analog signal into a digital output.	No units
66.	Memory Segmentation	-	Process of completely dividing the physically available memory into a number of logical segments.	No units
67.	Clock Input	-	Provides the basic timing for processor operation and bus control activity	No units
68.	Multiprogramming	-	If more than one process is carried out at the same time.	No units
69.	Loader	-	Copies program into computer's main memory at load time, begins the program execution at execution time.	No units
70.	Parallel Communication Interface	-	Gets a byte and sends all the bits in that byte simultaneously to the external system.	No units
71.	Interrupt Enable	INTE	Internal flip flop to enable or disable generation of INTR signal.	No units
72.	Interrupt Request	INTR	Output signal to interrupt the CPU to request the next data byte for output.	No units
73.	Interrupt Request Register	IRR	Store all interrupt levels which are requesting services.	No units
74.	In-Service Register	-	Store all the interrupt levels which are being serviced.	No units
75.	Address Latch Enable	ALE	Goes high during first clock cycle of a machine cycle .	No units
UNIT-IV :ARM 32 BIT MICROCONTROLLER				
76.	Addressing	-	Specifying the data to be operated by	

			the instruction	
77.	Direct addressing mode	-	Address of data is specified in the instruction itself.	No units
78.	Immediate addressing mode	-	The data is specified within the instruction itself	No units
79.	Register addressing mode	-	Instruction specifies the name of register in which data is available.	No units
80.	Implicit addressing mode	-	Some instruction operates on the content of accumulator.	No units
81.	Instruction	-	Binary pattern to perform a specific function.	No units
82.	Instruction Set	-	Group of instruction is called Instruction set.	No units
83.	T State	-	One subdivision of the operation performed in one clock period.	No units
84.	Machine Cycle	-	Time required for completing one operation of accessing memory.	No units
85.	Instruction Cycle	-	Time required for completing the execution of an instruction.	No units
86.	Watchdog timer	-	Resets the processor if the software / Program ever malfunctions and deviates from its normal operation	No units
87.	Data segment	DS	16-bit containing address of 64KB segment with program data.	No units
88.	Power on reset	-	Ensure that chip operate only when supply voltage is within specification.	No units
89.	Brown out reset	-	Power supply goes below a specified voltages (4V) it causes PIC to reset.	No units
90.	Analog to digital converter	ADC	Converts analog signal into equivalent digital number.	No units
91.	Subroutine	-	Group of instructions written to perform a specific task.	No units
92.	Look up table	-	System that helps to replace the runtime computations.	No units
93.	Program Status word	PSW	Keeps the current status of arithmetic, logic operations in different bits.	No units
94.	Flags	-	Group of five individual Flip-flops, to know the nature of output.	No units
95.	Stack segment	SS	16-bit register containing address of 64KB segment with program stack.	No units
96.	Half duplex	-	Data are transmitted in both the directions, but not simultaneously.	No units
97.	Full duplex	-	Data are transmitted in both the directions simultaneously.	No units
98.	In service register	ISR	Store all the interrupt levels which are being serviced.	No units

99.	USART	-	Programmable device functions and specification can be determined by writing instructions in its internal registers.	No units
100.	Key Debounce	-	The push button keys when pressed, bounces a few times, closing and opening the contacts before providing a steady reading.	No units
UNIT-V : ARM CORTEX M3 PROGRAMMING				
101.	N-key rollover	-	When a key is depressed, the debounce logic is set.	No units
102.	Oscillator Circuit	-	Generate timing clock signal for operation of circuit using crystal oscillator.	No units
103.	DMA Controller	DMAC	Control data transfer, I/O subsystem and a memory subsystem.	No units
104.	Key Bouncing	-	Microprocessor wait until the key reach to steady state	No units
105.	CALL Instructions	-	Microprocessor automatically stores the 16-bit address of contents of register	No units
106.	Extra segment	ES	16-bit register containing address of 64KB segment, usually with program data.	No units
107.	Code segment	CS	16-bit register containing address of 64 KB segment with processor instructions.	No units
108.	Execution Unit	EU	Executes instructions that have already fetched by BIU..	No units
109.	Base Pointer	BP	It is a 16-bit register pointing to data in stack segment.	No units
110.	Opcode	-	Instruction that identifies a specific operation.	No units
111.	Operand	-	Instruction represents a value on which the instruction acts.	No units
112.	Execute cycle	-	Decode the instruction to perform the work instructed by the instruction	No units
113.	T- Sate	-	The portion of operation performed in one clock period.	No units
114.	Disable Interrupt	-	When this instruction is executed, the interrupts are Disabled.	No units
115.	SWAP	-	Works only on the accumulator swaps the lower nibble and higher nibble	No units
116.	Timer mode	TMOD	Set the various timer operation modes.	No units
117.	Interrupt Service Routine	-	Breaks the normal sequence of execution of instructions & diverts its	No units

			execution to some other program.	
118.	Count register	-	Used as a counter in string manipulation and shift/rotate instructions	No units
119.	Base Register	-	Two 8-bit registers BL and BH, used as a 16-bit register.	No units
120.	Data register	-	Used as a port number in I/O operations.	No units
121.	Low level language	-	Low level language which uses binary 0 and 1.	No units
122.	Operating System	-	The interaction between hardware and software is managed by a set of programs.	No units
123.	Opcode Fetch Cycle	-	Machine cycle executed to fetch the opcode of an instruction stored in memory.	No units
124.	Queue	-	The data structure be accessed of first in and first out.	No units
125.	Libraries	-	Collection of procedures that used in other programs.	No units
Placement Questions				
126.	Various Registers	-	Accumulator register, Temporary register, Instruction register, Stack Pointer, Program Counter	No units
127.	Various Flags	-	Sign flag, Zero flag, Auxiliary flag, Parity flag, Carry flag.	No units
128.	Stack Used In 8051	-	LIFO (Last In First Out) the last stored information retrieved first.	No units
129.	Hardware Interrupts	-	TRAP, RST7.5, RST6.5, RST5.5, INTR.	No units
130.	Quality Factor	-	Reflects the lossness of a circuit.	No units
131.	Stack Pointer Register	-	Sixteen bit register used to point at the stack	No units
132.	Interfacing	-	Hardware software needed to connect devices together.	No units
133.	CISC Processor	-	Minimize the no of instructions per program.	No units
134.	Program counter	-	Holds a location in memory of the next step to be performed.	No units
135.	Trap input	-	Trap responds to both edge sensitive and level sensitive.	No units
136.	Hlt	-	The processor stops functioning buses driven to tri-state.	No units
137.	Hold States	-	The processor goes into hold state but the buses are not driven to tri-state.	No units

138.	Maximum clock frequency 8051	-	5 MHz is the Maximum clock frequency	No units
139.	clock frequency for 8051	-	3 MHz is the maximum clock frequency	No units
140.	Low order Register	-	Flag is called as Low order register	No units
141.	High order Register	-	Accumulator is called as high order register	No units
142.	Nibble	-	4-bit aggregation or half an octet	No units
143.	Cache memory	-	Temporary storage of data and information between main memory and CPU	No units
144.	Load Effective Address	-	Initializing register with an offset address	No units
145.	Ready pin	-	Check whether a peripheral is ready to accept or transfer data	No units
146.	Handshake output	-	Processor will load a data to port	No units
147.	Modulator Programming	-	Breakup large program into manageable unit	No units
148.	Directives	-	Instructions to the assembler concerning the program being assembled	No units
149.	Compiler	-	Translate high level language program into machine code	No units
150.	Memory Mapping	-	Process of interfacing memories to microprocessor	No units

Faculty Team Prepared **Signatures**

1. **Mrs.A.Nivetha**
2. **Dr.R.Praveena**
3. **Mrs.V.Hema**

HoD