MUTHAYAMMAL ENGINEERING COLLEGE

(An Autonomous Institution)

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Rasipuram - 637 408, Namakkal Dist., Tamil Nadu

MKC

MUST KNOW CONCEPTS (MKC)

ECE

2021-2022

Course Code & Course Name	**:**	**19ECE24 & Computer Architecture and Organization**
Year/Sem/Sec	**:**	**III/V/A,B&C**

S.No	Term	Notation (Symbol)	Concept/Definition/Meaning/Units/Equation/ Expression	Units
Unit I	**Introduction to Computer Architecture and Organization**			
1	Digital computer	-	Fast-electronic calculating machine that accepts digitized information from the user, process it according to the sequence of instructions and provides the processed information to the user.	-
2	Computer program	-	The sequence of instructions stored in the internal storage	-
3	CPU	-	The ALU in conjunction with control unit is called central processing unit (CPU)	-
4	ENIAC	-	ENIAC (Electronic Numerical Integrator and Computer is the first electronic computer.	-
5	CPU execution time	-	Time the CPU spends computing for a particular task.	-
6	CPU throughput rate	-	Ratio of number of machine instructions executed per second to the number of machine instructions per program.	-
7	Megaflops	MFLOPS	• It is the performance metric used to assess the super computer performance. • It is the ratio of number of floating-point operations in a program and execution time in micro seconds.	-

8	Benchmark programs	-	Benchmark programs are used for checking the performance of the processor for different applications.	-
9	Program Counter register	-	A special purpose register that is used to store the address of the next instruction to be executed.	-
10	Instruction Register	-	Register used to hold the instruction that is currently being executed.	-
11	Computer types according to size	-	• Microcomputer • Mini computer • Personal computer • Portable notebook computer • Workstations • Mainframe • Server • Supercomputer	-
12	Basic functional units of computer	-	• Input unit • Output unit • Memory unit • ALU • Control unit	-
13	EDVAC	-	EDVAC (Electronic Discrete Variable Computer) is the first program stored computer.	-
14	CPU time	-	Time the CPU spends computing for particular task	-
15	Types of Benchmark programs	-	• Desktop Benchmark • Server Benchmark • Embedded Benchmark	-
16	SPEC rating	-	• System Performance Evaluation Corporation rating. • It is the ration of running time of a reference computer to running time of the computer under test.	-
17	Basic levels in the digital system design	-	• Register level • Processor level	-
18	Processor level system	-	• CPU • Memory • IO devices	-

	design components			
19	Register level system design components	-	• Registers • Counters • Combinational circuits • Small sequential circuits	-
20	Types of PLD	-	• Read Only Memory (ROM) • Programmable Logic Array (PLA) • Programmable Array Logic (PAL)	-
21	Fixed point number system	-	Number system in which radix point is fixed	-
22	Floating point number system	-	Number system in which radix point is said to float.	-
23	Three fields in floating point number representation	-	• Sign • Significant digits (Mantissa) • Exponent	-
24	Single precision IEEE standard for floating point number	-	• Field 1 – Sign – 1 bit • Field 2 – Exponent – 8 bits • Field 3 – Mantissa – 23 bits	-
25	Double precision IEEE standard for floating point number	-	• Field 1 – Sign – 1 bit • Field 2 – Exponent – 1 bit • Field 3 – Mantissa – 52 bits	-

Unit II Arithmetic Unit and Data Path Design				
26	Data path unit	-	The data path unit is a collection of functional units capable of performing all arithmetic and logic operations.	-
27	Booth's algorithm	-	Booth algorithm is a technique for multiplication that works equally well for both negative and positive multiplier.	-
28	Division algorithms	-	• Restoring division algorithm, • Non-restoring division algorith	-
29	Guard bits	-	In floating-point arithmetic guard bits which are extra bits used in the intermediate steps of calculations to get maximum accuracy in the final result.	-
30	Chopping	-	Chopping is the simplest method of truncation or removal of guard bits.	-
31	Coprocessor	-	Coprocessor is a separate instruction processor that implements special functions with low-cost and fast hardware.	-
32	Coprocessor trap	-	When coprocessor is not connected in the system and coprocessor instructions are included in the program, the program control is transferred to a predetermined memory location where a software routine implementing the desired coprocessor instruction is stored. This type interrupt generated by the CPU is called coprocessor trap.	-
33	Von Neumann rounding	-	Von Neumann rounding is the simplest method of truncation.	-
34	Problems in floating-point arithmetic	-	• Mantissa overflow, • mantissa underflow, • exponent overflow and • exponent underflow a	-
35	Algorithms used for multiplication	-	• Roberson's algorithm and • Booth's algorithm	-
36	Parts of a processor unit	-	• Data Processing unit • Control unit	-
37	Types of Adders	-	• Serial Adder • Parallel Adder	-

38	Non-restoring division algorithm	-	Division algorithm that does not need restoring of remainder but needs restoring of remainder if it is negative	-
39	ALU	-	Arithmetic logic unit that performs adding, subtracting, shifting and logical operation.	-
40	Three methods of truncation	-	• Chopping • Von Neumann rounding • Rounding	-
41	Type of memory used in main memory	-	DRAM – Dynamic Random-Access Memory	-
42	Types of ALU	-	• Combinational ALU • Sequential ALU	-
43	Two ways of ALU expansion	-	• Spatial • Temporal	-
44	Motorola 68882 coprocessor	-	Coprocessor used with M68020nCPU	-
45	Rules for floating point multiplication	-	1. Add the exponent and subtract the bias 2. Multiply the mantissa and determine sign of result. 3.Normalize result	-
46	Rules for floating point division	-	1. Subtract the exponent and add the bias 2. Divide the mantissa and determine sign of result. 3.Normalize result	-
47	Robertson algorithm	-	Multiplication algorithm for 2's complement operands.	-
48	Look ahead carry adder	-	An electronic adder that improves speed by reducing the amount of time required to determine the carry bits.	-
49	Control word	-	The word that is used to select one of te processing options	-
50	Throughput of superscalar processor	-	More than one	-
Unit III Control Unit Design				
51	Control unit	-	Control unit issues control signals to the data processing part to perform operations on data.	-
52	Hardwired control	-	Control units use fixed logic circuits to interpret instructions and generate control signals from	-

			them.	
53	Microprogramming	-	Microprogramming is a method of control unit design in which the control signal selection and sequencing information is stored in a ROM or RAM called a control memory.	-
54	Instruction pipelining	-	A process in which the fetch, decode and execute cycles for several instructions are performed simultaneously to reduce overall processing time.	-
55	Superscalar processor	-	A processor capable of parallel instruction execution and having performance level greater than one instruction per cycle is known as superscalar processor.	-
56	Instruction level parallelism	-	In an instruction level parallelism, the instructions in a sequence are independent and are executed in parallel by overlapping.	-
57	Micro-pipelining	-	Many times, pipeline stages are subdivided upto logic gates level called micro-pipelining.	-
58	Pipeline hazards	-	Any reason the causes the pipeline to stall is called a hazard.	-
59	Four stage pipelines	-	• Instruction fetch, • operand loading, • execute instruction and • operand storing stages.	-
60	Microprogrammed control unit	-	The control unit whose binary control variables are stored in memory is called a microprogrammed control unit.	-
61	Control unit design approaches	-	• Hardwired control unit • Microprogrammed control unit	-
62	Design methods of hardwired control unit	-	• State-table method • Delay-element method • Sequence-counter method • PLA method	-
63	Types of Hazards	-	• Structural hazards, • data hazards and • instruction or • control hazard	-
64	Components of microprogram	-	• Microprogram sequencer • Control address memory • Control memory	-

	med control unit		• Microinstruction register • Decoder	
65	Processor registers	-	• Program counter (PC) • Address Register (AR) • Data Register (DR) • Accumulator (AC)	-
66	Components of control unit	-	• Control memory • Control address register • Subroutine register	-
67	Techniques for grouping of control signals	-	• Horizontal organization • Vertical organization	-
68	Microprogram	-	Sequence of one or more micro-operations designed to perform specific operation	-
69	IR	-	Instruction Register – Register which holds the opcode of the instruction being executed	-
70	MDR	-	Memory data register that holds the instruction code/data received from / sent to the memory.	-
71	Pipeline register	-	Control register that holds the present microinstruction while the next address is computed and read from memory	-
72	Pipelining	-	Temporal overlapping of processing	-
73	Pipeline processor	-	Processor supporting pipelining hardware architecture	-
74	Classification of data dependent hazards	-	• Write after read • Read after write • Write after write	-
75	Issues in implementing superscalar processors	-	• Instruction type • E-unit availability • True data dependency • Procedural dependency • Resource conflicts • Output dependency • Anti-dependency	-
Unit IV Memory Organization				
76	Cache memory	-	Cache memory is a small, fast memory that is inserted between the larger, slower main memory and the processor.	-
77	Non-volatile	-	A memory that holds data even if power is	-

	memory		turned off.	
78	Types of ROM	-	• Masked ROM, • programmable ROM (PROM), • erasable PROM (EPROM) and • electrically erasable programmable ROM (EEPROM) are the types of ROMs.	-
79	Types of RAM	-	• Static RAM (SRAM) and • Dynamic RAM (DRAM)	-
80	Virtual address	-	The addresses that processor issues to access either instruction or data are called virtual address or logical address.	-
81	Demand paging	-	The technique of getting desired page in the main memory	-
82	Segment translation	-	a process of converting logical address into a linear address.	-
83	page translation	-	a process of converting linear address into a physical address.	-
84	Virtual memory	-	Techniques that automatically swaps program or data blocks between the main memory and the secondary storage device	-
85	TLB	-	Translation Lookaside Buffer - The cache that stores the most recently used page table entries in it	-
86	Associative memory	-	A memory unit accessed by the content.	-
87	MAR	-	The MAR stands for memory address register. It holds the address of the active memory location.	-
88	Associative Memory also called as	-	Content addressable memory	-
89	Address decoding techniques	-	• Absolute decoding / full decoding • Linear decoding / Partial decoding	-
90	Advanced DRAMs	-	• Enhanced DRAM, • Cache DRAM • Synchronous DRAM • Rambus DRAM • Ramlink DRAM • Extended Data out DRAM	-
91	Example of Serial access	-	• Magnetic disk • Magnetic tape	-

	memory		• Optical memories	
92	Access Time	-	The time delay between receiving an address and the beginning of the actual data transfer.	-
93	Seek Time	-	Time required to move the read/write head to the proper track	-
94	Disk controller	-	A hardware interface provided to control the operation of a disk drive.	-
95	Optical memories	-	• Compact Disk Read only memory (CD-ROM) • Write-once Read-Many (WORM) • Erasable optical Disk	-
96	Memory Access methods	-	• Sequential access • Random access	-
97	Advantages of DRAM	-	• Cheap • More memory cells per unit area so small size	-
98	Physical memory types	-	• Semiconductor memory • Magnetic surface memory	-
99	Write policy to avoid the cache coherency	-	Write within	-
100	Efficient method of cache updating	-	Snoopy writes	-
Unit V Input/Output and System Organization				
101	Bus	-	A subsystem that is used to connect computer components and transfer data between them	-
102	Bus master	-	The device that is allowed to initiate data transfers on the bus at any given time is called bus master.	-
103	Operating system	-	• Operating system is a program which acts as an interface between a user of a computer and computer hardware. • It also provides an environment in which a user may execute programs.	-
104	I/O mapped	-	In I/O mapped I/O, processor provides separate	-

	I/O		address range for memory and I/O devices.	
105	Memory mapped I/O	-	In memory mapped I/O, memory control signals are used to the read and write I/O operations, whereas in I/O mapped I/O, I/O control signals are used to control read/write I/O operations.	-
106	ISR	-	Special routine that is executed to service the interrupt is called interrupt service routine (ISR).	-
107	Vectored interrupt	-	If the processor produces a CALL to a predetermined memory location which is the starting address of the ISR, the address is called vector address and such interrupts are called vectored interrupt.	-
108	Interrupt	-	An interrupt is an event that suspends the processing of currently executing program and begins the execution of another program.	-
109	Exception	-	Events that causes interrupt is called exception.	-
110	Fault tolerance	-	Ability of a system to execute specified algorithms correctly regardless of the hardware or software failures.	-
111	Typical control bus signals	-	• MEMR (Memory Read) • MEMW (Memory Read) • IOR (I/O Read) • IOW (I/O Read) • INTR Interrupt request • INTA Interrupt Acknowledgement • HOLD • HLDA Hold Acknowledge • bus request • Bus grant • Reset • Ready • CLK	-
112	Bus design parameters	-	• Type of bus • Method of arbitration • Timing • Bus width • Data transfer type	-
113	Two approaches of bus arbitration	-	• Centralized • Distributed	-

114	Central bus arbitration methods	-	• Daisy chaining • Polling method • Independent request method	-
115	Major requirement of IO module	-	• Control & timing • CPU communication • Device communication • Data buffering • Error detection	-
116	Memory interfacing techniques	-	• Memory mapped I/O • I/O mapped I/O	-
117	Two main IO instructions	-	• IN port address • OUT port address	-
118	Programmed I/O system	-	Computer system in which the I/O operations are completely controlled by the CPU	-
119	Interrupt driven I/O	-	a way of controlling input/output activity	-
120	I/O interface	-	The method that is used to transfer information between internal storage and external I/O devices	-
121	Three possible ways of data transfer to or from the peripherals	-	1. Programmed I/O. 2. Interrupt- initiated I/O. 3. Direct memory access (DMA).	-
122	DMA data transfer modes	-	• Single transfer (cycle stealing) • Block transfer • Demand / burst transfer	-
123	Types of I/O channels	-	• Selector channel • Multiplexer	-
124	Intel 8089	-	IO processor that has the ability to execute IO instructions	-
125	Types of redundancy for fault tolerance	-	• Hardware redundancy • Software redundancy • Information redundancy • Time redundancy	-
Placement Questions				
126	RISC	-	Reduced instruction set processor that use hardwired control. It uses separate instruction	-

			and data cache.	
127	CISC	-	Complex instruction set processor that use micro programed control	-
128	Services offered by operating systems	-	• Memory management • I/O device management • File system support • Job scheduling • Swapping of the other programs etc.	-
129	Types of operating system	-	• Batch • Multiprogramming • Time sharing • Real time	-
130	Example of real time operating system	-	• PSOS. PSOS is widely used in embedded applications and is a host target type of **RTOS** • VRTX. • RT Linux • Lynx.	-
131	Protections needed for operating system	-	• I/O protection • Memory protection • CPU protection	-
132	Operating system services	-	• Program execution • I/O operation • File system manipulation • Error detection • Resource allocation • Accounting • Protection	-
133	System calls	-	• Provides the interface a running program and the operating system	-
134	Categories of system calls	-	• Process or job control • File manipulation • Information maintenance	-
135	System calls used for file manipulation	-	• Create file • Delete file • Open • Close • Read	-

			• Write • Reposition • Get file attributes • Set file attributes	
136	System calls for process / job control	-	• End • Abort • Load • Execute • Create process • Terminate process • Get process attributes • Set process attributes • Wait for time • Wait event • Signal event	-
137	System program	-	• File modification • Program language support • Program loading & execution • Application	-
138	Types of multiprocessor stem architecture	-	• Loosely coupled multiprocessor system • Tightly coupled multiprocessor system	-
139	Contention problems in multiprocessor system	-	• Memory contention • Communication contention • Hotspot contention	-
140	Techniques for reducing contention	-	• Local memories • Better interconnection network system • Cache memory • Memory allocation	-
141	WMFC	-	Wait For Memory Function Complete signal that enables the processor to wait for the memory operation to complete	-
142	Memory type used in cache memory	-	SRAM – Static Random-Access Memory	-
143	The last on the hierarchy scale	-	Secondary memory	-

	of memory devices			
144	Application of ROM chips	-	To store Boot files	-
145	Two types of computer memory	-	• Primary memory • Secondary memory	-
146	Examples of secondary storage memory	-	• Compact disk, • floppy disk, • pen drive, • external hard drive, etc.	-
147	Memory mapping functions	-	used to map the memory blocks on to their corresponding cache block.	-
148	Dirty bit	-	The bit used to indicate whether the block was recently used or not	-
149	SCSI Bus	-	SCSI (Small Component System Interconnect) is used to connect to display devices to CPU	-
150	MFC	-	MFC stands for Memory Function Complete; signal is used to show complete of memory operation.	-

Faculty Team Prepared **Signatures**

1. Mr.V.Ramesh,AP/ECE
2. Mr.M.Eswaramoorthy,AP/ECE
3. Mrs.A.Nivetha,AP/ECE **HoD**