# MUTHAYAMMAL ENGINEERING COLLEGE

(An Autonomous Institution)

(Approved by AICTE, New Delhi, Accredited by NAAC & Affiliated to Anna University)
Rasipuram - 637 408, Namakkal Dist., Tamil Nadu

Estd. 2000

IQAC

## MUST KNOW CONCEPTS

**MKC**

**ECE**

**2021-2022**

**Course Code & Course Name** : **19GES24 – DIGITAL PRINCIPLES & SYSTEM DESIGN**

**Year/Sem/Sec** : **II / III / A, B & C**

| **Subject Code/Name** | | **19GES24 /DIGITAL PRINCIPLES AND SYSTEM DESIGN** | | |
|---|---|---|---|---|
| **S.No** | **Term** | **Notation ( Symbol)** | **Concept/Definition/Meaning/Units/Equation/Expression** | **Units** |
| **UNIT I - BOOLEAN ALGEBRA AND LOGIC GATES** | | | | |
| 1 | Digital Electronics | | Digital (electronic) circuits operate on digital signals ( 0 and 1). | |
| 2 | Number system | | Decimal Number system (0-9) base 10<br>Binary Number system( 0 and 1) base 2<br>Octal Number system (0-7) base8<br>Hexadecimal Number system(0-9, A- F) base 16 | |
| 3 | Signed Numbers | | Signed numbers contain both sign and magnitude of the number. Generally, the sign is placed in front of number.<br>If sign bit is zero, which indicates the binary number is positive. Similarly, if sign bit is one, which indicates the binary number is negative. | |
| 4 | Representation of Signed Binary Numbers | | Sign-Magnitude form<br>1's complement form<br>2's complement form | |
| 5 | Un-Signed Binary Numbers | | The bits present in the un-signed binary number holds the magnitude of a number. That means, if the un-signed binary number contains 'N' bits, then all N bits | |

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| | | | represent the magnitude of the number | |
| 6 | 1's complement form | | The 1's complement of a number is obtained by complementing all the bits of signed binary number ( 1 change into 0, 0 change into 1) | |
| 7 | The 2's complement | | The 2's complement of a binary number is obtained by adding one to the 1's complement of signed binary number. So, 2's complement of positive number gives a negative number. Similarly, 2's complement of negative number gives a positive number.<br>That means, if you perform two times 2's complement of a binary number including sign bit, then you will get the original signed binary number. | |
| 8 | Code and binary code. | | The group of symbols is called as code. The digital data is represented, stored and transmitted as group of bits. This group of bits is also called as binary code. | |
| 9 | Types of binary code | | • Weighted codes<br>• Un weighted codes<br>• Error detecting and correcting codes | |
| 10 | WEIGHTED CODE | | The weighted code are those that obey the position weighting principle, which states that the position of each number represent a specific weight. | |
| 11 | Un weighted codes | | The Non - Weighted Code are not positionally weighted. In other words, codes that are not assigned with any weight to each digit position. | |
| 12 | Commutative law | | $x + y = y + x$<br>$x.y = y.x$ | |
| 13 | Associative Law | | $x + (y + z) = (x + y) + z$<br>$x.(y.z) = (x.y).z$ | |

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| 14 | Distributive Law | | x.(y + z) = x.y + x.z<br>x + (y.z) = (x + y).(x + z) | |
| 15 | Duality theorem | | This theorem states that the dual of the Boolean function is obtained by interchanging the logical AND operator with logical OR operator and zeros with ones. For every Boolean function, there will be a corresponding Dual function. | |
| 16 | DeMorgan's Theorem | | 1. (x + y)′ = x′.y′<br>2. (x.y)′ = x′ + y′ | |
| 17 | Boolean function | | It is described by an algebraic expression consists of binary variable , constant and logic operators. | |
| 18 | min terms | m | Boolean product terms are called as min terms .<br>It denoted by "m" | |
| 19 | Canonical SoP | ∑ m | Canonical Sum of Products form. In this form, each product term contains all literals. So, these product terms are nothing but the min terms. Hence, canonical SoP form is also called as sum of min terms form. | |
| 20 | Max terms | M | Boolean sum terms are called as Max terms .<br>It denoted by "M" | |
| 21 | Canonical PoS | ∏M | Canonical Product of Sums form. In this form, each sum term contains all literals. So, these sum terms are nothing but the Max terms. Hence, canonical PoS form is also called as product of Max terms form. | |
| 22 | Karnaugh or K-Map | | It is graphical representation of Boolean functions and is used to simplify Boolean functions .K map is a matrix of squares and each square or Cell represents a minterm or maxterm from of Boolean expression | |
| 23 | don't care | | If don't care terms also present, then place don't cares 'x' in the respective cells of K-map. Consider only the don't cares 'x' that are helpful for grouping maximum number of adjacent zeroes. In those cases, | |

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| | | | treat the don't care value as '0'. | |
| 24 | Tabulation method | | It is difficult to simplify the functions using K-Maps. Because, the number of **cells** in K-map gets **doubled** by including a new variable. | |
| 25 | Logic Gates | | 1. Basic Logic gate – NOT,AND,OR<br>2. Universal Logic gate – NAND, NOR<br>3. Special Logic gate – EX OR, EX NOR | |
| 26 | NAND and NOR implementation | | Logic circuits designed using universal gates | |
| **UNIT II - COMBINATIONAL LOGIC** | | | | |
| 27 | Combinational circuits | | It is consist of Logic gates. These circuits operate with binary values. The output(s) of combinational circuit depends on the combination of present inputs | |
| 28 | Analysis and design procedure | | Circuit is analysed to make sure that given circuit is combinational and by using design procedure we implement the combinational circuit. | |
| 29 | Analysis procedure | | Label all gate outputs that are a function of input variables with arbitrary symbols. Determine the Boolean functions for each gate output.<br>Label the gates that are a function of input variables and previously labeled gates with other arbitrary symbols.<br>Find the Boolean functions for these gates.<br>Repeat the process outlined in step 2 until the outputs of the circuit are obtained. By repeated substitution of previously defined functions,<br>obtain the output Boolean functions in terms of input variables. | |
| 30 | Design procedure | | 1.The problem definition.<br>2.The no of available and required output variable is determined<br>3.The input and output variables are assigned letter symbols.<br>4.The truth table that defines the required relationship between inputs and outputs | |

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| | | | are<br>derived.<br>5.The simplified Booleanfunction for each output is obtained.<br>6. The logic diagram is drawn. | |
| 31 | Half Adder | | Half adder is a combinational circuit, which performs the addition of two single bits A & B and produce two outputs sum and carry. | |
| 32 | Full Adder | | Full adder is a combinational circuit, which performs the addition of three bits A, B and $C_{in}$. Where, A & B are the two parallel significant bits and $C_{in}$ is the carry bit, which is generated from previous stage. This Full adder also produces two outputs sum, S & carry, $C_{out}$, which are similar to Half adder. | |
| 33 | 4-bit Binary Adder | | The 4-bit binary adder performs the addition of two 4-bit numbers. Let the 4-bit binary numbers, $A=A_{3}A_{2}A_{1}A_{0}$ and $B= B_{3}B_{2}B_{1}B_{0}$. We can implement 4-bit binary adder in one of the two following ways. | |
| 34 | Carry look-ahead | | The parallel adder causes a unstable factor on carry bit, and produces longest propagation delay. That limit can be overcome by this technique | |
| 35 | Binary subtractor | | The circuit, which performs the subtraction of two binary numbers, is known as Binary subtractor. We can implement Binary subtractor in following two methods.1's and 2's complement form | |
| 36 | Rules of BCD adder | | When the binary sum is greater than 1001, The addition of binary 6(0110) to the binary sum converts it to the correct BCD representation | |
| 37 | Magnitude comparator | | **Its compares two digital or binary numbers** in order to find out whether one binary number is equal, less than or greater than. logically design a circuit -two inputs one for A and B and have three output terminals, A > B , A = B , A < B . | |
| 38 | Decoder | | Decoder is 'n' input lines and maximum of $2^n$ output lines. One of these outputs will be active High based on the combination of inputs present, when the decoder is enabled. | |

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| 39 | Encoder | | An Encoder is a combinational circuit that performs the reverse operation of Decoder. It has maximum of $2^n$ input lines and 'n' output lines. | |
| 40 | Encoder Applications | | **Encoders** are used to translate rotary or linear motion into a digital signal. Usually this is for the purpose of monitoring or controlling motion parameters such as speed, rate, direction, distance or position. | |
| 41 | Priority encoder | | If two inputs are active simultaneously, the output produces an undefined combination. We can establish an input priority to ensure that only one input is encoded. | |
| 42 | Multiplexer | | Multiplexer is a combinational circuit that has maximum of $2^n$ data inputs, 'n' selection lines and single output line. One of these data inputs will be connected to the output based on the values of selection lines. | |
| 43 | De-Multiplexer | | De-Multiplexer is a combinational circuit that performs the reverse operation of Multiplexer. It has single input, 'n' selection lines and maximum of $2^n$ outputs. | |
| 44 | Applications of Multiplexer and Demultiplexer | | Communication System – **Multiplexer** and Demultiplexer both are used in communication systems to carry out the process of data transmission. A De-**multiplexer** receives the output signals from the **multiplexer**; and, at the receiver end, it converts them back to the original form | |
| 45 | Code conversion | | Code converter is a circuit that makes the two systems compatible eventhough each uses a different binary codes. | |
| 46 | Gray code | | The reflected binary code or Gray code is an ordering of the binary numeral system such that two successive values differ in only one bit (binary digit). Gray codes are very useful in the normal sequence of binary numbers generated by the hardware that may cause an error or ambiguity during the transition from one number to the next. Gray code is not weighted code | |

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| 47 | BCD | | It is also called as 8421 code because each of the four bits is given a 'weighting' according to its column value in the binary system. The least significant bit (lsb) has the weight or value 1, the next bit, going left, the value 2. | |
| 48 | Excess-3 codes | | It is unweighted and can be obtained by adding 3 to each decimal digit then it can be represented by using 4 bit binary number for each digit | |
| 49 | HDL introduction | | 1.Hardware description language is a language that describes the hardware of a digital circuit in a textual form.<br>2. It can be used to represent logic diagrams, Boolean expressions and more complex digital circuits.<br>3.two applications of HDL processing<br>• Simulation<br>• Synthesis | |
| 50 | HDL models of comblnational circuits | | ➢ Gate level modeling<br>➢ Data level modeling<br>➢ Behaviour modelling | |
| **UNIT III - SYNCHRONOUS SEQUENTIAL LOGIC** | | | | |
| 51 | Memory Elements | | There are two types of memory elements based on the type of triggering that is suitable to operate it.<br>Latches<br>Flip-flops | Memory Elements |
| 52 | Latches | | Latches operate with enable signal, which is level sensitive | Latches |
| 53 | Flip-Flops | | Memory element used in clocked sequential circuits | Flip-Flops |
| 54 | Shift Register | | The one flip-flop can store one-bit of information. In order to store multiple bits of information, we require multiple flip-flops. The group of flip-flops, which are used to hold (store) the binary data is known as register. | Register |

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| 55 | Types Of shift Register | | Serial In − Serial Out shift register<br>Serial In − Parallel Out shift register<br>Parallel In − Serial Out shift register<br>Parallel In − Parallel Out shift register | Types Of Register |
| 56 | Johnson Ring Counter | | The **Johnson Ring Counter** or "Twisted Ring Counters", is another shift register with feedback exactly the same as the standard *Ring Counter* above, except that this time the inverted output Q of the last flip-flop is now connected back to the input D of the first flip-flop as shown below. | |
| 57 | Required Components of Serial Adder/Subtractor | | Required 2 register and one FA and one FF | **Required Components of Serial Adder/Subtractor** |
| 58 | Sequential Circuit | | The sequential circuit contains a set of inputs and output(s). The output(s) of sequential circuit depends not only on the combination of present inputs but also on the previous output(s). Previous output is nothing but the present state. | |
| 59 | Types of Sequential Circuits | | Asynchronous sequential circuits<br>Synchronous sequential circuits | |
| 60 | Synchronous sequential circuits | | Output changes at discrete interval of time. It is a circuit based on an equal state time or a state time defined by external means such as clock | |
| 61 | Asynchronous sequential circuits | | Output can be changed at any instant of time by changing the input. It is a circuit whose state time depends solely upon the internal logic circuit delays. | |
| 62 | Types of Triggering | | Level triggering<br>Edge triggering | |
| 63 | S-R Flip Flop | | It is basically a one-bit memory bistable device that has two inputs, one which will "SET" the device (meaning the output = "1"), and is labelled S and one which will "RESET" the device (meaning the output = "0"), labelled R. | |
| 64 | J-K Flip Flop | | It is basically a gated SR flip-flop with the addition of a clock input circuitry that prevents the illegal or invalid output | |

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| | | | condition that can occur when both inputs S and R are equal to logic level "1". | |
| 65 | D Flip Flop | | It is a modified Set-Reset flip-flop with the addition of an inverter to prevent the S and R inputs from being at the same logic level | |
| 66 | T Flip Flop | | These are basically a single input version of JK flip flop. This modified form of JK flip-flop is obtained by connecting both inputs J and K together. This flip-flop has only one input along with the clock input. | |
| 67 | Master Slave Flip Flop | | The master-slave flip-flop eliminates all the timing problems by using two SR flip-flops connected together in a series configuration. One flip-flop acts as the "Master" circuit, which triggers on the leading edge of the clock pulse while the other acts as the "Slave" circuit, which triggers on the falling edge of the clock pulse. | |
| 68 | Propagation Delay Time | | The Interval of time required after an input signal has been applied for the resulting output change to occur. | |
| 69 | Characteristics of register | | i. Memory Register (or) Buffer Register<br>ii. Shift Register | |
| 70 | Buffer Register | | It is a simplest form of registers which is simply used to store binary information. | |
| 71 | Shift Register | | A register may input and output data in serial or parallel form. A number of flip flops connected together in such a way that data may be shifted into and out of the register. | |
| 72 | Universal Shift Register | | A shift registers which can shift the data in both directions as well as loads it parallel. | |
| 73 | Uni-directional shift register | | A shift registers which can shift the data in only one direction. | |
| 74 | Bi-directional shift register | | A shift registers which can shift the data in both directions. | |

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| 75 | Counter | | It is a digital sequential logic device that will go through a certain predefined states based on the application of the input pulses. | |
| 76 | HDL for sequential circuits | | In verilog HDL there are two methods for defining a circuit:<br>➢ Structural modeling<br>➢ Behaviour modelling | |
| **UNIT-IV - ASYNCHRONOUS SEQUENTIAL LOGIC** | | | | |
| 77 | Asynchronous circuit | | The circuit in which the change in the input signals can affect the memory elements at any instants of the time. | |
| 78 | Different modes of operation | | The different modes of operation are fundamental mode and sequential mode circuits. | |
| 79 | Ripple counters | | Counter circuits made from cascaded J-K flip-flops where each clock input receives its pulses from the output of the previous flip-flop invariably exhibit a ripple effect, where false output counts are generated between some steps of the count sequence. | |
| 80 | Race condition | | Race condition (race) is a condition in sequential circuits in which two or more variables change at one time. | |
| 81 | Non-critical race | | The final stable state does not depend on the change order of state variables | |
| 82 | Critical race | | The change order of state variables will result in different stable states | |
| 83 | State assignment | | State assignment is the process of assignment of binary values to the states of the reduced state table in the design of asynchronous circuits. | |
| 84 | Cycle | | If an input change induces a feedback transitions through more than one unstable state | |

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| 85 | Hazard | | Hazard is the unwanted transient i.e.. Spike or glitch that occurs due to unequal propagation delays through a combination circuit. | |
| 86 | Stable state | | The time sequence of input, output and FF states can be enumerated in a state table it is also called as transition table. | |
| 87 | Transition Table | | Transition table is useful to analyze an asynchronous circuit from the circuit diagram | |
| 88 | Glitch | | The unwanted switching transients that may appear at the output of a circuit | |
| 89 | Static hazard | | Static hazard is a condition, which result in a single momentary incorrect output due to change is a single input variable when the output is expected to remain in the same state. | |
| 90 | Cause for Essential Hazard | | Operational error generally caused by an excessive delay to a Feedback variable in response to an input change, leading to a transition to an improper state. | |
| 91 | Flow Table | | It is similar to a transition table except the states are represented by letter symbols . | |
| 92 | Faults in asynchronous sequential circuits | | (1) Hazards<br>(2) Oscillations<br>(3) Critical races | |
| 93 | Static 1 hazard | | If the outputs before and after the change of input are both 1 with an incorrect output 0 in between. | |
| 94 | Static 0 hazard | | If the outputs before and after the change of input are both 0 with an incorrect output 1 in between | |
| 95 | Compatible pairs | | Two states are said to be compatible, if in every column of the corresponding rows in the flow table, there are identical states and if there is no conflict in the output values. | |

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| 96 | Maximal compatibles | | The maximal compatible is a group of compatibles that contains all the possible combinations of compatible states | |
| 97 | Types of hazards | | Static hazard, Dynamic hazard, Essential hazard. | |
| 98 | Primitive flow table | | primitive flow is the flow table that has only one stable state in each row. | |
| 99 | Secondary variables of asynchronous sequential circuits | | The present state and the next state variables in asynchronous sequential circuits are called Secondary / excitation variables. | |
| 100 | Application areas of asynchronous sequential circuits | | i. Used where speed is important<br>ii. Require only few components.<br>iii. Used where the input change at any time independent of clock.<br>iv. Communication between two units where each has own independent clock. | |
| 101 | State of sequential circuit | | The binary information stored in the memory elements at any given time defines the "state" of sequential circuit. | |
| **UNIT V - MEMORY AND PROGRAMMABLE LOGIC** | | | | |
| 102 | Types Of Memory | | 1. Primary memory (RAM and ROM).<br>2. Secondary memory(hard drive,CD,etc.) | |
| 103 | Random Access Memory | | It is a volatile memory as the data loses when the power is turned off. The programs and data that the CPU requires during execution of a program are stored in this memory. | |
| 104 | RAM Types | | *1. SRAM (Static Random Access Memory)*<br>*2. DRAM (Dynamic Random Access Memory).* | |
| 105 | Read Only Memory (ROM) | | Stores crucial information essential to operate the system, like the program essential to boot the computer. It is not volatile | |
| 106 | ROM Types | | ROM, PROM, EPROM, and EEPROM. | |

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| 107 | Error detection codes | | To detect the errors, present in the received data bit stream. These codes contain some bits, which are included appended to the original bit stream. | |
| 108 | Error correction codes | | To correct the errors, present in the received data bit stream so that, we will get the original data. Error correction codes also use the similar strategy of error detection codes | |
| 109 | Parity Code | | A parity bit is an extra bit included with a message to make the total number of 1's either even or odd. | |
| 110 | Types of Parity Codes | | 1.Even Parity Code<br>2. Odd Parity Code | |
| 111 | Even parity | | Checks if there is an even number of ones; if so, parity bit is zero. When the number of one's is odd then parity bit is set to 1. | |
| 112 | Odd Parity | | Checks if there is an odd number of ones; if so, parity bit is zero. When the number of one's is even then parity bit is set to 1. | |
| 113 | Hamming code | | It adds a minimum number of bits to the data transmitted in a noisy channel, to be able to correct every possible one-bit error. | |
| 114 | Programmable Array Logic | | PAL is a programmable logic device that has Programmable AND array & fixed OR array. | |
| 115 | Programmable Logic Array | | PLA is a programmable logic device that has both Programmable AND array & Programmable OR array. | |
| 116 | PROM (Programmable read-only memory) | | It can be programmed by user. Once programmed, the data and instructions in it cannot be changed. | |
| 117 | EPROM (Erasable Programmable read only memory) | | It can be reprogrammed. To erase data from it, expose it to ultra violet light. To reprogram it, erase all the previous data. | |
| 118 | EEPROM (Electrically erasable programmable read only | | The data can be erased by applying electric field, no need of ultra violet light. We can erase only portions of the chip. | |

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| | memory) | | | |
| 119 | Sequential programmable devices | | Sequential programmable devices include both gates and flip-flops. In this way, the device can be programmed to perform a variety of sequential-circuit functions. | |
| 120 | Sequential programmable devices Types | | 1. Sequential (or simple) programmable logic device (SPLD)<br>2. Complex programmable logic device (CPLD)<br>3. Field-programmable gate array (FPGA) | |
| 121 | Sequential (or simple) programmable logic device (SPLD) | | The SPLD includes flip-flops, in addition to the AND–OR array, within the integrated circuit chip. A PAL or PLA is modified by including a number of flip-flops connected to form a register | |
| 122 | Complex programmable logic device (CPLD) | | It is a collection of individual PLDs on a single integrated circuit. A programmable interconnection structure allows the PLDs to be connected to each other in the same way that can be done with individual PLDs | |
| 123 | Field programmable gate array (FPGA) | | FPGA logic block consists of lookup tables, multiplexers, gates, and flip-flops. A lookup table is a truth table stored in an SRAM and provides the combinational circuit functions for the logic block | |
| 124 | Application Specific Integrated Circuit( ASIC) | | These are usually designed from root level based on the requirement of the particular application. Examples are chips used in toys, the chip used for interfacing of memory and microprocessor | |
| 125 | Advantages of ASIC | | ➢ The small size of ASIC makes it a high choice for sophisticated larger systems.<br>➢ As a large number of circuits built over a single chip, this causes high-speed applications.<br>➢ ASIC has low power consumption.<br>➢ ASIC has no timing issues and post-production configuration. | |
| 126 | ASIC Types | | ➢ Programmable<br>1. FPGAs<br>2. PLDs<br>➢ Semi Custom<br>1.Gate Array Based | |

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| | | | i) Structured Gate<br>ii) Channel-less<br>iii) Channeled<br>2.Standard Cell Based<br>➢ Full Custom | |
| **GATE/Placement Related Questions** | | | | |
| 127 | Simplification | | 1899.981 ÷ √1444.12 – 119.910 % of 34.975 + 4.932 * 104.292 = **?**<br><br>**Ans:** 528 | |
| 128 | Profit and Percentage | | A box contains six pink balls and four orange balls and three balls drawn one after other. Find the probability of all three balls being Pink balls if the balls drawn are not replaced?<br><br>**Ans:** 1/6 | |
| 129 | Number Series | | Find the wrong term in the following number series?<br>**90, 86, 95, 79, 103, 68, 117**<br><br>**Ans:** 103 | |
| 130 | Number Series | | What value should come in the place of question mark in the given series?<br>**19, 23, 32, 48, 73, 109, ?**<br><br>**Ans:** 158 | |
| 131 | Relation ship | | Eight persons B, E, J, K, M, S, T and V are in a family with three different generations. J is the son of B. E is the daughter of K and sister of S. M is the mother of E. V is the sister-in-law of S, who has only two siblings. S is the aunt of J. T is the niece of B. E does not has any child.<br>**If J is married to X, then how is X related to E?**<br><br>**Ans:** Cannot be determined | |
| 132 | Computer Awareness | | The address of input/output device or memory is carried by the _____ and the data to be transferred is carried by the _____<br><br>**Ans:** Address bus, Data bus | |

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| 133 | Directions | | A man started walking from his place. He goes 5m south. He turns 90 degree anticlockwise and walks for 7m. Now he turns left and goes 3m. After turning right, he walks for 4m, again he walks for 3m after turning left. Now he turns towards west and walks for 5m. He again walks for 5m before he stops.<br>**What is the shortest distance between his starting point and ending point?**<br><br>**Ans:** 1m | |
| 134 | Speed and Time | | A bag contains 4 red marbles, 5 green marbles and 6 pink marbles. If 3 marbles are taken at randomly, then find the probability that 2 marbles are Pink?<br><br>**Ans: 27/91** | |
| 135 | Time and Work | | A can do a work in 15 days, B can do it in 12 days but C can do (3/4)th of the work in 18 days. Find the time taken by all together to complete the work?<br><br>**Ans:** 5 5/23 days | |
| 136 | Time and Work | | A contractor hired 40 men to complete a project in 15 days. 40 men started working, after 9 days the contractor notices that only three-fifth of the work gets completed. Then how many extra men can be employed to complete the remaining work on time?<br><br>**Ans: 0** | |
| 137 | Carry flag | | Set when carry occurs after an operation, otherwise reset. | |
| 138 | Parity flag | | Set if the result of an operation contains even number of 1 bits, otherwise reset. | |
| 139 | **Stack Pointer** | | Stack pointer is a special purpose 16-bit register in the Microprocessor, which holds the address of the top of the stack. | |
| 140 | **Program Counter** | | Program counter holds the address of either the first byte of the next instruction to be fetched for execution. | |
| 141 | **Bus** | | A bus is a group of conducting lines that carriers data, address, & control signals. | |

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| 142 | **Tri-state Logic** | | Three Logic Levels are used and they are High, Low, High impedance state. | |
| 143 | **Hardware Interrupts** | | TRAP, RST7.5, RST6.5, RST5.5, INTR. | |
| 144 | **Software Interrupts** | | RST0, RST1, RST2, RST3, RST4, RST5, RST6, RST7. | |
| 145 | **Addressing Modes** | | Immediate, Direct, Register, Register indirect, Implied addressing modes. | |
| 146 | **Quality Factor Mean** | | The Quality factor is also defined, as Q. So it is a number, which reflects the lossness of a circuit. Higher the Q, the lower are the losses. | |
| 147 | Assembler | | Assembler is used to translate the high level language program to machine code. | |
| 148 | Emulator | | Emulators are used to test and debug the hardware and software of an external system. | |
| 149 | Compiler | | Compiler is used to translate the high-level language program into machine code at a time. | |
| 150 | BIU | | Bus interface unit is responsible for transferring the data addresses on the buses necessary for -execution unit. | |
| 151 | Multiplexing | | Using a single bus for two different functions is called multiplexing. | |



| Faculty Team Prepared | | Signatures | HOD |
|---|---|---|---|
| 1. | **Mr.M.Eswaramoorthy** | | |
| 2. | **Mrs.G.Ranjitha** | | |
| 3. | **Mrs.P. Subhasundari** | | |