MUTHAYAMMAL ENGINEERING COLLEGE

(An Autonomous Institution)

(Approved by AICTE, New Delhi, Accredited by NAAC & Affiliated to Anna University)

Rasipuram - 637 408, Namakkal Dist., Tamil Nadu.

Estd. 2000

IQAC

MUST KNOW CONCEPTS

MKC

CSE

2021-22

Course Code & Course Name : 19CSC05-Computer Organization and Architecture

Year/Sem/Sec : II / III / A, B & C

S.No.	Term	Notation (Symbol)	Concept / Definition / Meaning / Units / Equation / Expression	Units
Unit-I : Basic Structure of Computers				
1.	Computer Architecture	-	Computer architecture is defined as the functional operation of the individual hardware unit in a computer system and the flow of information among the control of those units.	-
2.	Computer Hardware	-	Computer hardware is the electronic circuit and electro mechanical equipment that constitutes the computer	-
3.	Functional Units	-	1. Input unit 2. Output unit 3. Control unit 4. Memory unit 5. Arithmetic and logical unit	-
4.	CPU	-	The arithmetic and logic unit in conjunction with control unit is commonly called Central Processing Unit (CPU)	-
5.	Functions of Input Unit	-	A computer accepts digitally coded information through input unit using input devices such as keyboard and mouse	-
6.	Functions of Control Unit	-	The control unit co-ordinates and controls the activities amongst the functional units.	-
7.	Function of ALU	-	Performs arithmetic operations such as add, subtract, division and	-

			multiplication, and logical operations such as AND, OR etc.	
8.	CPI	-	The term clock cycles per instruction is the average number of clock cycles each instruction takes to execute, is often abbreviated as CPI. CPI=CPUclock cycles/Instruction count.	-
9.	Word	-	Group of n bits is called as word	-
10.	Response Time	-	Response time is the time between the start and the completion of the event. Also referred to as execution time or latency	-
11.	Throughput	-	Throughput is the total amount of work done in a given amount of time.	-
12.	Addressing modes	-	The different ways that a processor can access data are referred to as addressing schemes or addressing modes	-
13.	Different addressing modes	-	Register Mode, Absolute mode or Direct mode, Immediate mode, Indirect mode, Index mode, Relative mode, Auto increment mode, Auto decrement mode	-
14.	BCD	-	Binary Coded decimal is the format usually used to store data in the computer	-
15.	Bus	-	A group of lines that serves a connecting path for several devices is called a bus	-
16.	Instruction Register	-	Holds the instructions that is currently being executed	-
17.	Program Counter	-	This is another specialized register that keeps track of execution of a program	-
18.	Memory Address Register	-	It holds the address of the location to be accessed	-
19.	Memory Data Register	-	It contains the data to be written into or read out of the address location	-
20.	Elapsed time	-	The total time required to execute	-

			the program is elapsed time	
21.	Processor time	-	The time needed to execute a instruction is called the processor time	-
22.	Load	-	Load operation, the processor sends the address of the desired location to the memory and requests that its contents be read	-
23.	Store	-	Store operation transfers an item of information from the processor to a specific memory location, destroying the former contents of that location	-
24.	Conditional Code falgs	-	The processor keeps track of the results of its operations using flags called Conditional Code flags	-
25.	Program-controlled I/O	-	A simple way of performing I/O tasks is to use a method known as program-controlled I/O	-
Unit-II : Arithmetic Unit				
26.	ALU	-	An arithmetic-logic unit (ALU) is the part of a computer processor (CPU) that carries out arithmetic and logic operations	-
27.	Full Adder	-	Full Adder is the adder which adds three inputs and produces two outputs. The first two inputs are A and B and the third input is an input carry as C-IN. The output carry is designated as C-OUT and the normal output is designated as S which is SUM.	-
28.	carry look-ahead adder	-	A carry look-ahead adder reduces the propagation delay by introducing more complex hardware	-

29.	Ripple carry adder	-	The n-bit parallel adder using n number of full-adder circuits connected in cascade, i.e. the carry output of each adder is connected to the carry input of the next higher-order adder is called ripple carry adder.	-
30.	Booth's multiplier	-	Booth's algorithm generates a 2n-bit product and treats both positive and negative numbers uniformly. This algorithm suggests that we can reduce the number of operations required for multiplication by representing multiplier as a difference between two numbers.	-
31.	IEEE floating point single precision	-	(field 1)Sign ⟵ 1-bit (field 2)Exponent ⟵ 8-bits (field 3)Mantissa ⟵ 23-bits	-
32.	IEEE floating point double precision	-	(field 1)Sign ⟵ 1-bit (field 2)Exponent ⟵ 1-bit (field 3)Mantissa ⟵ 52-bits	-
33.	Underflow	-	In a single precision, if the number requires an exponent less than -126 or in a double precision, if the number requires an exponent less than -1022 to represent its normalized from to underflow occurs.	-
34.	Overflow	-	In a single precision, if the number requires an exponent greater than +127 or in a double precision, if the number requires an exponent greater than +1023 to represent its normalized form the overflow occurs.	-

35.	Rules of floating point multiplication	-	Add the exponents and subtract bias.(127 in case of single precision numbers and 1023 in case of double precision numbers). Multiply the mantissas and determine the sign of the result. Normalize the result.	-
36.	Guard bits	-	The mantissas of initial operands and final results are limited to 24-bits, including the implicit leading 1. But if we provide extra bits in the intermediate steps of calculations we can get maximum accuracy in the final result. These extra bits use in the intermediate calculations are called guard bits.	-
37.	Rules of floating point division	-	Subtract the exponents and add bias.(127 in case of single precision numbers and 1023 in case of double precision numbers). Divide the mantissas and determine the sign of the result. Normalize the result	-
38.	Advantage of Non Restoring over Restoring division	-	Non restoring division avoids the need for restoring the contents to register after an successful subtraction	-
39.	Carry look-ahead adders	-	Carry look-ahead adders are used for addition of large integers	-
40.	Flag V	-	The Flag 'V' when set to 1 indicates that The operation has resulted in an overflow	-
41.	LSB	-	Least Significant Bit	-
42.	MSB	-	Most Significant Bit	-
43.	Bit-pair recoding	-	Bit-pair recoding is the product of the multiplier results in using at most one summand for each pair of bits in the multiplier. It is derived directly from the Booth algorithm.	-
44.		-	When the decimal point is placed	-

	Normalized Number		to the right of the first(non zero) significant bit, then the number is said to be normalized	
45.	IEEE	-	Institute of Electrical and Electronics Engineers	-
46.	Single-precision floating-point	-	Single-precision floating-point format is a computer number format, usually occupying 32 bits in computer memory	-
47.	Double-precision floating-point	-	Double Precision is also a format given by IEEE for representation of floating-point number. It occupies 64 bits in computer memory.	-
48.	Mantissa	-	The positive portion of a logarithm, which is to the right of a decimal point. For example, with the number 1.234, .234 is the mantissa.	-
49.	NaN	-	Not a Number	-
50.	Guard bit	-	To retain maximum accuracy, all extra bits during operation are kept (e.g., multiplication). These extra bits are called as guard bits	-
Unit-III : Basic Processing Unit and Pipelining				
51.	Datapath	-	The registers, the ALU and the interconnecting bus are collectively referred to as datapath	-
52.	Mircro instruction	-	A computer instruction that activates the circuits necessary to perform a single machine operation usually as part of the execution of a machine-language instruction.	-
53.	TLB	-	Translation Look aside Buffer is used to hold the page table entries that correspond to the most recently accessed pages.	-
54.	Interrupt	-	An interrupt is an event that causes	-

			the execution of one program to be suspended and another program to be executed	
55.	Exception	-	The term exception is often used to refer to any event that causes an interruption	-
56.	Bus Arbitration	-	Bus arbitration is the process by which the next device to become the bus master is selected and bus mastership is transferred to it. The selection of bus master is usually done on the priority basis.	-
57.	Tri-state gates	-	The gates having three output states: logic 0, logic 1 and high-impedance are called tri-state gates.	-
58.	Loop buffer	-	A loop buffer is a small very high speed memory. It is used to store recently perfected instructions in sequence.	-
59.	Pipelining	-	Pipelining is a technique of decomposing a sequential process into sub operations with each sub process being executed in a special dedicated segment that operates concurrently with all other segments	-
60.	Instruction Pipelining	-	Performing fetch, decode and execute cycles for several instructions simultaneously to reduce overall processing time is refered to as instruction pipelining	-
61.	Hazard in Pipelining	-	Any reason that causes the pipeline to stall is called a hazard	-
62.	Instruction or control hazard	-	The hazard due to pipelining branch and other instructions that change the contents of program counter is called instruction or	-

			control hazard	
63.	Delayed Load and Delayed Slot	-	A load which requires that the following instruction do not use its result is said to be delayed load and the pipeline slot after load instructioin is called delayed slot	-
64.	Classification of data hazards	-	• RAM (read after writ)hazard • WAW (Write after write) hazard • WAR (Write after read) hazard.	-
65.	Static branch prediction	-	The branch prediction decision is always the same every time a given instruction is executed. Any approach that has this characteristic is called static branch prediction	-
66.	Dynamic branch prediction	-	The prediction decision may change depending on execution history is called dynamic branch prediction	-
67.	Cache in pipelining	-	Each pipeline stage is expected to complete in one clock cycle. The clock period should be enough to let the slowest pipeline stage to complete. The cache memory reduces the memory access time and makes pipelining useful.	-
68.	Delayed branching	-	A technique called delayed branching can minimize the penalty incurred as a result of conditional branch instructions.	-
69.	Four stages in the instruction pipelining	-	S1- Fetch (F): Read instruction from the memory. S2-Decode (D): Decode the opcode and fetch source operand (s) if necessary. S3-Execute (E): Perform the operation specified by the instruction. S4-Store (S): Store the result in the	-

			destination.	
70.	Hazard	-	Any condition that causes the pipeline to stall is called as hazard	-
71.	Data Hazard	-	A condition in which either the source or destination operands of an instruction are not available at the time expected in the pipeline	-
72.	Instruction hazard	-	A data miss in the cache memory might require a fetch from the main memory. this condition is called as instruction hazard	-
73.	Structural hazard	-	When two instructions require the use of a given hardware resource at the same time then this condition is called as structural hazard	-
74.	PDU	-	Prefetch and Dispatch Unit of the processor is responsible for maintaining a continuous supply of instructions for the execution unit	-
75.	MBR	-	Memory Buffer register (MBR) holds the instruction during instruction execution by the processor	-
Unit-IV : Memory System				
76.	Features of a ROM cell	-	It can hold one bit data. It can hold data even if power is turned off. It is read only	-
77.	Static Memory	-	Memories that consists of circuits capable of retaining their state as long as power is applied is called Static memories.	-
78.	Word count	-	The number of words in the block to be transferred.	-
79.	Mapping techniques	-	1. Direct-mapping technique 2. Associative-mapping technique The associative mapping technique	-

			is further classified as fully associative and set associative techniques	
80.	Virtual memory	-	Techniques that automatically move program and datablocks into the physical main memory when they are required for execution are called as virtual memory.	-
81.	Memory Cycle time	-	It is the minimum time delay required between the initiation of two successive memory operations.	-
82.	Memory Management Unit	-	It is a special memory control circuit used for implementing the mapping of the virtual address space onto the physical memory.	-
83.	Memory latency	-	It is used to refer to the amount of time it takes to transfer a word of data to or from the memory.	-
84.	Memory contoller	-	A memory controller is a circuit which is interposed between the processor and the dynamic memory. It is used for performing multiplexing of address bits	-
85.	Load through	-	When a read miss occurs for a system with cache the required word may be sent to the processor as soon as it is read from the main memory instead of loading in to the cache.	-
86.	Hit	-	A successful access to data in cache memory is called hit.	-
87.	Hit rate	-	The number of hits stated as a fraction of all attempted access.	-
88.	Miss rate	-	It is the number of misses stated as a fraction of attempted accesses.	-
89.	Miss penalty	-	The extra time needed to bring the	-

			desired information into the cache.	
90.	Prefetch instructions	-	Prefetch Instructions are those instructions which can be inserted into a program either by the programmer or by the compiler.	-
91.	Pages	-	All programs and data are composed of fixed length units called pages each consists of blocks of words that occupies contiguous locations in main memory.	-
92.	Dirty bit	-	The cache location is updated with an associated flag bit called dirty bit.	-
93.	Write miss	-	During the write operation if the addressed word is not in cache then said to be write miss.	-
94.	virtual address	-	The binary address that the processor used for either instruction or data called as virtual address.	-
95.	Virtual page number	-	Each virtual address generated by the processor whether it is for an instruction fetch is interpreted as a virtual page.	-
96.	Page frame	-	An area in the main memory that can hold one page is called as page frame.	-
97.	Disk drive	-	The electromechanical mechanism that spins the disk and moves the read/write heads called disk drive.	-
98.	Disk controller	-	The electronic circuitry that controls the operation of the system called as disk controller.	-
99.	Error checking	-	It computes the error correcting code (ECC)value for the data read from a given sector and compares it with the corresponding ECC value	-

			read from the disk.	
100.	Main memory address	-	The address of the first main memory location of the block of words involved in the transfer is called as main memory address.	-
Unit-V : Input / Output Organization				
101.	Functions of IO system	-	Interface to the CPU and memory through the system bus. Interface to one or more IO devices by tailored data link.	-
102.	Input-output interface	-	Input-output interface provides a method for transferring binary information between internal storage, such as memory and CPU registers, and external I/O devices	-
103.	DMA Controller	-	The I/O device interface control circuit that is used for direct memory access is known as DMA controller.	-
104.	Polling	-	Polling is a scheme or an algorithm to identify the devices interrupting the processor. Polling is employed when multiple devices interrupt the processor through one interrupt pin of the processor.	-
105.	Synchronous bus	-	Synchronous buses are the ones in which each item is transferred during a time slot(clock cycle) known to both the source and destination units. Synchronization can be achieved by connecting both units to a common clock source.	-
106.	Asynchronous bus	-	Asynchronous buses are the ones in which each item being transferred is accompanied by a control signal that indicates its presence to the destination unit. The	-

			destination can respond with another control signal to acknowledge receipt of the items.	
107.	Interrupt	-	An interrupt is any exceptional event that causes a CPUU to temporarily transfer control from its current program to another program , an interrupt handler that services the event in question.	-
108.	Exception	-	The term exception is used to refer to any event that causes an interruption	-
109.	Bus arbitration	-	it is process by which the next device to become the bus master is selected and bus mastership is transferred to it.	-
110.	Parallel port	-	A parallel port transfers data in the form a number of bits, typically 8 to 16, simultaneously to or from the device.	-
111.	Serial port	-	A serial port transfers and receives data one bit at a time.	-
112.	Peripheral component interconnect	-	The Peripheral component interconnect (PCI) bus is a standard that supports the any particular processor.	-
113.	SCSI	-	It is the acronym for small computer system interface. Devices such as disks are connected to a computer via 50-wire cable, which can be upto 25 meters in length and can transfer data at rate up to 55 megabytes/s.	-
114.	USB	-	The Universal Serial Bus (USB) is an industry standard developed to provide two speed of operation called low-speed and full-speed. They provide simple, low cost and	-

			easy to use interconnection system.	
115.	Locality of Reference	-	Many instruction in localized area of the program are executed repeatedly during some time period and the remainder of the program is accessed relatively infrequently this is referred as locality of reference.	-
116.	Interface	-	The word interface refers to the boundary between two circuits or devices	-
117.	Reliability	-	Means feature that help to avoid and detect such faults	-
118.	Availability	-	Means features that follow the system to stay operational even often faults do occur.	-
119.	Standard I/O Interface	-	*SCSI (small computer system interface),bus standards *Back plane bus standards *IEEE 796 bus (multibus signals) *NUBUS & IEEE 488 bus standard	-
120.	I/O Devices	-	*Video terminals *Video displays *Alphanumeric displays *Graphics displays * Flat panel displays *Printers	-
121.	Bus master	-	The device that is allowed to initiate data transfers on the bus at any given time is called as Bus master	-
122.	Bus Arbitration	-	Bus Arbitration refers to the process by which the current bus master accesses and then leaves the control	-

			of the bus and passes it to the another bus requesting processor unit.	
123.	Distributed Arbitration	-	All the buses waiting to use the bus have equal responsibility in carrying out the arbitration process without using the central arbiter	-
124.	Initiator	-	The device that initiates data transfer by issuing read or write commands on the bus is called as initiator	-
125.	Target	-	The addressed device that responds to read and write commands is called a target	-
Placement Questions				
126.	Address space	-	In a virtual memory system, the addresses used by the programmer belongs to Address space	-
127.	Write-back	-	The method for updating the main memory as soon as a word is removed from the Cache is called write-back.	-
128.	Divide overflow	-	Divide overflow is generated when the sign of the dividend is same as that of divisor.	-
129.	Internal interrupt	-	Stack overflow occurs while execution of a program due to logical faults. So it is a program dependent, hence interrupt activated	-
130.	Stack-organized architecture	-	In stack organized architecture push and pop instruction is needs a address field to specify the location of data for pushing into the stack and destination location during pop operation but for logic and arithmetic operation the instruction does not need any address field as	-

			it operates on the top two data available in the stack.	
131.	Assembler	-	Address symbol table is generated by the Assembler. During the first pass of assembler address symbol table is generated which contains the label used by the programmer and its actual address with reference to the stored program.	-
132.	2's complement	-	The negative numbers in the binary system can be represented by 2's complement	-
133.	Address fault	-	An attempt to access a location not owned by a Program is called Address fault	-
134.	Hardware interrupt	-	An interrupt for which hardware automatically transfers the program to a specific memory location is known as Hardware interrupt	-
135.	System Software	-	It is a collection of programs that are executed as needed to perform functions such as receiving and interpreting user commands, entering and editing application programs and storing them as files in secondary storage devices. For example, Assembler, Linker, Compiler etc.	-
136.	Multiple Functional Units	-	System may have two or more ALUs so that they can execute two or more instructions at the same time.	-
137.	Multiple Processors	-	System may have two or more processors operating concurrently.	-
138.	Parallel Processing	-	To fulfill increasing demands for higher performance it is necessary to process data concurrently to achieve better throughput instead	-

			of processing each instruction sequentially as in a conventional computer. Processing data concurrently is known as parallel processing.	
139.	Multicore	-	A multicore is an architecture design that places multiple processors on a single die (computer chip) to enhance performance and allow simultaneous processing of multiple tasks more efficiently. Each processor is called a core. The multicore architecture designs are known as Chip Multiprocessors (CMPs) because they allow single chip multiprocessing.	-
140.	Interleaved or fine-grained multithreading	-	The processor executes two or more threads at a time. It switches from one thread to another at each clock cycle. During execution, if a thread is blocked because of data dependencies or memory latencies, that thread is skipped and a ready thread is executed.	-
141.	Blocked or coarse-grained multithreading	-	The processor executes instructions of a thread sequentially and if an event (e.g. cache miss) that causes any delay occurs, it switches to another thread.	-
142.	Strong scaling	-	Speedup achieved on a multiprocessor without increasing the size of the problem.	-
143.	Weak scaling	-	Speedup achieved on a multiprocessor while increasing the size of the problem proportionally to the increase the number of the processor.	-

144.	Locality of Reference	-	The program may contain a simple loop, or a few procedures that repeatedly call each other. The point is that many instructions in localized area of the program are executed repeatedly during some time period and the remainder of the program is accessed relatively infrequently	-
145.	Translation Look-aside Buffer	-	To support demand paging and virtual memory processor has to access page table which is kept in the main memory. To avoid the access time and degradation of performance, a small portion of the page table is accommodated in the memory management unit. This portion is called Translation Look-aside Buffer.	-
146.	Exception	-	The term exception is often used to refer to any event that causes an interruption	-
147.	Tri-state gates	-	The gates having three output states: logic 0, logic 1 and high-impedance are called tri-state gates.	-
148.	Underflow	-	In a single precision, if the number requires an exponent less than -126 or in a double precision, if the number requires an exponent less than -1022 to represent its normalized from to underflow occurs.	-
149.	Overflow	-	In a single precision, if the number requires an exponent greater than +127 or in a double precision, if the number requires an exponent greater than +1023 to represent its normalized form the overflow occurs.	-

150.	Mapping functions	-	The memory blocks are mapped on to the cache with the help of Mapping functions	-

Faculty Team Prepared **Signatures**

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