MUTHAYAMMAL ENGINEERING COLLEGE

(An Autonomous Institution)

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Rasipuram - 637 408, Namakkal Dist., Tamil Nadu

Estd. 2000

MUST KNOW CONCEPTS

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Subject		19ADC03 / Processor Architecture		
S. No	**Term**	**Notation (Symbol)**	**Concept/Definition/Meaning/Units/Equation/ Expression**	**Units**
UNIT – I INTRODUCTION TO 80X86 PROCESSOR				
1.	Chip		A chip is also called an integrated circuit of semiconductor material embedded with integrated circuitry.	
2.	Microprocessor		It is a program controlled semiconductor device (IC), which fetches, decode and executes instructions.	
3.	80X86 Microprocessor		16/32 bit processors like 80286, 80386, 80486 and Pentium processors.	
4.	80386 Microprocessor		32 bit microprocessor. It has 32 bit internal registers, a 32 bit data bus and a 32 bit address bus.	
5.	80386 Features		Different operating modes ,new register set ,expanded instruction set, memory management unit, page translation mechanism, and task management functions.	
6.	80386 Architecture		It consists of 6 functional units.	
7.	Bus interface unit		Bus interface unit accepts internal request for code fetch and for data transfer from the code fetch and from the execution unit.	
8.	Code Fetch unit		Code Fetch unit fetches sequentially the instruction byte stream from the memory.	
9.	Instruction decode unit		Instruction decode unit takes instruction byte from the code fetch queue and translates them into micro code.	
10.	Execution unit		Execution unit reads the instruction from the instruction queue and executes the instruction. It has 3 units 1. Control unit 2. Data unit 3. Protection test unit	
11.	Segmentation unit		Translates logical address into a linear address at the request of the execution unit.	
12.	Paging unit		Paging translates linear address into a physical	

			address. if paging is enabled.	
13.	Pin description		The number of changes have been made in 80386DX hardware to make it more versatile and improve its function.	
14.	Functional Description		These signals are separated in to 4 groups. 1. Memory/IO Interface 2. Interrupt interface 3. DMA interface 4. Coprocessor interface	
15.	Register set		The first item of interest to the programmer is the register set. It can be categories according to their usage. • General purpose register • Segment register • Index ,pointer ,and base register • Flag register • System address register • Control register • Debug register	
16.	80386 operating modes		1. Real mode 2. Protected mode 3. Virtual 8086 mode	
17.	80386 Real mode		80386 Mp can operated in real mode or protected mode. when 80386 is reset or powered up it is in real mode	
18.	Segmentation		The segment in real mode can be read, write or executed, i.e. no protection is available	
19.	Bus cycles		Memory/IO Interface signals It includes data bus, separate address bus and five bus status signals and three bus control signals	
20.	Data bus		It has 32 pins.these lines used nto transfer 8,16,24,32 bit data at one time	
21.	Separate address bus		80386 generates 32 bit address.	
22.	Bus status signals		The status signal decides the bus cycle to be performed. • Address status • Write/read • Memory/IO • Data/control • lock	
23.	Bus control signals		It allows external logic to control the bus cycle. Ready, next address request, bus size 16.	
24.	Address pipelined		The method of specifying the data to be operated by the instruction is called addressing • Register operand addressing • Memory operand addressing. • Immediate operand addressing	
25.	Memory and I/O organization		The memory and I/O organisation is the process of interfacing memories to microprocessor and allocating	

			addresses to each memory locations	
UNIT II Assembly language programming				
26.	Assembly language progamming			
27.	*Instruction*		DATA TRANSFER INSTRUCTIONS: LOGICAL INSTRUCTIONS SHIFT AND ROTATE INSTRUCTIONS: ARITHMETIC INSTRUCTIONS: TRANSFER INSTRUCTIONS:	
28.	ASSEMBLER DIRECTIVES		Assembly Directives are instructions that are executed by the Assembler at assembly time, not by the CPU at run time. They can make the assembly of the program dependent on parameters input by the programmer, so that one program can be assembled different ways.	
29.	PROCEDURE**S**		A procedure is a collection of instructions to which we can direct the flow of our program, and once the execution of these instructions is over control is given back to the next line to process of the code which called on the procedure	
30.	Macros		Definition of the macro A macro is a group of repetitive instructions in a program which are codified only once and can be used as many times as necessary	
31.	Timing delay and loops.		Procedure used to design a specific delay. A register is loaded with a number , depending on the′ time delay required and then the register is decremented until it reaches zero by setting up a loop with c.	
32.	DOS internal and DOS calls		To use a DOS function call in a DOS program, place the function number in AH and other data that might be necessary in other registers	
33.	Programmable peripheral device		If the functions performed by peripheral devices can be altered or changed by a program instruction then the peripheral device is called programmable devices.	
34.	Modes of Operation supported by 8255		Mode-0 Simple I/O port Mode-1 Handshake I/O port Mode-2 Bidirectional I/O port	
35.	Control Word		It is a word stored in a register (control register) used to control the operation of a program digital device.	
36.	Size of Ports in 8255		Port-A : 8-bits Port-B : 8-bits Port-CU : 4-bits Port-CL : 4-bits	
37.	Use of 8251 Chip		8251 chip is mainly used as the asynchronous serial interface between the processor and the external	

			equipment.	
38.	Expand USART		USART stands for universal synchronous/Asynchronous Receiver/ Transmitter.	
39.	USART		It is a programmable communication interface that can communicate by using either synchronous or asynchronous serial data.	
40.	Memory Mapping		The assignment of memory addresses to various registers in a memory chip is called as memory mapping.	
41.	I/O Mapping		The assignment of addresses to various I/O devices in the memory chip is called as I/O mapping.	
42.	Function of Mode Set Register in 8257		The function of the mode set register is to enable the DMA channels individually and also to set the various modes of operation.	
43.	Count Register		16-bit Count register is used for ascertaining that the data transfer through a DMA channel ceases or stops after the required number of DMA cycles.	
44.	Use of Modem Control Unit in 8251		The modem control unit handles the modem handshake signals to coordinate the communication between the modem and the USART.	
45.	Output Modes used in 8279		Display Scan. Display Entry	
46.	Display Entry		8279 allows options for data entry on the displays. The display data is entered for display from the right side or from the left side.	
47.	Display Scan		In this mode, 8279 provides 8 or 16 character-multiplexed displays those can be organized as dual 4-bit or single 8-bit display units.	
48.	Scan Counter		The scan counter has two modes to scan the key matrix and refresh the display.	
49.	Types of Command Words used in 8259		1. Initialization command words (ICWs) 2. Operation command words (OCWs)	
50.	Function Of GATE Signal In Timer 8254		In timer 8254, the GATE signal act as a control signal to start, stop or maintain the counting process.	
51.	Functions Performed By INTEL 8251		8251 is used for converting parallel data to serial data or vice versa.	
52.	Baud Rate		The number of bits transmitted per second is called baud rate. The standard baud rates are 75, 110, 150, 300, 600, 1100, 2400, 9600 and 19200.	
53.	Types Of DMA		The different types of DMA data transfer are cycle stealing DMA, Block transfer DMA and Demand transfer DMA.	
54.	Handshake Port		The port used for exchange the signals between I/O devices and port or between port and the processor for exchanging or informing various condition of the device is called handshake port.	

55.	Simplex Transmission		Data is transmitted in only one direction.	
56.	Duplex Transmission		Data is transmitted in both directions	
57.	Data Amplifier		Data Amplifiers are required to separate the valid data from the time multiplexed address data signal.	
UNIT III MEMORY MANAGEMENT				
58.	Memory Mapping		The assignment of memory addresses to various registers in a memory chip is called as memory mapping.	
59.	Segmentation		A segment selector is loaded into a segment register (cs, ds, etc.) to select one of the regular segments in the system as the one addressed via that segment register .	
60.	80386Dx descriptor		Descriptor Tables GDT, LDT, IDT, descriptor cache, Code, data and stack descriptors, system descriptors, privilege levels, Segmentation .	
	Memory management through segmentation		This registers are not available for programmers, rather they are internally used to store the descriptor information, like attributes, limit and base addresses of segments.	
61.	Types of segment register		segment registers have corresponding six 73 bit descriptor registers. Each of them contains 32 bit base address,32 bit base limit and 9 bit attributes. These are automatically loaded when the corresponding segments are loaded with selectors.	
62.	GDTR and IDTR:		These registers hold the 32-bit linear base address and 16-bit limit of the GDT and IDT respectively. The GDT and IDT segments, since they are global to all tasks in the system, and defined by 32-bit linear addresses (subject to page translation if paging is enabled) and 16-bit limit values	
63.	LDTR and TR		These registers hold the 16-bit selector for the LDT descriptor and the TSS descriptor, respectively. The LDT and TSS segments, since they are task specific segments, are defined by selector values stored in the system segment registers	
64.	Memory addressing in Real Mode		In the real mode, the can address at the most 1Mbytes of physical memory using address lines A0 -A19.	
65.	Paging unit		Paging unit is disabled in real addressing mode, and hence addresses are the same as the physical addresses	
66.	Protected mode addressing without paging		All the capabilities of 80386 are available for utilization in its protected mode of operation	
67.	paging		Paging is another type of memory management useful for virtual memory multitasking operating systems	
68.	Linear to physical		The upper 20 bit page frame address is combined with the lower 12 bit of the linear address. The	

	address		address bits A12- A21 are used to select the 1024 page table entries. The page table can be shared between the tasks.	
		UNIT IV	MULTITASKING, INTERRUPTS ,EXCEPTIONS AND I/O	
69.	EXCEPTIONS		Exceptions are synchronous events that are the responses of the CPU to certain conditions detected during the execution of an instruction	
70.	INTERRUPTS		Interrupts are asynchronous events typically triggered by external devices needing attention.	
71.	DEBUG EXCEPTIONS		Debug exception may be reflected back to an applications program if it results from the trap flag (TF).	
72.	Virtual Mode		If this flag is set, the 80386 enters the virtual 8086 mode within the protection mode. This is to beset only when the 80386 is in protected mode	
73.	RF MODE		This flag is used with the debug register breakpoints. It is checked at the starting of every instruction cycle and if it is set, any debug fault is ignored during the instruction cycle.	
74.	RELATED DESCRIPTOR		The 80386 descriptors have a 20-bit segment limit and 32-bit segment address. The descriptor of 80386 are 8-byte quantities access right or attribute bits alongwith the base and limit of the segments.	
75.	Virtual to real mode		Once the 80386 enters the protected mode from the real mode, it cannot return back to the real mode without a reset operation	
76.	protected multitasking		the 80386 employs several special data structures. It does not, however, use special instructions to control multitasking; instead, it interprets ordinary control-transfer instructions differently when they refer to the special data structures	
77.	The registers and data structures that support multitasking ,		* Task state segment * Task state segment descriptor * Task register * Task gate descriptor	
78.	Interrupts and exceptions		. Interrupts and exceptions can cause task switches (if needed in thesystem design). The	

			processor not only switches automatically to the task that handles the interrupt or exception, but it automatically switches back to the interrupted task when the interrupt or exceptionhas been serviced. Interrupt tasks may interrupt lower-priority.	
79.	Task State Segment		All the information the processor needs in order to manage a task is stored in a special type of segment, a task state segment (TSS).	
80.	TSS Descriptor		The task state segment, like all other segments, is defined by a descriptor.	
81.	Task Register		The task register has both a "visible" portion (i.e., can be read and changed by instructions) and an "invisible" portion (maintained by the processor to correspond to the visible portion; cannot be read by any instruction).	
82.	Task Gate Descriptor		A task gate descriptor provides an indirect, protected reference to a TSS	
83.	**Task Switching**		The 80386 switches execution to another task in any of four cases: 1. The current task executes a JMP or CALL that refers to a TSS descriptor. 2. The current task executes a JMP or CALL that refers to a task gate. 3. An interrupt or exception vectors to a task gate in the IDT. 4. The current task executes an IRET when the NT flag is set.	
84.	**Task Linking**		The back-link field of the TSS and the NT (nested task) bit of the flag word together allow the 80386 to automatically return to a task that CALL ed another task or was interrupted by another task. When a CALL instruction, an interrupt instruction, an external interrupt, or an exception causes a switch to a new task, the 80386 automatically fills the back-link of the new TSS with the selector of the outgoing task's TSS and, at the same time, sets the NT bit in the new task's flag register.	

85.	Modifying Task Linkages		Any modification of the linkage order of tasks should be accomplished only by software that can be trusted to correctly update the back-link and the busy-bit. Such changes may be needed to resume an interrupted task before the task that interrupted it. Trusted software that removes a task from the back-link chain must follow one of the following policies	
86.	Task Address Space		The LDT selector and PDBR fields of the TSS give software systems designers flexibility in utilization of segment and page mapping features of the 80386	
87.	Task Linear-to-Physical Space Mapping		The choices for arranging the linear-to-physical mappings of tasks fall into two general classes: 1. One linear-to-physical mapping shared among all tasks. 2. Several partially overlapping linear-to-physical mappings.	
88.	**Task Logical Address Space**		By itself, a common linear-to-physical space mapping does not enable sharing of data among tasks. To share data, tasks must also have a common logical-to-linear space mapping; i.e., they must also have access to descriptors that point into a shared linear address space. There are three ways to create common logical-to-physical address-space mappings:	
UNIT V MICROCONTROLLERS				
89.	Microcontroller		A device which contains the microprocessor with integrated peripherals like memory, serial ports, parallel ports, timer/counter, interrupt controller, data acquisition interfaces like ADC, DAC is called microcontroller.	
90.	DPTR		DPTR stands for data pointer. DPTR consists of a high byte (DPH) and a low byte (DPL). Its function is to hold a 16bit address.	
91.	SP		SP stands for stack pointer. SP is a 8- bit wide register. It is incremented before data is stored during PUSH and CALL instructions.	
92.	Program Counter in 8051		The program counter keeps track of program execution. To execute a program the starting address of the program	

			is loaded in program counter.	
93.	Stack		Stack is a sequence of RAM memory locations defined by the programmer.	
94.	PSEN		PSEN stands for program store enable. In 8051 based system in which an external ROM holds the program code, this pin is connected to the OE pin of the ROM.	
95.	Special Functions Registers available in 8051		•Accumulator • B Register • Program Status Word. • Stack Pointer. • Data Pointer.• Port 0• Port 1• Port 2 • Port 3• Interrupt priority control register.• Interrupt enable control register.	
96.	NEU		The numeric execution unit executes all the instructions including arithmetic, logical transcendental, and data transfer instructions.	
97.	Register Banks		The 8051 uses 8 "R" registers which are used in many of its instructions. These "R" registers are numbered from 0 through 7 (R0, R1, R2, R3, R4, R5, R6, and R7). These registers are generally used to assist in manipulating values and moving data from one memory location to another.	
98.	DPL/DPH (Data Pointer Low/High)		The SFRs DPL and DPH work together to represent a 16-bit value called the Data Pointer.	
99.	PCON (Power Control)		The Power Control SFR is used to control the 8051's power control modes.	
100.	TCON (Timer Control)		The Timer Control SFR is used to configure and modify the way in which the 8051's two timers operate.	
101.	TMOD (Timer Mode)		The Timer Mode SFR is used to configure the mode of operation of each of the two timers.	
102.	TL0/TH0 (Timer 0 Low/High)		These two SFRs, taken together, represent timer 0.	
103.	TL1/TH1 (Timer 1 Low/High)		These two SFRs, taken together, represent timer 1.	
104.	SCON (Serial Control)		The Serial Control SFR is used to configure the behavior of the 8051's on-board serial port.	
105.	TL1/TH1 (Timer 1 Low/High)		These two SFRs, taken together, represent timer 1.	
106.	SBUF (Serial Control)		The Serial Buffer SFR is used to send and receive data via the on-board serial port.	
107.	IE (Interrupt Enable)		The Interrupt Enable SFR is used to enable and disable specific interrupts. The low 7 bits of the SFR are used to enable/disable the specific interrupts.	
108.	Jump Range		LJMP(Long jump)-address 16 AJMP(Absolute Jump)-address 11 SJMP(Short Jump)-relative address	
109.	Addressing Modes of 8051		Direct addressing Register addressing	

			Register indirect addressing. Implicit addressing Immediate addressing Index addressing	
110.	Interrupts Of 8051		INT0,TF0,INT1,TF1,R1&T1	
111.	PIC Microcontrollers		Peripheral Interface Controller was developed for supporting PDP computers to control its peripheral devices	
112.	Features of PIC		Speed, Instruction set simplicity, Power-on-reset and brown-out reset	
113.	Four Clock Sources		PIC microcontroller has four optional clock sources. Low power crystal – Mid range crystal – High range crystal – RC oscillator (low cost).	
114.	Low - end PIC Architectures		The microcontroller consisted of a simple processor executing 12-bit wide instructions with basic I/O functions.	
115.	Examples of Low - end PIC Architectures		The low-end device numbers are 12C5XX,16C5X,16C505	
116.	Mid range PIC architectures		Mid range PIC architectures are built by upgrading low-end architectures with more number of peripherals,	
117.	Examples Of Mid range PIC architectures		Mid-range devices are 16C6X , 16C7X , 16F87X.	
118.	WATCH DOG TIMER (WDT)		The Watchdog Timer is a free running on-chip RC oscillator which does not require any external components.	
119.	WDT PERIOD		The WDT has a nominal time-out period of 18 ms. The time-out periods vary with temperature, VDD and process variations from part to part.	
120.	Types Of CPU Registers		Working Register, Status Register, FSR, INDF, Program Counter.	
121.	Types Of Register File Structure		1.General Purpose Register 2.Special Purpose Register	
122.	Interrupt		The PIC16F8XX family has up to 11 sources of interrupt. The interrupt control register (INTCON) records individual interrupt requests in flag bits	
123.	CCP (Capture-Compare PWM)		The CCP module(s) can operate in one of three modes 16-bit capture, 16-bit compare, or up to 10-bit Pulse Width Modulation (PWM)	
124.	Capture mode		Captures the 16-bit value of TMR1 into the CCPRxH: CCPRxL register pair.	
125.	Compare mode		Compare mode compares the TMR1H:TMR1L register pair to the CCPRxH: CCPRxL register pair.	
126.	PWM mode		PWM mode compares the TMR2 register to a 10-bit duty cycle register (CCPRxH:CCPRxl) as well as to an 8-bit period register (PR2).	
127.	Looping		In this technique, the Programming Techniques using 8085 is instructed to execute certain set of instructions repeatedly to execute a particular task number of times.	
128.	Counting		This technique allows programmer to count how many times the instruction/set of instructions are executed.	

129.	Unconditional Return instruction		RET is the instruction used to mark the end of sub-routine. It has no parameter.	
130.	Conditional Return instruction		By these instructions program control is transferred back to main program and value of PC is popped from stack only if condition is satisfied.	
131.	Advantages of Subroutine		Decomposing a complex programming task into simpler steps. Reducing duplicate code within a program. Enabling reuse of code across multiple programs. Improving tractability or makes debugging of a program easy.	
Placement Oriented Questions				
132.	Which Stack Is Used In 8085?		LIFO (Last In First Out) stack is used in 8085.In this type of Stack the last stored information can be retrieved first	
133.	In 8085 Which Is Called As High Order / Low Order Register?		Flag is called as Low order register & Accumulator is called as High order Register.	
134.	How Many Bit Combinations Are There In A Byte?		Byte contains 8 combinations of bits.	
135.	What Are The Various Registers In 8085?		Accumulator register, Temporary register, Instruction register, Stack Pointer, Program Counter are the various registers in 8085	
136.	Give Examples For Micro Controller?		Z80, Intel MSC51 &96, Motorola are the best examples of Microcontroller.	
137.	What Is Clock Frequency For 8085?		3 MHz is the maximum clock frequency for 8085.	
138.	In What Way Interrupts Are Classified In 8085?		In 8085 the interrupts are classified as Hardware and Software interrupts.	
139.	What Is The RST For The TRAP?		RST 4.5 is called as TRAP.	
140.	How Many Interrupts Are There In 8085?		There are 12 interrupts in 8085.	
141.	Which Interrupt Has The Highest Priority?		TRAP has the highest priority	
142.	What Happens When HLT Instruction Is		The Micro Processor enters into Halt-State and the buses	

	Executed In Processor?		are tri-stated.	
143.	Example For Non-Maskable Interrupts?		Trap is called as Non-Maskable interrupts, which is used during emergency condition.	
144.	Name The 1st / 2nd / 3rd / 4th Generation Processor?		The processor are made of PMOS / NMOS / HMOS / HCMOS technology which is called 1st / 2nd / 3rd / 4th generation processor, and that is made up of 4 / 8 / 16 / 32 bits respectively.	
145.	Why Crystal Is Being Preferred As A Clock Source?		Reasons-high stability, large Q (Quality Factor) & the frequency that doesn't drift with aging. so crystal is used as a clock source most of the times.	
146.	What Are The Various Flags Used In 8085?		Sign flag, Zero flag, Auxiliary flag, Parity flag, Carry flag.	
147.	What Is Tri-State Logic?		Three Logic Levels are used and they are High, Low, High impedance state. The high and low are normal logic levels & high impedance state is electrical open circuit conditions. Tri-state logic has a third line called enable line.	
148.	What Is A Microprocessor?		Microprocessor is a program-controlled device that fetches the instructions from memory, decode it & executes the instructions. Generally Microprocessor are single- chip devices.	
149.	Accumulator		Accumulator is an 8 bit register which stores data and performs arithmetic and logical operations. The result of the operation is stored in the accumulator. It is designated by the letter 'A'.	
150.	Micro Controller		A microcontroller is a compact integrated circuit designed to govern a specific operation in an embedded system. A typical microcontroller includes a processor, memory and input/output (I/O) peripherals on a single chip.	
Faculty Team Prepared			Mrs. P.Subhasundari	Signature

HoD