# MUTHAYAMMAL ENGINEERING COLLEGE

(An Autonomous Institution)

(Approved by AICTE, New Delhi, Accredited by NAAC & Affiliated to Anna University)

Rasipuram - 637 408, Namakkal Dist., Tamil Nadu

Estd. 2000

IQAC

**L1**

## LECTURE HANDOUTS

**EEE**

**II/III**

**Course Name with Code** :**19EEC03 / Linear Integrated Circuits**

**Course Faculty** :**Mr.R.Suresh**

**Unit** :**I- Characteristics of Opamp** **Date of Lecture:**

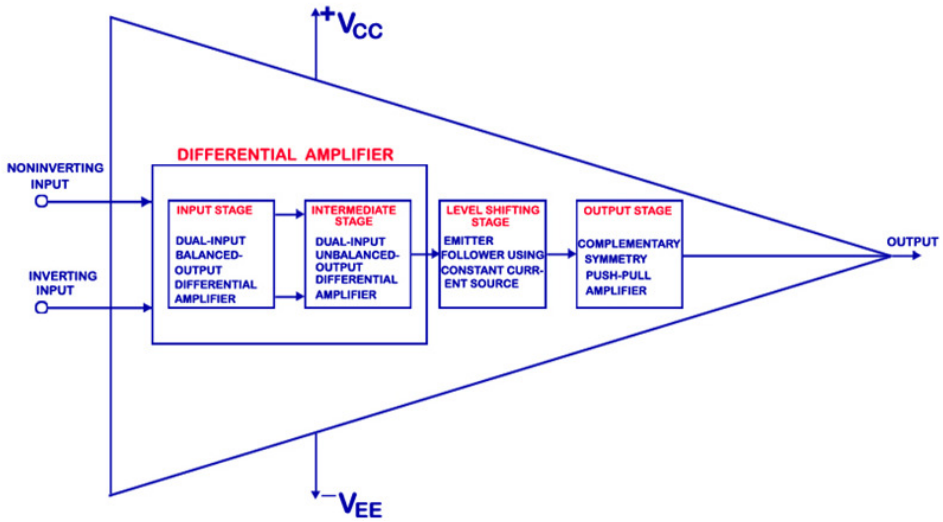
**Topic of Lecture:** Block Diagram of a Typical Opamp

**Introduction :**An op-amp is a multi-stage , direct coupled, high gain negative feedback amplifier that has one or more differential amplifiers and its concluded with a level translator and an output stage. A voltage-shunt feedback is provided in an op-amp to obtain a stabilized voltage gain.

**Prerequisite knowledge for Complete understanding and learning of Topic:**
Electronic Devices

**Detailed content of the Lecture:**

- The main use of an op-amp is to amplify ac and dc input signals and was initially used for basic mathematical operations such as addition, subtraction, multiplication, differentiation and integration. Nowadays , the application of op-amp's varies from ac and dc signal amplification to use in active filters, oscillators, comparators, voltage regulators, instrumentation and control systems, pulse generators, square wave generators and many more electronic circuits.
- For the design of all these circuits the op-amp's are manufactured with integrated transistors, diodes, capacitors and resistors, thus making it an extremely compact, multi tasking, low cost, highly reliable and temperature stable integrated circuit.
- It is also designed in such a way that the external characteristics can be changed with the addition of external components like capacitors and resistors.
- Thus it can act as a complete amplifier with various characteristics.



- The op-amp begins with a differential amplifier stage, which operates in the differential mode. Thus the inputs noted with '+' & '- ' .
- The positive sign is for the non-inverting input and negative is for the inverting input.
- The non-inverting input is the ac signal (or dc) applied to the differential amplifier which produces the same polarity of the signal at the output of op-amp.
- The inverting signal input is the ac signal (or dc) applied to the differential amplifier. This produces a 180 degrees out of phase signal at the output.
- The inverting and non-inverting inputs are provided to the input stage which is a dual input, balanced output differential amplifier.
- The voltage gain required for the amplifier is provided in this stage along with the input resistance for the op-amp.
- The output of the initial stage is given to the intermediate stage, which is driven by the output of the input stage.
- In this stage direct coupling is used, which makes the dc voltage at the output of the intermediate stage above ground potential.
- Therefore, the dc level at its output must be shifted down to 0Volts with respect to the ground.

**Video Content / Details of website for further learning (if any):**

https://nptel.ac.in/courses/108108111/

**Important Books/Journals for further learning including the page nos.:**


- D.RoyChoudhary, SheilB.Jani, "Linear Integrated Circuits", II edition, New Age, pp. 1-3, 2015


**Course Faculty**

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**L2**

## LECTURE HANDOUTS

**EEE**

**II/III**

**Course Name with Code** :**19EEC03 / Linear Integrated Circuits**

**Course Faculty** : **Mr.R.Suresh**

**Unit** :**I- Characteristics of Opamp** **Date of Lecture:**

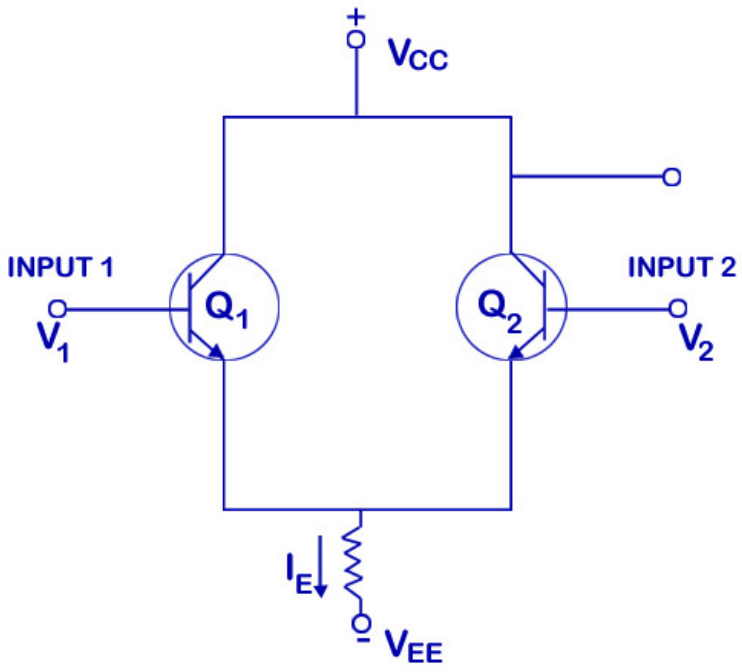
**Topic of Lecture:** Characteristics of Ideal Opamp

- **Introduction :**A differential amplifier circuit that is modified to use an op-amp. This constitutes the basic op-amp circuit and explains about the input characteristics of a typical op-amp IC

**Prerequisite knowledge for Complete understanding and learning of Topic:**

Electronic Devices

**Detailed content of the Lecture:**




- The basic configuration of the circuit is drawn above.
- Two transistors Q1 and Q2 are provided, in which the input is provided to the base of both the transistors.
- Both the transistor emitters are connected to a common emitter RE so that the two input signals are affected by either or both input signals.
- Two supply voltages VCC and VEE are connected to both the collectors and emitters QI and Q2.
- In the circuit diagram, there is no indication of common ground point.

- It must be understood that the opposite points of both positive and negative voltage supplies are connected to the ground.
- When input at point 1(V1) increases , the emitter current of transistor Q1 increases, and thus causes an increase of voltage at top of the emitter resistance RE.
- Thus it decreases the base-emitter voltage VBE of transistor Q2.
- Thus, when VBE of Q2 decreases, there is less current flow in the transistor Q2.This brings a voltage drop in the collector resistance RC and an increase in the output voltage VOUT as it is the difference between the collector supply voltage VCC and voltage drop in collector resistance RC (ICRC).
- This brings us to the conclusion that there is will be an increase in output voltage when there is an increase in input voltage V1.
- This why V1 is considered as the non-inverting input.
- Vout is in phase with V1.
- In another instant, when the voltage V2 increases, the collector current of Q2 increases, and makes way for a voltage drop in collector resistance and thus a decreased output voltage VOUT.
- This is why V2 is considered as the inverting input. VOUT is 180 degrees out of phase with V2.
- An ideal op amp is usually considered to have the following characteristics
- Infinite open-loop gain $G = v_{out} / v_{in}$
- Infinite input impedance $R_{in}$, and so zero input current
- Zero input offset voltage
- Infinite output voltage range
- Infinite bandwidth with zero phase shift and infinite slew rate
- Zero output impedance $R_{out}$
- Zero noise
- Infinite common-mode rejection ratio (CMRR)
- Infinite power supply rejection ratio.

These ideals can be summarized by the two "golden rules":

- In a closed loop the output attempts to do whatever is necessary to make the voltage difference between the inputs zero.
- The inputs draw no current.

**Video Content / Details of website for further learning (if any):**

https://nptel.ac.in/courses/108108111/

**Important Books/Journals for further learning including the page nos.:**


- D.RoyChoudhary, SheilB.Jani, “Linear Integrated Circuits”, II edition, New Age, pp. 5-7, 2015


**Course Faculty**

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**L3**

## LECTURE HANDOUTS

**EEE**

**II/III**

**Course Name with Code** :**19EEC03 / Linear Integrated Circuits**

**Course Faculty** : **Mr.R.Suresh**

**Unit** :**I- Characteristics of Opamp** **Date of Lecture:**

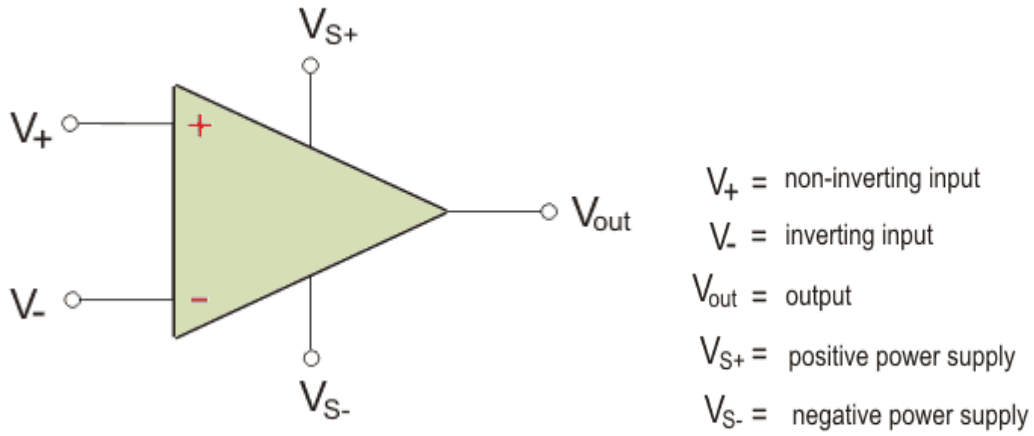
**Topic of Lecture:** Characteristics of Practical OpAmp

**Introduction :** Operational amplifier or op amps as they are usually referred are linear devices that can give ideal DC amplification. They are fundamentally voltage amplifying devices used with external feedback components like resistors or capacitors.

**Prerequisite knowledge for Complete understanding and learning of Topic:**
Electronic Devices

**Detailed content of the Lecture:**

- An **op amp** is a three terminal device, with one terminal called the inverting input, other the non-inverting input and the last one is the output. Below is a diagram of a typical op amp:
- As you can see from the diagram, op amp has three terminals for input and output and 2 for power supply.




**Open Loop Voltage Gain(A)**

The open loop voltage gain without any feedback for an ideal op amp is infinite. But typical values of open loop voltage gain for a real op amp ranges from 20,000 to 2, 00,000. Let the input voltage be $V_{in}$. Let A be the open loop voltage gain. Then the output voltage is $V_{out} = AV_{in}$. The value of a typically is in the range specified above but for an ideal op amp, it is infinite.

**Input Impedance($Z_{in}$)**

Input Impedance is defined as the input voltage by the input current. The input impedance of an ideal op amp is infinite. That is there no current flowing in the input circuit. However, an ideal op amp has certain current flowing in the input circuit of the magnitude of few pico-amps to a few milli-amps.

**Output Impedance ($Z_{out}$)**

Output impedance is defined as the ratio of the output voltage to the input current. The output impedance of an ideal op amp is zero, however, real op amps have an output impedance of 10-20 kΩ. An ideal op amp behaves like a perfect voltage source delivering current without any internal losses. The internal resistance reduce the voltage available to the load.

**Bandwidth(BW)**

An ideal op amp has an infinite bandwidth that is it can amplify any signal from DC to the highest AC frequencies without any losses. So therefore, an ideal op amp is said to have infinite frequency response. In real op amps, the bandwidth is generally limited. The limit depends on the gain bandwidth (GB) product. GB is defined as the frequency where the amplifier gain becomes unity.

**Offset Voltage($V_{io}$)**

The offset voltage of an ideal op amp is zero, which means that the output voltage will be zero if the difference between the inverting and non-inverting terminal is zero. If both the terminals are grounded, the output voltage will be zero. But real **op amps** have an offset voltage.

**Common Mode Rejection Ratio(CMRR)**

Common mode refers to the situation when the same voltage is applied to both the inverting and non-inverting terminal of the op amp. The common mode rejection refers to the ability of the op amp to reject the common mode signal. Now we are in a position to understand the term common mode rejection ratio.

- The common mode rejection ratio refers to the measure of the ability of the op amp to reject the common mode signal. Mathematically it is defined as
- Where, $A_D$ is the differential gain of the op amp, ∞ for an ideal op amp. $A_{CM}$ refers to the common mode gain of the op-amp.
- The CMRR of an ideal op amp is ∞. That means it is able to reject all common mode signal. Also from the formula, we can see the $A_D$ is infinite for an ideal op amp and $A_{CM}$ is zero. Therefore the CMRR of an ideal op-amp is infinite. Therefore it will reject any signal which is common to both.
- However, real omp have finite CMRR, and does not reject all common mode signals.

**Video Content / Details of website for further learning (if any):**

https://nptel.ac.in/courses/108108111/

**Important Books/Journals for further learning including the page nos.:**


- D.Roy Choudhary, Sheil B.Jani, "Linear Integrated Circuits", II edition, New Age, pp. 11-14, 2015


**Course Faculty**

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**L4**

## LECTURE HANDOUTS

**EEE**

**II/III**

**Course Name with Code** :**19EEC03 / Linear Integrated Circuits**

**Course Faculty** : **Mr.R.Suresh**

**Unit** :**I- Characteristics of Opamp** **Date of Lecture:**

**Topic of Lecture:** Parameters of Opamp

**Introduction :** An Operational Amplifier, or op-amp for short, is fundamentally a voltage amplifying device designed to be used with external feedback components such as resistors and capacitors between its output and input terminals. These feedback components determine the resulting function or "operation" of the amplifier and by virtue of the different feedback configurations whether resistive, capacitive or both, the amplifier can perform a variety of different operations, giving rise to its name of "Operational Amplifier".

**Prerequisite knowledge for Complete understanding and learning of Topic:**

Electronic Devices

**Detailed content of the Lecture:**

- COMMON-MODE REJECTION (CMRR)
- COMMON-MODE INPUT VOLTAGE
- INPUT OFFSET VOLTAGE
- INPUT BIAS CURRENT
- INPUT IMPEDANCE
- INPUT OFFSET CURRENT
- OUTPUT IMPEDANCE
- SLEW RATE

Since most of the circuits dealing with operational amplifiers are voltage amplifiers, we will limit the tutorials in this section to voltage amplifiers only, (Vin and Vout).

The output voltage signal from an Operational Amplifier is the difference between the signals being applied to its two individual inputs. In other words, an op-amps output signal is the difference between the two input signals as the input stage of an Operational Amplifier is in fact a differential amplifier as shown below.

p-amp Parameter and Idealised Characteristic

Open Loop Gain, (Avo) Infinite – The main function of an operational amplifier is to amplify the input signal and the more open loop gain it has the better. ...

- Input impedance, (ZIN) ...
- Output impedance, (ZOUT) ...
- Bandwidth, (BW) ...
- Offset Voltage, (VIO)

An Operational Amplifier is basically a three-terminal device which consists of two high impedance inputs. One of the inputs is called the Inverting Input, marked with a negative or "minus" sign, ( – ). The other input is called the Non-inverting Input, marked with a positive or "plus" sign ( + ).

A third terminal represents the operational amplifiers output port which can both sink and source either a voltage or a current. In a linear operational amplifier, the output signal is the amplification factor, known as the amplifiers gain ( A ) multiplied by the value of the input signal and depending on the nature of these input and output signals, there can be four different classifications of operational amplifier gain.

**Video Content / Details of website for further learning (if any):**

https://nptel.ac.in/courses/108108111/

**Important Books/Journals for further learning including the page nos.:**

- D.Roy Choudhary, Sheil B.Jani, "Linear Integrated Circuits", II edition, New Age, pp. 17-19, 2015

**Course Faculty**

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**LECTURE HANDOUTS**

**L5**

**EEE**

**II/III**

**Course Name with Code** :**19EEC03 / Linear Integrated Circuits**

**Course Faculty** : **Mr.R.Suresh**

**Unit** : **I- Characteristics of Opamp** **Date of Lecture:**

**Topic of Lecture:** Inverting Amplifier Configurations

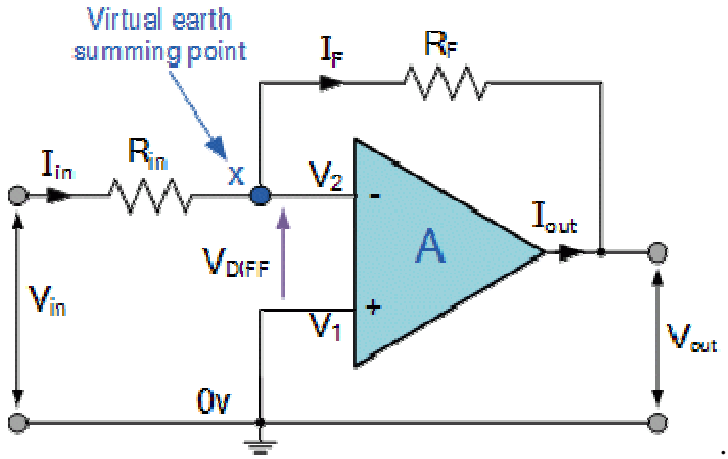
**Introduction :**

Inverting Operational Amplifier, The Inverting Operational Amplifier configuration is one of the simplest and most commonly used op-amp topologies.

**Prerequisite knowledge for Complete understanding and learning of Topic:**

Electronic Devices

**Detailed content of the Lecture:**




We saw in the last tutorial that the **Open Loop Gain**, ( $A_{VO}$ ) of an operational amplifier can be very high, as much as 1,000,000 (120dB) or more.

However, this very high gain is of no real use to us as it makes the amplifier both unstable and hard to control as the smallest of input signals, just a few micro-volts, (μV) would be enough to cause the output voltage to saturate and swing towards one or the other of the voltage supply rails losing complete control of the output.

As the open loop DC gain of an operational amplifier is extremely high we can therefore afford to lose some of this high gain by connecting a suitable resistor across the amplifier from the output terminal back to the inverting input terminal to both reduce and control the overall gain of the amplifier. This then produces and effect known commonly as Negative Feedback, and thus produces a

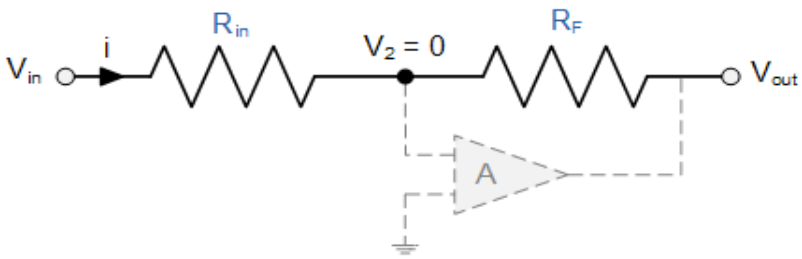
very stable Operational Amplifier based system.

**Negative Feedback** is the process of "feeding back" a fraction of the output signal back to the input, but to make the feedback negative, we must feed it back to the negative or "inverting input" terminal of the op-amp using an external **Feedback Resistor** called R$f$. This feedback connection between the output and the inverting input terminal forces the differential input voltage towards zero.

This effect produces a closed loop circuit to the amplifier resulting in the gain of the amplifier now being called its **Closed-loop Gain**. Then a closed-loop inverting amplifier uses negative feedback to accurately control the overall gain of the amplifier, but at a cost in the reduction of the amplifiers gain.

This negative feedback results in the inverting input terminal having a different signal on it than the actual input voltage as it will be the sum of the input voltage plus the negative feedback voltage giving it the label or term of a Summing Point. We must therefore separate the real input signal from the inverting input by using an **Input Resistor**, Rin.

As we are not using the positive non-inverting input this is connected to a common ground or zero voltage terminal as shown below, but the effect of this closed loop feedback circuit results in the voltage potential at the inverting input being equal to that at the non-inverting input producing a Virtual Earth summing point because it will be at the same potential as the grounded reference input. In other words, the op-amp becomes a "differential amplifier".




$$i = \frac{Vin - Vout}{Rin + Rf}$$

$$\text{therefore, } i = \frac{Vin - V2}{Rin} = \frac{V2 - Vout}{Rf}$$

$$i = \frac{Vin}{Rin} - \frac{V2}{Rin} = \frac{V2}{Rf} - \frac{Vout}{Rf}$$

$$\text{so, } \frac{Vin}{Rin} = V2\left[\frac{1}{Rin} + \frac{1}{Rf}\right] - \frac{Vout}{Rf}$$

and as, $i = \frac{Vin - 0}{Rin} = \frac{0 - Vout}{Rf}$ $\frac{Rf}{Rin} = \frac{0 - Vout}{Vin - 0}$

the Closed Loop Gain (Av) is given as, $\frac{Vout}{Vin} = -\frac{Rf}{Rin}$

Then, the **Closed-Loop Voltage Gain** of an Inverting Amplifier is given as.

$$Gain\,(Av) = \frac{V_{out}}{V_{in}} = -\frac{R_f}{R_{in}}$$

**Video Content / Details of website for further learning (if any):**

https://nptel.ac.in/courses/108108111/

**Important Books/Journals for further learning including the page nos.:**

- D.Roy Choudhary, Sheil B.Jani, "Linear Integrated Circuits", II edition, New Age, pp. 52-55, 2015

**Course Faculty**

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**LECTURE HANDOUTS**

**L6**

**EEE**

**II/III**

**Course Name with Code** :19EEC03 / Linear Integrated Circuits

**Course Faculty** : Mr.R.Suresh

**Unit** :I- Characteristics of Opamp **Date of Lecture:**

**Topic of Lecture:** Non-Inverting Amplifier Configurations

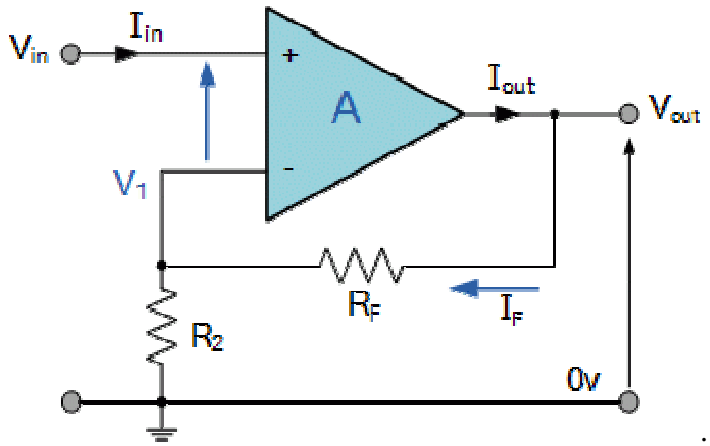
**Introduction :**

Non-inverting Operational Amplifier, The second basic configuration of an operational amplifier circuit is that of a Non-inverting Operational Amplifier design.

**Prerequisite knowledge for Complete understanding and learning of Topic:**

Electronic Devices

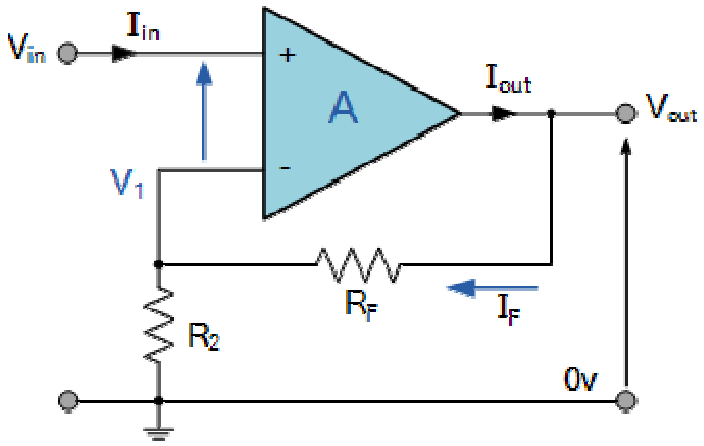
**Detailed content of the Lecture:**




In this configuration, the input voltage signal, ( $V_{IN}$ ) is applied directly to the non-inverting ( + ) input terminal which means that the output gain of the amplifier becomes "Positive" in value in contrast to the "Inverting Amplifier" circuit we saw in the last tutorial whose output gain is negative in value. The result of this is that the output signal is "in-phase" with the input signal.

Feedback control of the non-inverting operational amplifier is achieved by applying a small part of the output voltage signal back to the inverting ( – ) input terminal via a R$f$ – R2 voltage divider network, again producing negative feedback. This closed-loop configuration produces a non-inverting amplifier circuit with very good stability, a very high input impedance, Rin approaching infinity, as no current flows into the positive input terminal, (ideal conditions) and a low output impedance, Rout as shown below.

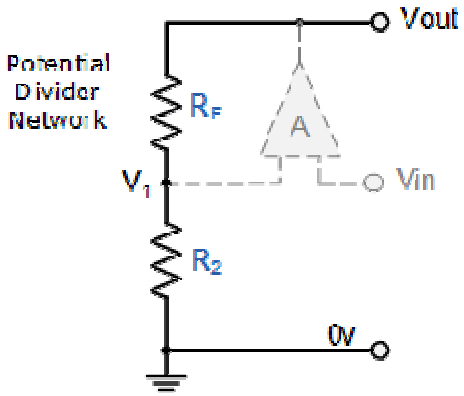
## Non-inverting Operational Amplifier Configuration




In the previous Inverting Amplifier tutorial, we said that for an ideal op-amp "No current flows into the input terminal" of the amplifier and that "V1 always equals V2". This was because the junction of the input and feedback signal ( V1 ) are at the same potential.

In other words the junction is a "virtual earth" summing point. Because of this virtual earth node the resistors, R*f* and R2 form a simple potential divider network across the non-inverting amplifier with the voltage gain of the circuit being determined by the ratios of R2 and R*f* as shown below.

## Equivalent Potential Divider Network




Then using the formula to calculate the output voltage of a potential divider network, we can calculate the closed-loop voltage gain ( $A_V$ ) of the **Non-inverting Amplifier** as follows:

$$V_1 = \frac{R_2}{R_2 + R_F} \times V_{OUT}$$

Ideal Summing Point: $V_1 = V_{IN}$

Voltage Gain, $A_{(V)}$ is equal to: $\frac{V_{OUT}}{V_{IN}}$

Then, $A_{(V)} = \frac{V_{OUT}}{V_{IN}} = \frac{R_2 + R_F}{R_2}$

Transpose to give: $A_{(V)} = \frac{V_{OUT}}{V_{IN}} = 1 + \frac{R_F}{R_2}$

Then the closed loop voltage gain of a **Non-inverting Operational Amplifier** will be given as:

$$A_{(v)} = 1 + \frac{R_F}{R_2}$$

We can see from the equation above, that the overall closed-loop gain of a non-inverting amplifier will always be greater but never less than one (unity), it is positive in nature and is determined by the ratio of the values of R$f$ and R2.

If the value of the feedback resistor R$f$ is zero, the gain of the amplifier will be exactly equal to one (unity). If resistor R2 is zero the gain will approach infinity, but in practice it will be limited to the operational amplifiers open-loop differential gain, ( $A_O$ ).

We can easily convert an inverting operational amplifier configuration into a non-inverting amplifier configuration by simply changing the input connections as shown.

**Video Content / Details of website for further learning (if any):**

https://nptel.ac.in/courses/108108111/

**Important Books/Journals for further learning including the page nos.:**

- D.Roy Choudhary, Sheil B.Jani, "Linear Integrated Circuits", II edition, New Age, pp. 25-29, 2015

**Course Faculty**

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**L7**

## LECTURE HANDOUTS

**EEE**

**II/III**

**Course Name with Code** :19EEC03 / Linear Integrated Circuits

**Course Faculty** : Mr.R.Suresh

**Unit** :I- Characteristics of Opamp **Date of Lecture:**

**Topic of Lecture:** Frequency Response

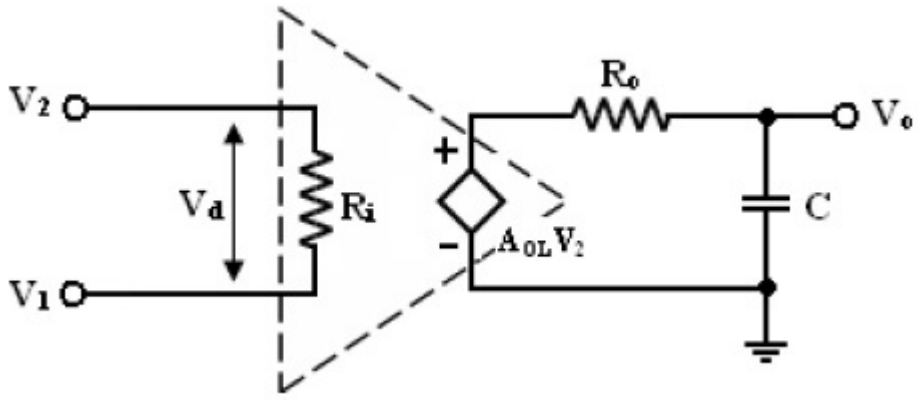
**Introduction :Frequency response** is the quantitative measure of the output spectrum of a system or device in **response** to a stimulus, and is used to characterize the dynamics of the system. It is a measure of magnitude and phase of the output as a function of **frequency**, in comparison to the input.

**Prerequisite knowledge for Complete understanding and learning of Topic:**

Electronic Devices

**Detailed content of the Lecture:**

- The variation in operating frequency will cause variations in gain magnitude and its phase angle. The manner in which the gain of the op-amp responds to different frequencies is called the frequency response.
- Op-amp should have an infinite bandwidth Bw =∞ (i.e) if its open loop gain in 90dB with dc signal its gain should remain the same 90 dB through audio and onto high radio frequency.
- The op-amp gain decreases (roll-off) at higher frequency what reasons to decrease gain after a certain frequency reached. There must be a capacitive component in the equivalent circuit of the op-amp. For an op-amp with only one break (corner) frequency all the capacitors effects can be represented by a single capacitor C. Below fig is a modified variation of the low frequency model with capacitor C at the o/p.

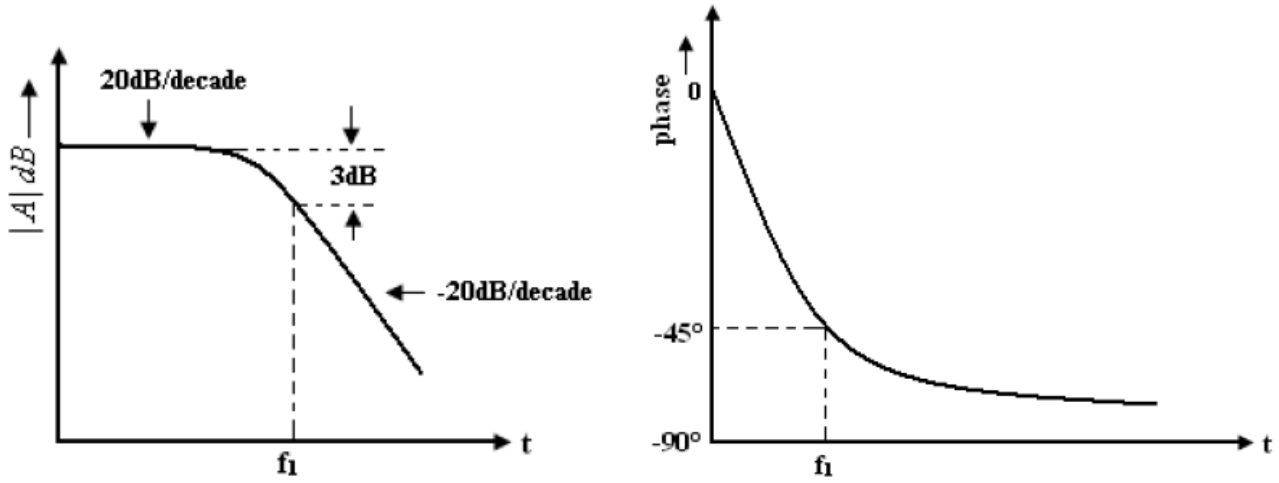



There is one pole due to R0 C and one -20dB/decade.

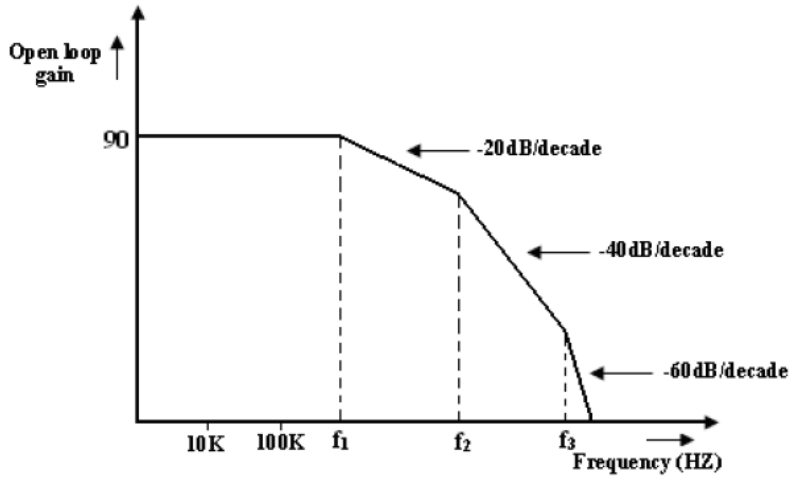
The open loop voltage gain of an op-amp with only one corner frequency is obtained from above fig. f1 is the corner frequency or the upper 3 dB frequency of the op-amp.

The magnitude and phase angle of the open loop volt gain are fu of frequency can be written as,

1. For frequency f<< f1 the magnitude of the gain is 20 log AOL in dB. ]
2. At frequency f = f1 the gain in 3 dB down from the dc value of AOL in dB. This frequency f1 is called corner frequency.
3. For f>> f1 the fain roll-off at the rate off -20dB/decade or -6dB/decade.




From the phase characteristics that the phase angle is zero at frequency f =0. At the corner frequency f1 the phase angle is -450 (lagging and a infinite frequency the phase angle is -900 .
It shows that a maximum of 900 phase change can occur in an op-amp with a single capacitor C. Zero frequency is taken as te decade below the corner frequency and infinite frequency is one decade above the corner frequency




**Video Content / Details of website for further learning (if any):**

https://nptel.ac.in/courses/108108111/

**Important Books/Journals for further learning including the page nos.:**

- D.RoyChoudhary, SheilB.Jani, "Linear Integrated Circuits", II edition, New Age, pp. 29-33, 2015

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**L8**

## LECTURE HANDOUTS

**EEE**

**II/III**

**Course Name with Code** :19EEC03 / Linear Integrated Circuits

**Course Faculty** : Mr.R.Suresh

**Unit** :I- Characteristics of Opamp **Date of Lecture:**

**Topic of Lecture:** Circuit Stability

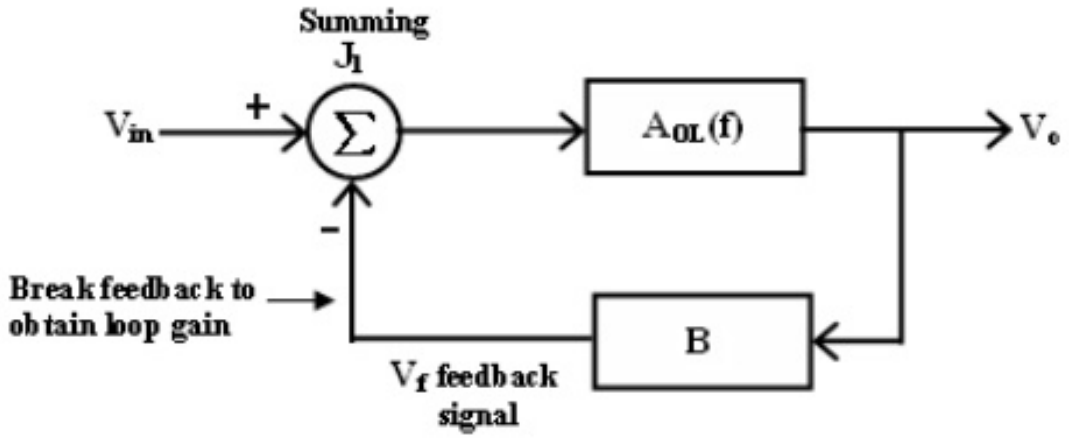
**Introduction :**A **circuit** or a group of **circuit** connected together as a system is said to be **stable**, if its o/p reaches a fixed value in a finite time. (or) A system is said to be unstable, if its o/p increases with time instead of achieving a fixed value

**Prerequisite knowledge for Complete understanding and learning of Topic:**

Electronic Devices

**Detailed content of the Lecture:**

- The Circuit Stability:
- A circuit or a group of circuit connected together as a system is said to be stable, if its o/p reaches a fixed value in a finite time. (or) A system is said to be unstable, if its o/p increases with time instead of achieving a fixed value. In fact the o/p of an unstable sys keeps on increasing until the system break down. The unstable system are impractical and need be made stable. The criteriangn for stability is used when the system is to be tested practically. In theoretically, always used to test system for stability , ex: Bode plots.
- Bode plots are compared of magnitude Vs Frequency and phase angle Vs frequency. Any system whose stability is to be determined can represented by the block diagram.




The block between the output and input is referred to as forward block and the block between the output signal and f/b signal is referred to as feedback block. The content of each block is referred Transfer frequency‘ From fig we represented it by AOL (f) which is given by

$A_{OL}$ (f) = $V_0$ /$V_{in}$ if $V_f$ = 0. -----(1)

where $A_{OL}$ (f) = open loop volt gain. The closed loop gain $A_f$ is given by

$A_F = V_0 / V_{in}$

$A_F = A_{OL} / (1+(A_{OL}) (B)$ ----(2)

B = gain of feedback circuit.

B is a constant if the feedback circuit uses only resistive components. Once the magnitude Vs frequency and phase angle Vs frequency plots are drawn, system stability may be determined as follows

Method:1:

Determine the phase angle when the magnitude of ($A_{OL}$) (B) is 0dB (or) 1. If phase angle is > .-$180^0$ , the system is stable. However, the some systems the magnitude may never be 0, in that cases method 2, must be used.

Method 2:

Determine the phase angle when the magnitude of ($A_{OL}$) (B) is 0dB (or) 1. If phase angle is > .-$180^0$ , If the magnitude is –ve decibels then the system is stable. However, the some systems the phase angle of a system may reach **-$180^0$ , under such conditions method 1 must be used to determine the system stability.**

**Video Content / Details of website for further learning (if any):**

https://nptel.ac.in/courses/108108111/

**Important Books/Journals for further learning including the page nos.:**

- D.RoyChoudhary, SheilB.Jani, “Linear Integrated Circuits”, II edition, New Age, pp47-53, 2015

**Course Faculty**

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## LECTURE HANDOUTS

**EEE**

**II/III**

**Course Name with Code** :**19EEC03 / Linear Integrated Circuits**

**Course Faculty** : **Mr.R.Suresh**

**Unit** :**I- Characteristics of Opamp** **Date of Lecture:**

**Topic of Lecture:** Circuit Stability

**Introduction :**A **circuit** or a group of **circuit** connected together as a system is said to be **stable**, if its o/p reaches a fixed value in a finite time. (or) A system is said to be unstable, if its o/p increases with time instead of achieving a fixed value

**Prerequisite knowledge for Complete understanding and learning of Topic:**

Electronic Devices

**Detailed content of the Lecture:**

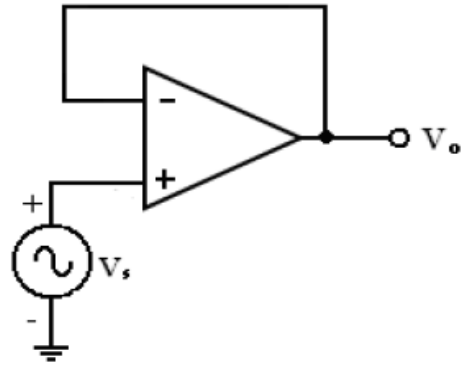
Slew Rate

Another important frequency related parameter of an op-amp is the slew rate. (Slew rate is the maximum rate of change of output voltage with respect to time. Specified in V/μs).

Reason for Slew rate: There is usually a capacitor within 0, outside an op-amp oscillation. It is this capacitor which prevents the o/p voltage from fast changing input. The rate at which the volt across the capacitor increases is given by

$dVc/dt = I/C$ --------(1)

- I -> Maximum amount furnished by the op-amp to capacitor C.
- Op-amp should have the either a higher current or small compensating capacitors. For 741 IC, the maximum internal capacitor charging current is limited to about 15μA. So the slew rate of 741 IC is $SR = dVc/dt |max = Imax/C$ .
- For a sine wave input, the effect of slew rate can be calculated as consider volt follower -> The input is large amp, high frequency sine wave .
- If $Vs = VmSinwt$ then output $V0 = Vmsinwt$ . The rate of change of output is given by $dV0/dt = Vm\ w\ coswt$.

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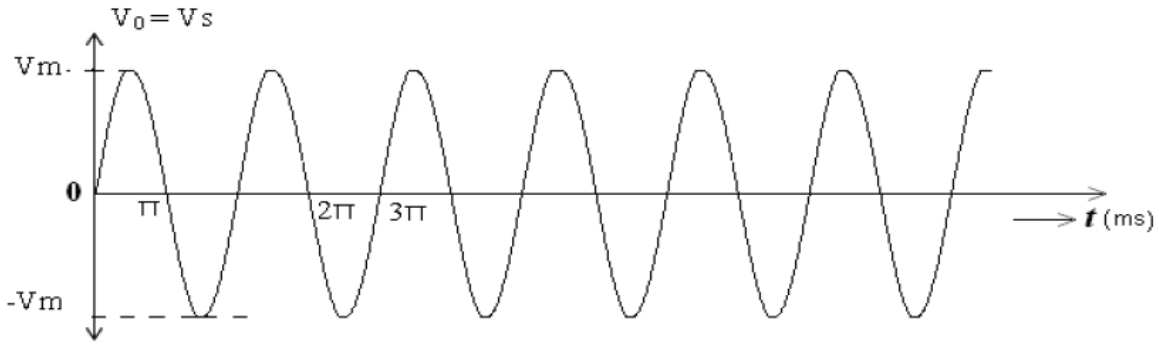


**Input and Output Waveforms**

The max rate of change of output across when coswt =1

(i.e) SR = dV0/dt |max = wVm. SR = 2ΠfVm V/s = 2ΠfVm v/ms.

- ➢ Thus the maximum frequency fmax at which we can obtain an undistorted output volt of peak value Vm is given by fmax (Hz) = Slew rate/6.28 * Vm . called the full power response.

It is maximum frequency of a large amplitude sine wave with which op-amp can have without distortion.

**Video Content / Details of website for further learning (if any):**

https://nptel.ac.in/courses/108108111/

**Important Books/Journals for further learning including the page nos.:**

- D.RoyChoudhary, SheilB.Jani, "Linear Integrated Circuits", II edition, New Age, pp. 47-53, 2015

**Course Faculty**

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**L10**

## LECTURE HANDOUTS

**EEE**

**II/III**

**Course Name with Code** :**19EEC03 / Linear Integrated Circuits**

**Course Faculty** : **Mr.R.Suresh**

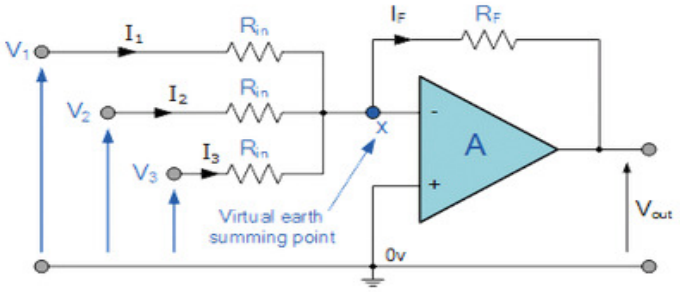
**Unit** :**II- Applications of Operational Amplifier** **Date of Lecture:**

**Topic of Lecture:** DC and AC Amplifiers

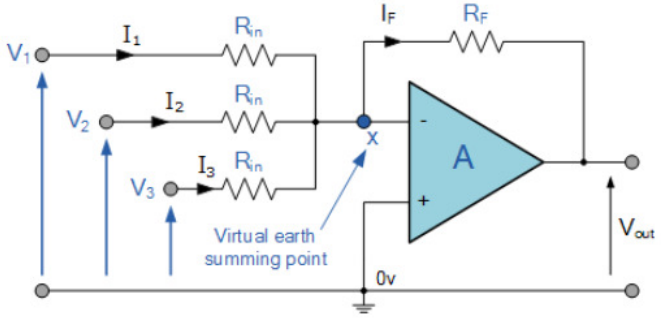
**Introduction** :The Summing Amplifier is another type of operational amplifier circuit configuration that is used to combine the voltages present on two or more inputs into a single output voltage.

**Prerequisite knowledge for Complete understanding and learning of Topic:**
Electronic Devices

**Detailed content of the Lecture:**




We saw previously in the inverting operational amplifier that the inverting amplifier has a single input voltage, (Vin) applied to the inverting input terminal. If we add more input resistors to the input, each equal in value to the original input resistor, (Rin) we end up with another operational amplifier circuit called a Summing Amplifier, "summing inverter" or even a "voltage adder".




In this simple summing amplifier circuit, the output voltage, ( Vout ) now becomes proportional to the sum of the input voltages, $V_1$, $V_2$, $V_3$, etc. Then we can modify the original equation for the inverting amplifier to take account of these new inputs thus:

$$I_F = I_1 + I_2 + I_3 = -\left[\frac{V1}{Rin} + \frac{V2}{Rin} + \frac{V3}{Rin}\right]$$

$$\text{Inverting Equation: } Vout = -\frac{Rf}{Rin} \times Vin$$

$$\text{then, } -Vout = \left[\frac{R_F}{Rin}V1 + \frac{R_F}{Rin}V2 + \frac{R_F}{Rin}V3\right]$$

However, if all the input impedances, ( $R_{IN}$ ) are equal in value, we can simplify the above equation to give an output voltage of:

**Summing Amplifier Equation**

$$-Vout = \frac{R_F}{R_{IN}}\left(V1 + V2 + V3 \ldots . etc\right)$$

**Video Content / Details of website for further learning (if any):**

https://nptel.ac.in/courses/108108111/

**Important Books/Journals for further learning including the page nos.:**


- D.RoyChoudhary, SheilB.Jani, "Linear Integrated Circuits", II edition, New Age, pp 37-39, 2015


**Course Faculty**

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## LECTURE HANDOUTS

**EEE**

**II/III**

**Course Name with Code** :19EEC03 / Linear Integrated Circuits

**Course Faculty** : Mr.R.Suresh

**Unit** :II- Applications of Operational Amplifier **Date of Lecture:**

**Topic of Lecture:** Summing Amplifier

**Introduction :** The Summing Amplifier is another type of operational amplifier circuit configuration that is used to combine the voltages present on two or more inputs into a single output voltage.

**Prerequisite knowledge for Complete understanding and learning of Topic:**

Electronic Devices

**Detailed content of the Lecture:**

We saw previously in the inverting operational amplifier that the inverting amplifier has a single input voltage, (Vin) applied to the inverting input terminal. If we add more input resistors to the input, each equal in value to the original input resistor, (Rin) we end up with another operational amplifier circuit called a **Summing Amplifier**, "*summing inverter*" or even a "*voltage adder*" circuit as shown below.In this simple summing amplifier circuit, the output voltage, ( Vout ) now becomes proportional to the sum of the input voltages, $V_1$, $V_2$, $V_3$, etc. Then we can modify the original equation for the inverting amplifier to take account of these new inputs thus:

$$I_F = I_1 + I_2 + I_3 = -\left[\frac{V1}{Rin} + \frac{V2}{Rin} + \frac{V3}{Rin}\right]$$

$$\text{Inverting Equation: } Vout = -\frac{Rf}{Rin} \times Vin$$

$$\text{then, } -Vout = \left[\frac{R_F}{Rin}V1 + \frac{R_F}{Rin}V2 + \frac{R_F}{Rin}V3\right]$$

However, if all the input impedances, ( $R_{IN}$ ) are equal in value, we can simplify the above equation to give an output voltage of:

### Summing Amplifier

We now have an operational amplifier circuit that will amplify each individual input voltage and produce an output voltage signal that is proportional to the algebraic "SUM" of the three individual input voltages $V_1$, $V_2$ and $V_3$. We can also add more inputs if required as each individual input "sees" their respective resistance, Rin as the only input impedance.

This is because the input signals are effectively isolated from each other by the "virtual earth" node at the inverting input of the op-amp. A direct voltage addition can also be obtained when all the resistances are of equal value and R$f$ is equal to Rin.

Note that when the summing point is connected to the inverting input of the op-amp the circuit will produce the negative sum of any number of input voltages. Likewise, when the summing point is connected to the non-inverting input of the op-amp, it will produce the positive sum of the input voltages.

**A** Scaling Summing Amplifier can be made if the individual input resistors are "NOT" equal. Then the equation would have to be modified to:

scaling summing amplifier equation

To make the math's a little easier, we can rearrange the above formula to make the feedback resistor R$f$ the subject of the equation giving the output voltage as:

Summing amplifier feedback equation

This allows the output voltage to be easily calculated if more input resistors are connected to the amplifiers inverting input terminal. The input impedance of each individual channel is the value of their respective input resistors, ie, R1, R2, R3 … etc.

Sometimes we need a summing circuit to just add together two or more voltage signals without any amplification. By putting all of the resistances of the circuit above to the same value R, the op-amp will have a voltage gain of unity and an output voltage equal to the direct sum of all the input voltages as shown:

unity gain summing amplifier

The Summing Amplifier is a very flexible circuit indeed, enabling us to effectively "Add" or "Sum" (hence its name) together several individual input signals. If the inputs resistors, R1, R2, R3 etc, are all equal a "unity gain inverting adder" will be made. However, if the input resistors are of different values a "scaling summing amplifier" is produced which will output a weighted sum of the input signals.

**Video Content / Details of website for further learning (if any):**

https://nptel.ac.in/courses/108108111/

**Important Books/Journals for further learning including the page nos.:**


- D.Roy Choudhary, Sheil B.Jani, "Linear Integrated Circuits", II edition, New Age, pp 47-50, 2015


**Course Faculty**

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**LECTURE HANDOUTS**

**EEE**

**II/III**

**Course Name with Code** :**19EEC03 / Linear Integrated Circuits**

**Course Faculty** : **Mr.R.Suresh**

**Unit** :**II- Applications of Operational Amplifier** **Date of Lecture:**

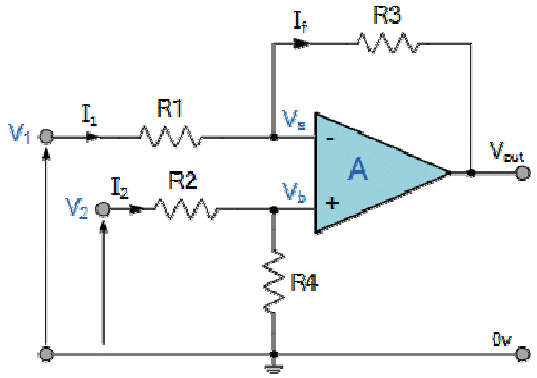
**Topic of Lecture:** Difference Amplifier

**Introduction :**A **difference amplifier** is a special purpose **amplifier** designed to measure **differential** signals, otherwise known as a subtractor. A key feature of a **difference amplifier** is its ability to remove unwanted common mode signals, known as common mode rejection (CMR).

**Prerequisite knowledge for Complete understanding and learning of Topic:**

Electronic Devices

**Detailed content of the Lecture:**



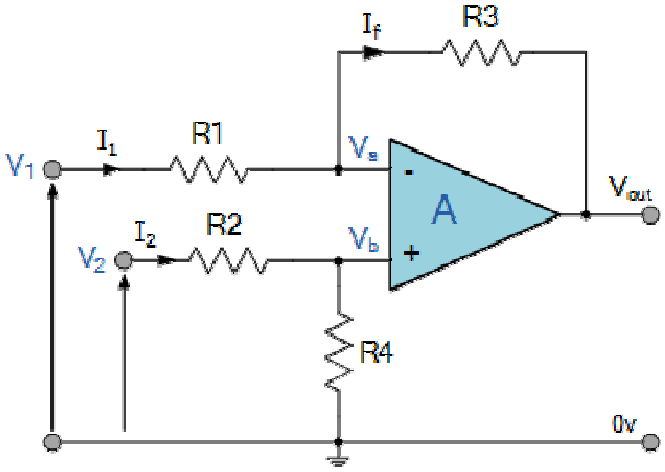

Thus far we have used only one of the operational amplifiers inputs to connect to the amplifier, using either the “inverting” or the “non-inverting” input terminal to amplify a single input signal with the other input being connected to ground.

But as a standard operational amplifier has two inputs, inverting and no-inverting, we can also connect signals to both of these inputs at the same time producing another common type of operational amplifier circuit called a **Differential Amplifier**.

Basically, as we saw in the first tutorial about operational amplifiers, all op-amps are “Differential Amplifiers” due to their input configuration. But by connecting one voltage signal onto one input terminal and another voltage signal onto the other input terminal the resultant output voltage will be proportional to the “Difference” between the two input voltage signals of $V_1$ and $V_2$.

Then *differential amplifiers* amplify the difference between two voltages making this type of operational amplifier circuit a **Subtractor** unlike a summing amplifier which adds or sums together the input voltages. This type of operational amplifier circuit is commonly known as a **Differential Amplifier** configuration and is shown below:

## Differential Amplifier




By connecting each input in turn to 0v ground we can use superposition to solve for the output voltage Vout. Then the transfer function for a **Differential Amplifier** circuit is given as:

$$I_1 = \frac{V_1 - V_a}{R_1}, \quad I_2 = \frac{V_2 - V_b}{R_2}, \quad I_3 = \frac{V_a - (V_{out})}{R_3}$$

$$\text{Summing point } V_a = V_b$$

$$\text{and } V_b = V_2\left(\frac{R_4}{R_2 + R_4}\right)$$

$$\text{If } V_2 = 0, \text{ then: } V_{out(a)} = -V_1\left(\frac{R_3}{R_1}\right)$$

$$\text{If } V_1 = 0, \text{ then: } V_{out(b)} = V_2\left(\frac{R_4}{R_2 + R_4}\right)\left(\frac{R_1 + R_3}{R_1}\right)$$

$$V_{out} = -V_{out(a)} + V_{out(b)}$$

$$\therefore V_{out} = -V_1\left(\frac{R_3}{R_1}\right) + V_2\left(\frac{R_4}{R_2 + R_4}\right)\left(\frac{R_1 + R_3}{R_1}\right)$$

When resistors, R1 = R2 and R3 = R4 the above transfer function for the differential amplifier can be simplified to the following expression:

## Differential Amplifier Equation

$$V_{OUT} = \frac{R_3}{R_1}\left(V_2 - V_1\right)$$

If all the resistors are all of the same ohmic value, that is: R1 = R2 = R3 = R4 then the circuit will become a **Unity Gain Differential Amplifier** and the voltage gain of the amplifier will be exactly one or unity. Then the output expression would simply be Vout = $V_2 - V_1$.

Also note that if input V1 is higher than input V2 the output voltage sum will be negative, and if V2 is higher than V1, the output voltage sum will be positive.

**Video Content / Details of website for further learning (if any):**

https://nptel.ac.in/courses/108108111/

**Important Books/Journals for further learning including the page nos.:**

- D.RoyChoudhary, SheilB.Jani, "Linear Integrated Circuits", II edition, New Age, pp 39-43, 2015

**Course Faculty**

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**L13**

## LECTURE HANDOUTS

**EEE**

**II/III**

**Course Name with Code** :**19EEC03 / Linear Integrated Circuits**

**Course Faculty** : **Mr.R.Suresh**

**Unit** :**II- Applications of Operational Amplifier** **Date of Lecture:**

**Topic of Lecture:** Voltage Follower

**Introduction :**A **voltage follower** (also called a unity-gain amplifier, a buffer amplifier, and an isolation amplifier) is a op-amp circuit which has a **voltage** gain of 1. This means that the op amp does not provide any amplification to the signal.

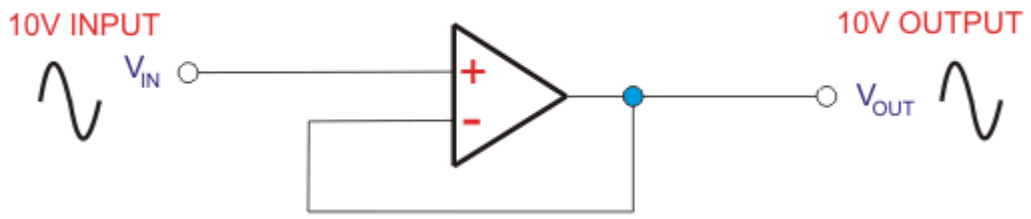
**Prerequisite knowledge for Complete understanding and learning of Topic:**

Electronic Devices

**Detailed content of the Lecture:**

**Voltage follower** is an Op-amp circuit whose output voltage straight away follows the input voltage. That is output voltage is equivalent to the input voltage. Op-amp circuit does not provide any amplification. Thus, voltage gain is equal to 1. They are similar to discrete emitter follower. The other names of voltage follower are Isolation Amplifier, Buffer Amplifier, and Unity-Gain Amplifier. The voltage follower provides no attenuation or no amplification but only buffering. This circuit has an advantageous characteristic of very high input impedance.

This high input impedance of voltage follower is the reason of it being used in several circuits. The **voltage follower** gives an efficient isolation of output from the input signal. The circuit of voltage follower is shown below.



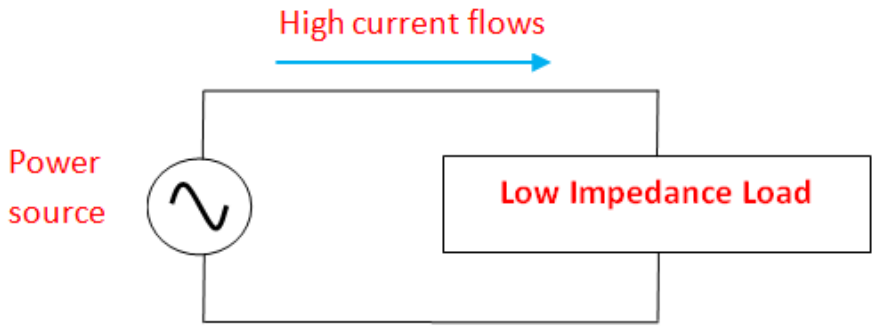

Now, let us go through the most fundamental law; that is Ohm's law.

$$Current = \frac{Voltage}{Resistance}$$

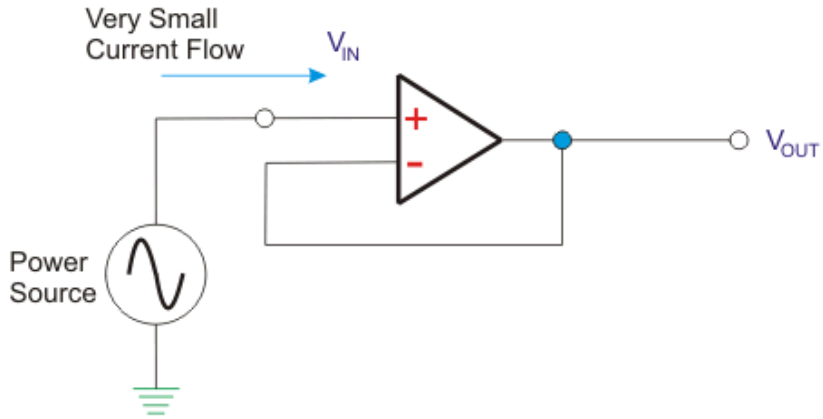
So, we can say that when resistance increases, the current drawn from the power source decreases. Thus, we conclude that the power is unaffected if the current is feeding a load of high impedance. For understanding this concept and the use of **voltage follower**, we can go through the following

examples.

First, we can consider a circuit of low impedance load and a power source is feeding it shown below. Here, a large amount of current is drawn by the load due to the low resistance load as explained by Ohm's law. Thus, the circuit takes a large amount of power from the power source, resulting in high disturbances in the source.




Next, we can consider that we are giving the same power to the **voltage follower**. Because of its very high input impedance, a minimal amount of current is taken by this circuit. The output of the circuit will be same as that of the input due to the lack of feedback resistors.




**Video Content / Details of website for further learning (if any):**

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**Important Books/Journals for further learning including the page nos.:**

- D.RoyChoudhary, SheilB.Jani, "Linear Integrated Circuits", II edition, New Age, pp 37-39, 2015

**Course Faculty**

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**L14**

## LECTURE HANDOUTS

**EEE**

**II/III**

**Course Name with Code** :**19EEC03 / Linear Integrated Circuits**

**Course Faculty** : **Mr.R.Suresh**

**Unit** : **II- Applications of Operational Amplifier** **Date of Lecture:**

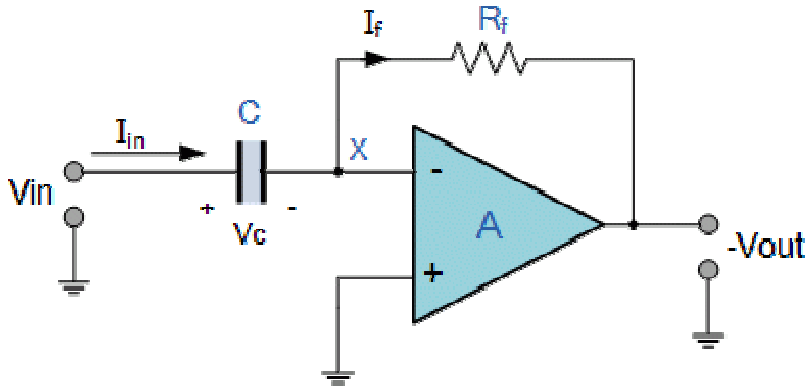
**Topic of Lecture:** Differentiator

**Introduction :**In electronics, a **differentiator** is a circuit that is designed such that the output of the circuit is approximately directly proportional to the rate of change (the time derivative) of the input. A true **differentiator** cannot be physically realized, because it has infinite gain at infinite frequency.

**Prerequisite knowledge for Complete understanding and learning of Topic:**

Electronic Devices

**Detailed content of the Lecture:**

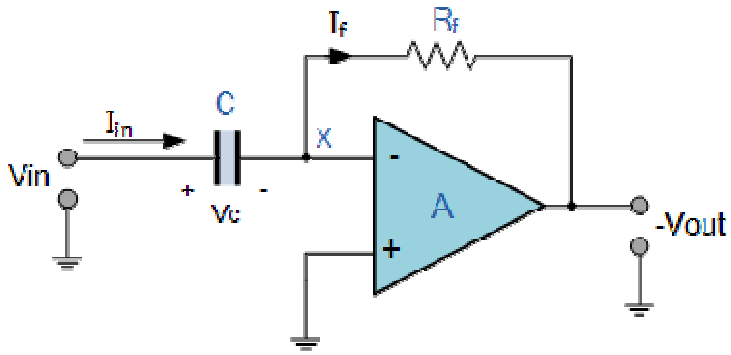



Here, the position of the capacitor and resistor have been reversed and now the reactance, $X_C$ is connected to the input terminal of the inverting amplifier while the resistor, R*f* forms the negative feedback element across the operational amplifier as normal.

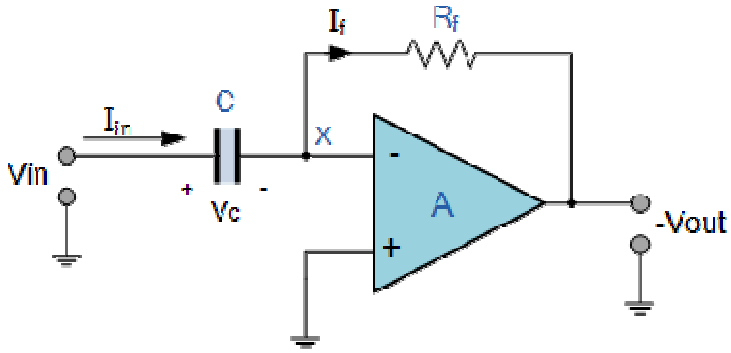
This operational amplifier circuit performs the mathematical operation of **Differentiation**, that is it "*produces a voltage output which is directly proportional to the input voltage's rate-of-change with respect to time*". In other words the faster or larger the change to the input voltage signal, the greater the input current, the greater will be the output voltage change in response, becoming more of a "spike" in shape.

As with the integrator circuit, we have a resistor and capacitor forming an RC Network across the operational amplifier and the reactance ( Xc ) of the capacitor plays a major role in the performance of a **Op-amp Differentiator**.

**Op-amp Differentiator Circuit**




**Op-amp Differentiator Circuit**




The input signal to the differentiator is applied to the capacitor. The capacitor blocks any DC content so there is no current flow to the amplifier summing point, X resulting in zero output voltage. The capacitor only allows AC type input voltage changes to pass through and whose frequency is dependant on the rate of change of the input signal.

At low frequencies the reactance of the capacitor is "High" resulting in a low gain ( R*f*/Xc ) and low output voltage from the op-amp. At higher frequencies the reactance of the capacitor is much lower resulting in a higher gain and higher output voltage from the differentiator amplifier.

However, at high frequencies an op-amp differentiator circuit becomes unstable and will start to oscillate. This is due mainly to the first-order effect, which determines the frequency response of the op-amp circuit causing a second-order response which, at high frequencies gives an output voltage far higher than what would be expected. To avoid this the high frequency gain of the circuit needs to be reduced by adding an additional small value capacitor across the feedback resistor R*f*.

Ok, some math's to explain what's going on!. Since the node voltage of the operational amplifier at its inverting input terminal is zero, the current, i flowing through the capacitor will be given as:

$$I_{IN} = I_F \quad \text{and} \quad I_F = -\frac{V_{OUT}}{R_F}$$

The charge on the capacitor equals Capacitance times Voltage across the capacitor

$$Q = C \times V_{IN}$$

Thus the rate of change of this charge is:

$$\frac{dQ}{dt} = C\frac{dV_{IN}}{dt}$$

but dQ/dt is the capacitor current, *i*

$$I_{IN} = C\frac{dV_{IN}}{dt} = I_F$$

$$\therefore -\frac{V_{OUT}}{R_F} = C\frac{dV_{IN}}{dt}$$

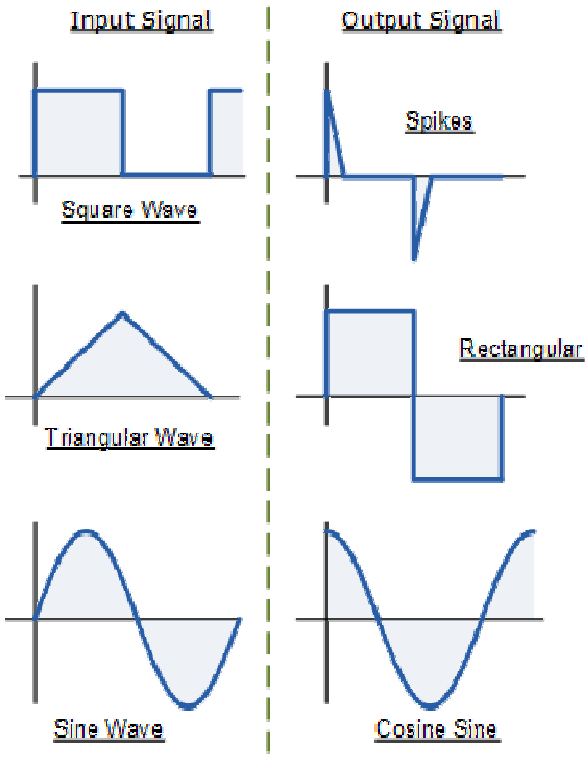
from which we have an ideal voltage output for the op-amp differentiator is given as:

$$V_{OUT} = -R_F C\frac{dV_{IN}}{dt}$$

Therefore, the output voltage Vout is a constant –R*f**C times the derivative of the input voltage Vin with respect to time. The minus sign (–) indicates a180$^o$ phase shift because the input signal is connected to the inverting input terminal of the operational amplifier.

One final point to mention, the **Op-amp Differentiator** circuit in its basic form has two main disadvantages compared to the previous operational amplifier integrator circuit. One is that it suffers from instability at high frequencies as mentioned above, and the other is that the capacitive input makes it very susceptible to random noise signals and any noise or harmonics present in the source circuit will be amplified more than the input signal itself. This is because the output is proportional to the slope of the input voltage so some means of limiting the bandwidth in order to achieve closed-loop stability is required.

**Op-amp Differentiator Waveforms**



If we apply a constantly changing signal such as a Square-wave, Triangular or Sine-wave type signal to the input of a differentiator amplifier circuit the resultant output signal will be changed and whose final shape is dependant upon the RC time constant of the Resistor/Capacitor combination.

**Video Content / Details of website for further learning (if any):**

https://nptel.ac.in/courses/108108111/

**Important Books/Journals for further learning including the page nos.:**


- D.RoyChoudhary, SheilB.Jani, "Linear Integrated Circuits", II edition, New Age, pp66-69, 2015


**Course Faculty**

# MUTHAYAMMAL ENGINEERING COLLEGE

(An Autonomous Institution)

(Approved by AICTE, New Delhi, Accredited by NAAC & Affiliated to Anna University)

Rasipuram - 637 408, Namakkal Dist., Tamil Nadu

Estd. 2000


**L15**

## LECTURE HANDOUTS

**EEE**

**II/III**

**Course Name with Code** :**19EEC03 / Linear Integrated Circuits**

**Course Faculty** : **Mr.R.Suresh**

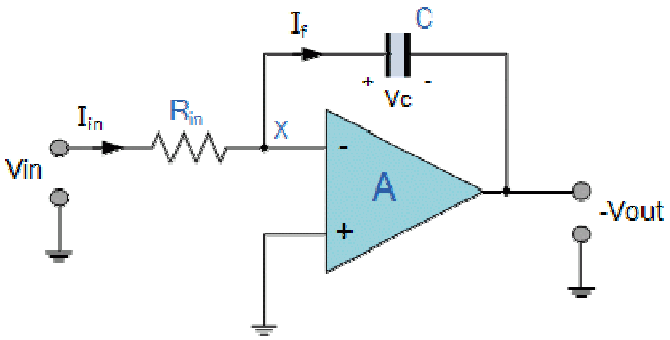
**Unit** :**II- Applications of Operational Amplifier** **Date of Lecture:**

**Topic of Lecture:** Integrator

**Introduction :**An **integrator** in measurement and control applications is an element whose output signal is the time integral of its input signal. It accumulates the input quantity over a defined time to produce a representative output. Integration is an important part of many engineering and scientific applications

**Prerequisite knowledge for Complete understanding and learning of Topic:**
Electronic Devices

**Detailed content of the Lecture:**

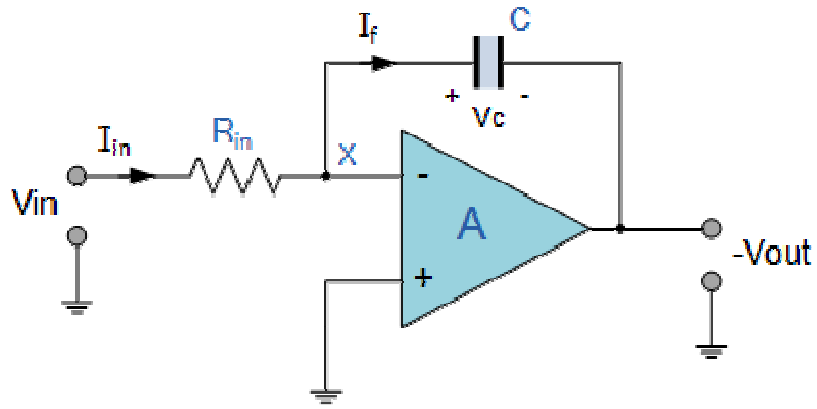



Operational amplifiers can be used as part of a positive or negative feedback amplifier or as an adder or subtractor type circuit using just pure resistances in both the input and the feedback loop.

But what if we where to change the purely resistive ( R*f* ) feedback element of an inverting amplifier with a frequency dependant complex element that has a reactance, ( X ), such as a Capacitor, C. What would be the effect on the op-amps voltage gain transfer function over its frequency range as a result of this complex impedance.

By replacing this feedback resistance with a capacitor we now have an RC Network connected across the operational amplifiers feedback path producing another type of operational amplifier circuit commonly called an **Op-amp Integrator** circuit as shown below.

## Op-amp Integrator Circuit




As its name implies, the **Op-amp Integrator** is an operational amplifier circuit that performs the mathematical operation of **Integration**, that is we can cause the output to respond to changes in the input voltage over time as the op-amp integrator produces an *output voltage which is proportional to the integral of the input voltage*.

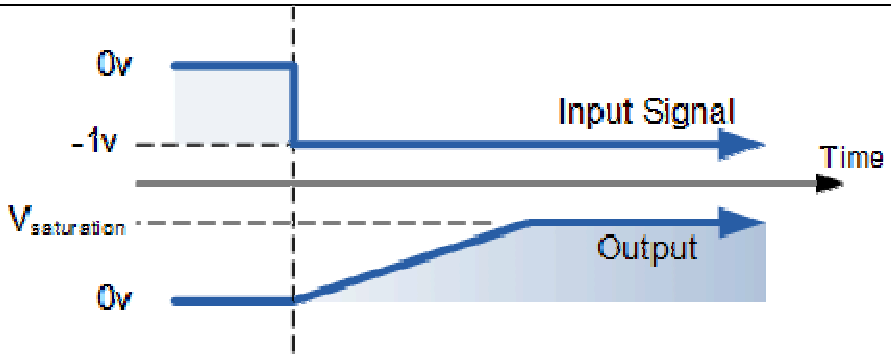
In other words the magnitude of the output signal is determined by the length of time a voltage is present at its input as the current through the feedback loop charges or discharges the capacitor as the required negative feedback occurs through the capacitor.

When a step voltage, Vin is firstly applied to the input of an integrating amplifier, the uncharged capacitor C has very little resistance and acts a bit like a short circuit allowing maximum current to flow via the input resistor, Rin as potential difference exists between the two plates. No current flows into the amplifiers input and point X is a virtual earth resulting in zero output. As the impedance of the capacitor at this point is very low, the gain ratio of $X_C/R_{IN}$ is also very small giving an overall voltage gain of less than one, ( voltage follower circuit ).

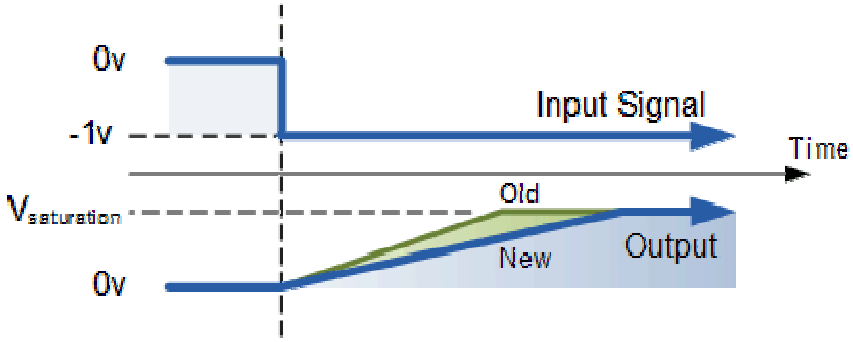
As the feedback capacitor, C begins to charge up due to the influence of the input voltage, its impedance Xc slowly increase in proportion to its rate of charge. The capacitor charges up at a rate determined by the RC time constant, ( $\tau$ ) of the series RC network. Negative feedback forces the op-amp to produce an output voltage that maintains a virtual earth at the op-amp's inverting input.

Since the capacitor is connected between the op-amp's inverting input (which is at virtual ground potential) and the op-amp's output (which is now negative), the potential voltage, Vc developed across the capacitor slowly increases causing the charging current to decrease as the impedance of the capacitor increases. This results in the ratio of Xc/Rin increasing producing a linearly increasing ramp output voltage that continues to increase until the capacitor is fully charged.

At this point the capacitor acts as an open circuit, blocking any more flow of DC current. The ratio of feedback capacitor to input resistor ( $X_C/R_{IN}$ ) is now infinite resulting in infinite gain. The result of this high gain (similar to the op-amps open-loop gain), is that the output of the amplifier goes into saturation as shown below. (Saturation occurs when the output voltage of the amplifier swings heavily to one voltage supply rail or the other with little or no control in between).

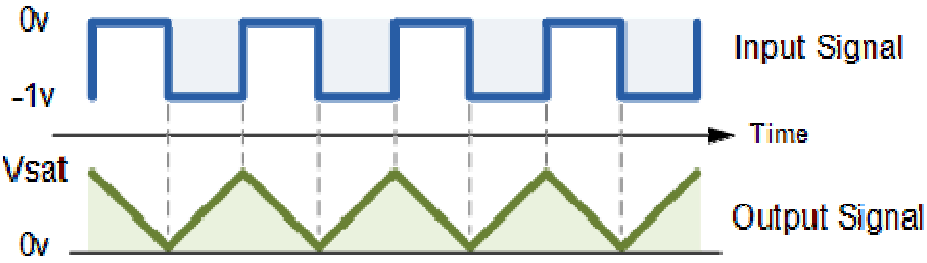



The rate at which the output voltage increases (the rate of change) is determined by the value of the resistor and the capacitor, "RC time constant". By changing this RC time constant value, either by changing the value of the Capacitor, C or the Resistor, R, the time in which it takes the output voltage to reach saturation can also be changed for example.




If we apply a constantly changing input signal such as a square wave to the input of an **Integrator Amplifier** then the capacitor will charge and discharge in response to changes in the input signal. This results in the output signal being that of a sawtooth waveform whose output is affected by the RC time constant of the resistor/capacitor combination because at higher frequencies, the capacitor has less time to fully charge. This type of circuit is also known as a **Ramp Generator** and the transfer function is given below.

### Op-amp Integrator Ramp Generator




We know from first principals that the voltage on the plates of a capacitor is equal to the charge on the capacitor divided by its capacitance giving Q/C. Then the voltage across the capacitor is output Vout therefore: -Vout = Q/C. If the capacitor is charging and discharging, the rate of charge of voltage across the capacitor is given as:

$$V_c = \frac{Q}{C}, \qquad V_c = V_x - V_{out} = 0 - V_{out}$$

$$\therefore -\frac{dV_{out}}{dt} = \frac{dQ}{Cdt} = \frac{1}{C}\frac{dQ}{dt}$$

But dQ/dt is electric current and since the node voltage of the integrating op-amp at its inverting input terminal is zero, X = 0, the input current I(in) flowing through the input resistor, Rin is given as:

$$I_{in} = \frac{V_{in} - 0}{R_{in}} = \frac{V_{in}}{R_{in}}$$

The current flowing through the feedback capacitor C is given as:

$$I_f = C\frac{dV_{out}}{dt} = C\frac{dQ}{Cdt} = \frac{dQ}{dt} = \frac{dV_{out}.C}{dt}$$

Assuming that the input impedance of the op-amp is infinite (ideal op-amp), no current flows into the op-amp terminal. Therefore, the nodal equation at the inverting input terminal is given as:

$$I_{in} = I_f = \frac{V_{in}}{R_{in}} = \frac{dV_{out}.C}{dt}$$

$$\therefore \frac{V_{in}}{V_{out}} \times \frac{dt}{R_{in}C} = 1$$

From which we derive an ideal voltage output for the **Op-amp Integrator** as:

$$V_{out} = -\frac{1}{R_{in}C}\int_0^t V_{in}\,dt = -\int_0^t V_{in}\frac{dt}{R_{in}.C}$$

To simplify the math's a little, this can also be re-written as:

$$V_{out} = -\frac{1}{j\omega RC}V_{in}$$

Where: $\omega = 2\pi f$ and the output voltage Vout is a constant 1/RC times the integral of the input voltage $V_{IN}$ with respect to time.

Thus the circuit has the transfer function of an inverting integrator with the gain constant of -1/RC. The minus sign ( – ) indicates a 180° phase shift because the input signal is connected directly to the inverting input terminal of the operational amplifier.

**Video Content / Details of website for further learning (if any):**

https://nptel.ac.in/courses/108108111/

**Important Books/Journals for further learning including the page nos.:**


- D.RoyChoudhary, SheilB.Jani, "Linear Integrated Circuits", II edition, New Age, pp 70-77, 2015


**Course Faculty**

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Estd. 2000

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**L16**

## LECTURE HANDOUTS

**EEE**

**II/III**

**Course Name with Code** :**19EEC03 / Linear Integrated Circuits**

**Course Faculty** :**Mr.R.Suresh**

**Unit** :**II- Applications of Operational Amplifier** **Date of Lecture:**

**Topic of Lecture:** Clamper

**Introduction : Clamper circuits** are the electronic circuits that **shift the dc level of the AC signal**. Clampers are also known as DC voltage restorers or level shifter. Clampers are basically classified as **positive** and **negative** that includes both biased and unbiased conditions individually.

**Prerequisite knowledge for Complete understanding and learning of Topic:**

Electronic Devices

**Detailed content of the Lecture:**

### Clamper Circuit

A Clamper circuit can be defined as the circuit that consists of a diode, a resistor and a capacitor that shifts the waveform to a desired DC level without changing the actual appearance of the applied signal.

In order to maintain the time period of the wave form, the **tau** must be greater than, half the time period discharging time of the capacitor should beslow.

$$\tau = Rc$$

Where

- R is the resistance of the resistor employed
- C is the capacitance of the capacitor used

The time constant of charge and discharge of the capacitor determines the output of a clamper circuit.

- In a clamper circuit, a vertical shift of upward or downward takes place in the output waveform with respect to the input signal.
- The load resistor and the capacitor affect the waveform. So, the discharging time of the capacitor should be large enough.

The DC component present in the input is rejected when a capacitor coupled network is used as a capacitor blocks dc

Hence when **dc** needs to be **restored**, clamping circuit is used.

## Types of Clampers

There are few types of clamper circuits, such as

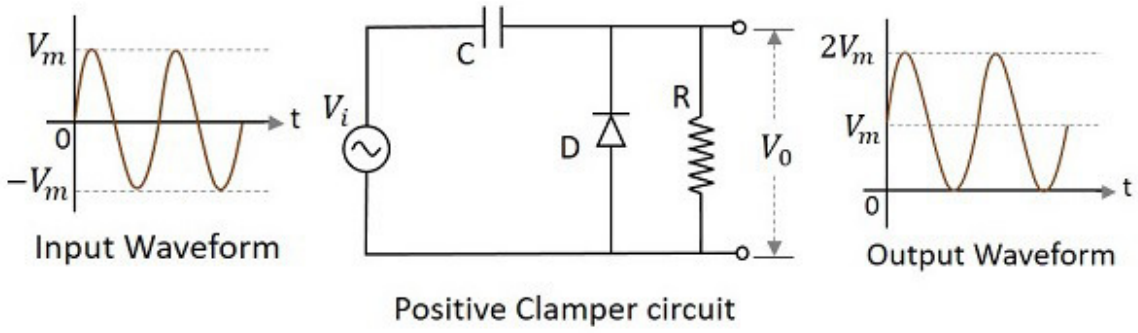
- Positive Clamper
- Positive clamper with positive $V_r$
- Positive clamper with negative $V_r$
- Negative Clamper
- Negative clamper with positive $V_r$
- Negative clamper with negative $V_r$

Let us go through them in detail.

## Positive Clamper Circuit

A Clamping circuit restores the DC level. When a negative peak of the signal is raised above to the zero level, then the signal is said to be **positively clamped**.

A Positive Clamper circuit is one that consists of a diode, a resistor and a capacitor and that shifts the output signal to the positive portion of the input signal. The figure below explains the construction of a positive clamper circuit.




Initially when the input is given, the capacitor is not yet charged and the diode is reverse biased. The output is not considered at this point of time. During the negative half cycle, at the peak value, the capacitor gets charged with negative on one plate and positive on the other. The capacitor is now charged to its peak value $V_m$

The diode is forward biased and conducts heavily.

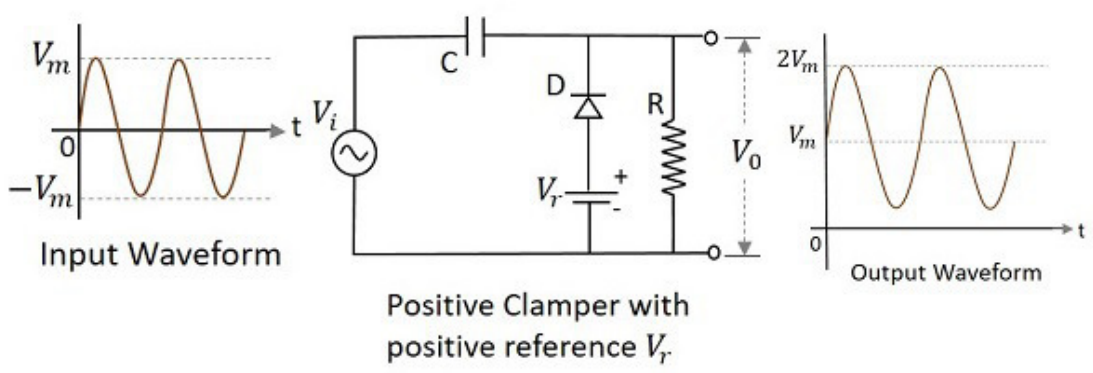
During the next positive half cycle, the capacitor is charged to positive Vm while the diode gets reverse biased and gets open circuited. The output of the circuit at this moment will be

$$V_0 = V_i + V_m$$

Hence the signal is positively clamped as shown in the above figure. The output signal changes according to the changes in the input, but shifts the level according to the charge on the capacitor, as it adds the input voltage.

## Positive Clamper with Positive $V_r$

A Positive clamper circuit if biased with some positive reference voltage, that voltage will be added to the output to raise the clamped level. Using this, the circuit of the positive clamper with positive reference voltage is constructed as below.




During the positive half cycle, the reference voltage is applied through the diode at the output and as the input voltage increases, the cathode voltage of the diode increase with respect to the anode voltage and hence it stops conducting. During the negative half cycle, the diode gets forward biased and starts conducting. The voltage across the capacitor and the reference voltage together maintain the output voltage level.

**Video Content / Details of website for further learning (if any):**

https://nptel.ac.in/courses/108108111/

**Important Books/Journals for further learning including the page nos.:**


- D.Roy Choudhary, Sheil B.Jani, "Linear Integrated Circuits", II edition, New Age, pp 80-88, 2015


**Course Faculty**

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IQAC


**LECTURE HANDOUTS**

**L17**

**EEE**

**II/III**

**Course Name with Code** :**19EEC03 / Linear Integrated Circuits**

**Course Faculty** : **Mr.R.Suresh**

**Unit** :**II- Applications of Operational Amplifier** **Date of Lecture:**

**Topic of Lecture:** Clipper

**Introduction :**Clipper **circuits** are the electronic circuits that **shift the dc level of the AC signal**. Clampers are also known as DC voltage restorers or level shifter. Clampers are basically classified as **positive** and **negative** that includes both biased and unbiased conditions individually.

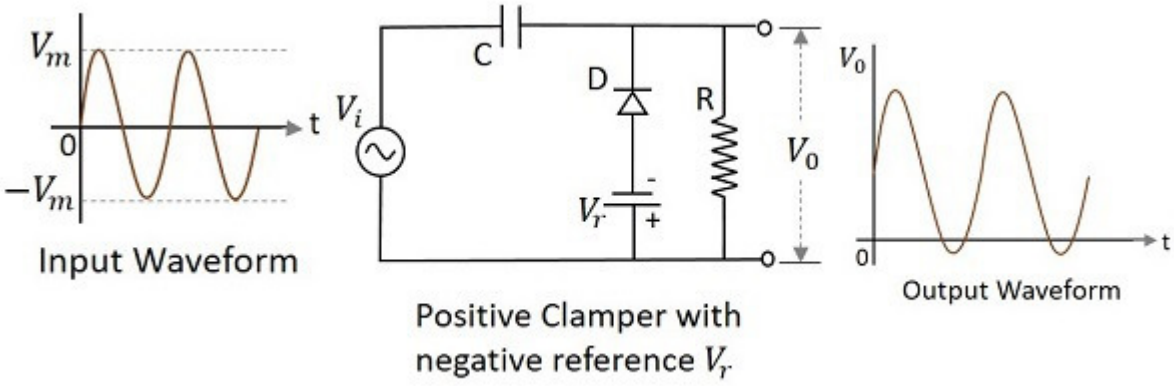
**Prerequisite knowledge for Complete understanding and learning of Topic:**

Electronic Devices

**Detailed content of the Lecture:**

## Positive Clipper with Negative $Vr$

A Positive clamper circuit if biased with some negative reference voltage, that voltage will be added to the output to raise the clamped level. Using this, the circuit of the positive clamper with positive reference voltage is constructed as below.

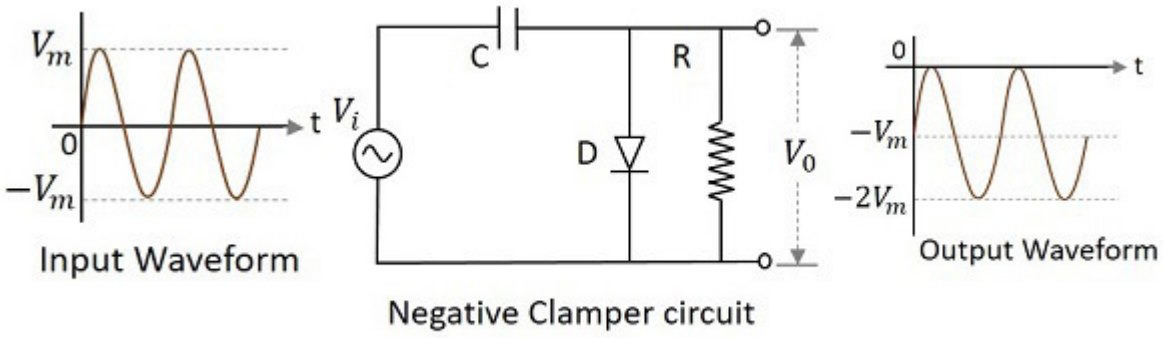



During the positive half cycle, the voltage across the capacitor and the reference voltage together maintain the output voltage level. During the negative half-cycle, the diode conducts when the cathode voltage gets less than the anode voltage. These changes make the output voltage as shown in the above figure.

## Negative Clipper

A Negative Clamper circuit is one that consists of a diode, a resistor and a capacitor and that shifts the output signal to the negative portion of the input signal. The figure below explains the construction

of a negative clamper circuit.




During the positive half cycle, the capacitor gets charged to its peak value $v_m$

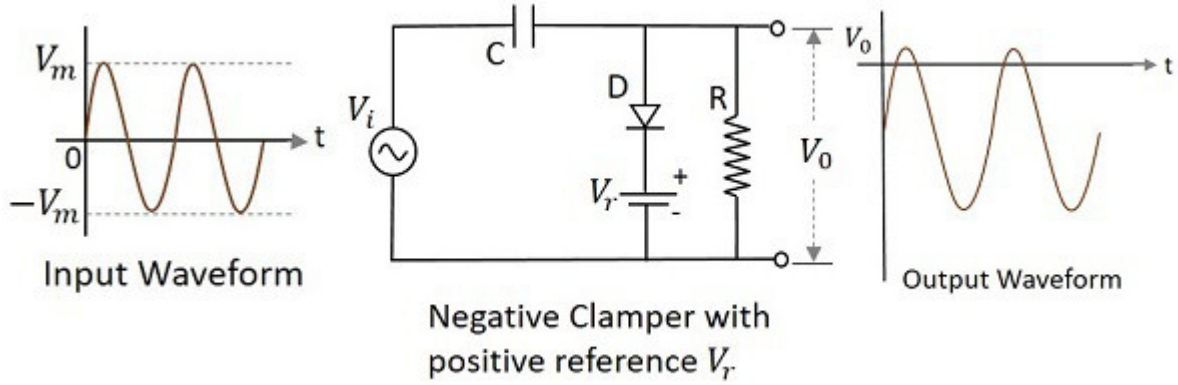
The diode is forward biased and conducts. During the negative half cycle, the diode gets reverse biased and gets open circuited. The output of the circuit at this moment will be

$$V_0=V_i+V_m$$

Hence the signal is negatively clamped as shown in the above figure. The output signal changes according to the changes in the input, but shifts the level according to the charge on the capacitor, as it adds the input voltage.

## Negative Clipper with positive $V_r$

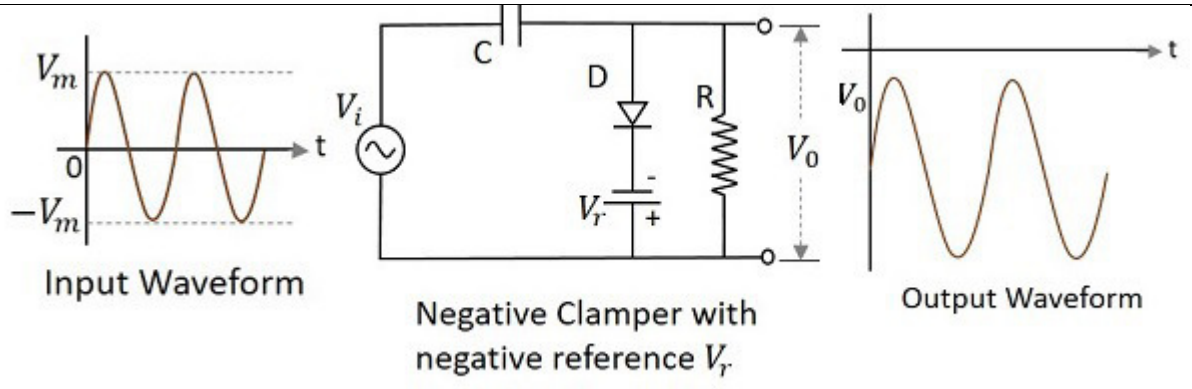
A Negative clamper circuit if biased with some positive reference voltage, that voltage will be added to the output to raise the clamped level. Using this, the circuit of the negative clamper with positive reference voltage is constructed as below.




Though the output voltage is negatively clamped, a portion of the output waveform is raised to the positive level, as the applied reference voltage is positive. During the positive half-cycle, the diode conducts, but the output equals the positive reference voltage applied. During the negative half cycle, the diode acts as open circuited and the voltage across the capacitor forms the output.

## Negative Clamper with Negative $V_r$

A Negative clamper circuit if biased with some negative reference voltage, that voltage will be added to the output to raise the clamped level. Using this, the circuit of the negative clamper with negative reference voltage is constructed as below.




The cathode of the diode is connected with a negative reference voltage, which is less than that of zero and the anode voltage. Hence the diode starts conducting during positive half cycle, before the zero voltage level. During the negative half cycle, the voltage across the capacitor appears at the output. Thus the waveform is clamped towards the negative portion.

**Video Content / Details of website for further learning (if any):**

https://nptel.ac.in/courses/108108111/

**Important Books/Journals for further learning including the page nos.:**

- D.RoyChoudhary, SheilB.Jani, "Linear Integrated Circuits", II edition, New Age, pp 80-88, 2015

**Course Faculty**

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**L18**

## LECTURE HANDOUTS

**EEE**

**II/III**

**Course Name with Code** :**19EEC03 / Linear Integrated Circuits**

**Course Faculty** : **Mr.R.Suresh**

**Unit** :**II- Applications of Operational Amplifier** **Date of Lecture:**

**Topic of Lecture: Filter**

**Introduction :** The ripple in the signal denotes the presence of some AC component. This ac component has to be completely removed in order to get pure dc output. So, we need a circuit that **smoothens** the rectified output into a pure dc signal.

A **filter circuit** is one which removes the ac component present in the rectified output and allows the dc component to reach the load

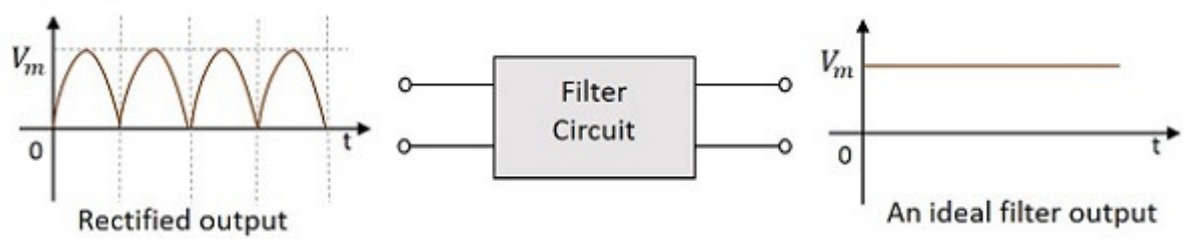
**Prerequisite knowledge for Complete understanding and learning of Topic:**

Electronic Devices

**Detailed content of the Lecture:**

A **filter circuit** is one which removes the ac component present in the rectified output and allows the dc component to reach the load.

The following figure shows the functionality of a filter circuit.




A filter circuit is constructed using two main components, inductor and capacitor. We have already studied in Basic Electronics tutorial that

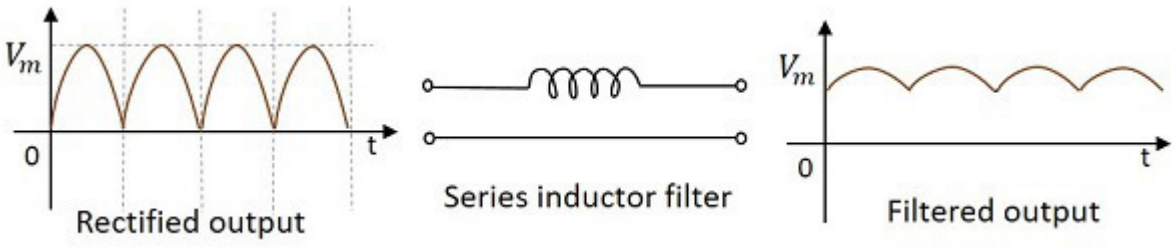
- An inductor allows **dc** and blocks **ac**.
- A capacitor allows **ac** and blocks **dc**.

Let us try to construct a few filters, using these two components.

### Series Inductor Filter

As an inductor allows dc and blocks ac, a filter called **Series Inductor Filter** can be constructed by connecting the inductor in series, between the rectifier and the load. The figure below shows the circuit

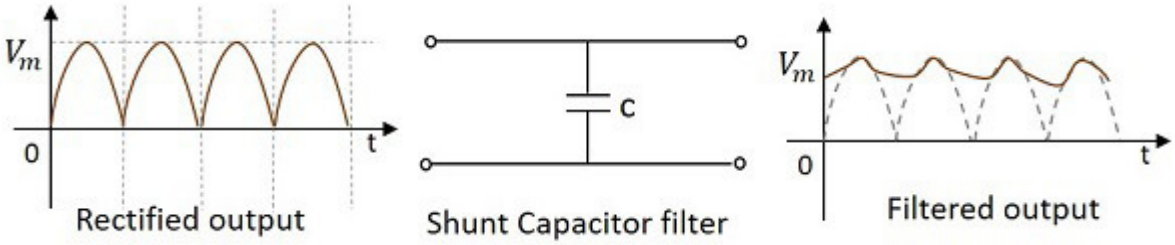
of a series inductor filter.




The rectified output when passed through this filter, the inductor blocks the ac components that are present in the signal, in order to provide a pure dc. This is a simple primary filter.

## Shunt Capacitor Filter

As a capacitor allows ac through it and blocks dc, a filter called **Shunt Capacitor Filter** can be constructed using a capacitor, connected in shunt, as shown in the following figure.

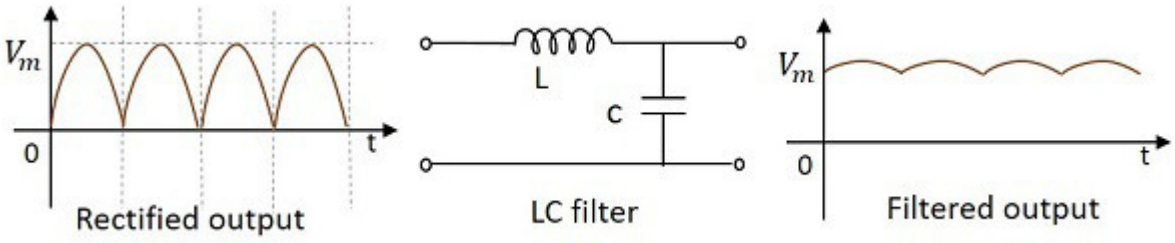



The rectified output when passed through this filter, the ac components present in the signal are grounded through the capacitor which allows ac components. The remaining dc components present in the signal are collected at the output.

The above filter types discussed are constructed using an inductor or a capacitor. Now, let's try to use both of them to make a better filter. These are combinational filters.

## L-C Filter

A filter circuit can be constructed using both inductor and capacitor in order to obtain a better output where the efficiencies of both inductor and capacitor can be used. The figure below shows the circuit diagram of a LC filter.




The rectified output when given to this circuit, the inductor allows dc components to pass through it, blocking the ac components in the signal. Now, from that signal, few more ac components if any present are grounded so that we get a pure dc output.

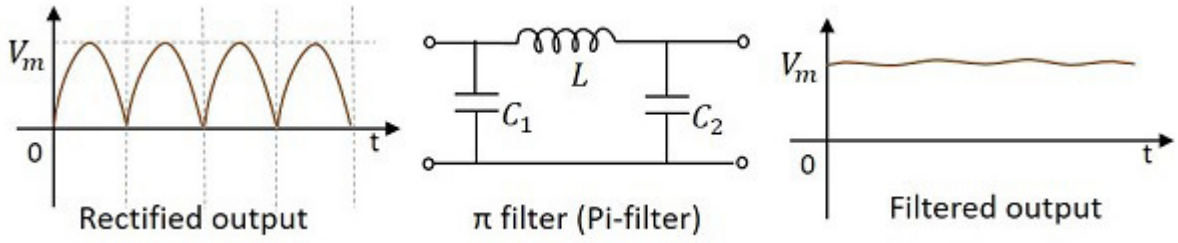
This filter is also called as a **Choke Input Filter** as the input signal first enters the inductor. The output of this filter is a better one than the previous ones.

## Π- Filter Pifilter

This is another type of filter circuit which is very commonly used. It has capacitor at its input and hence it is also called as a **Capacitor Input Filter**. Here, two capacitors and one inductor are connected in the form of π shaped network. A capacitor in parallel, then an inductor in series, followed by another capacitor in parallel makes this circuit.

If needed, several identical sections can also be added to this, according to the requirement. The figure below shows a circuit for $\pi$

filter ***Pi–filter***

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### Working of a Pi filter

In this circuit, we have a capacitor in parallel, then an inductor in series, followed by another capacitor in parallel.

- **Capacitor $C_1$ –** This filter capacitor offers high reactance to dc and low reactance to ac signal. After grounding the ac components present in the signal, the signal passes to the inductor for further filtration.
- **Inductor L –** This inductor offers low reactance to dc components, while blocking the ac components if any got managed to pass, through the capacitor $C_1$.
- **Capacitor $C_2$ –** Now the signal is further smoothened using this capacitor so that it allows any ac component present in the signal, which the inductor has failed to block.

**Video Content / Details of website for further learning (if any):**

https://nptel.ac.in/courses/108108111/

**Important Books/Journals for further learning including the page nos.:**


- D.Roy Choudhary, Sheil B.Jani, "Linear Integrated Circuits", II edition, New Age, pp89-95, 2015


**Course Faculty**

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**L19**

## LECTURE HANDOUTS

**EEE**

**II/III**

**Course Name with Code** :**19EEC03 / Linear Integrated Circuits**

**Course Faculty** : **Mr.R.Suresh**

**Unit** :**III- Waveform Generator** **Date of Lecture:**

**Topic of Lecture:** Oscillators

**Introduction :**An **oscillator** is a circuit which produces a continuous, repeated, alternating waveform without any input. **Oscillators** basically convert unidirectional current flow from a DC source into an alternating waveform which is of the desired frequency, as decided by its circuit components

**Prerequisite knowledge for Complete understanding and learning of Topic:**

Electronic Devices

**Detailed content of the Lecture:**

### What is an Oscillator?

An **oscillator** is a circuit which produces a continuous, repeated, alternating waveform without any input. Oscillators basically convert unidirectional current flow from a DC source into an alternating waveform which is of the desired frequency, as decided by its circuit components.

The basic principle behind the working of oscillators can be understood by analyzing the behavior of an LC tank circuit shown in Figure 1 below, which employs an inductor L and a completely pre-charged capacitor C as its components. Here, at first, the capacitor starts to discharge via the inductor, which results in the conversion of its electrical energy into the electromagnetic field, which can be stored in the inductor. Once the capacitor discharges completely, there will be no current flow in the circuit.

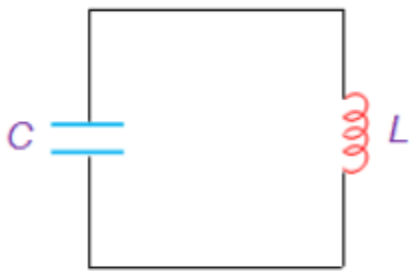


Figure 1 LC Tank Circuit

However, by then, the stored electromagnetic field would have generated a back-emf which results in the flow of current through the circuit in the same direction as that of before. This current flow through the circuit continues until the electromagnetic field collapses which result in the back-

conversion of electromagnetic energy into electrical form, causing the cycle to repeat. However, now the capacitor would have charged with the opposite polarity, due to which one gets an oscillating waveform as the output.

However, the oscillations which arise due to the inter-conversion between the two energy-forms cannot continue forever as they would be subjected to the effect of energy loss due to the resistance of the circuit. As a result, the amplitude of these oscillations decreases steadily to become zero, which makes them damped in nature.

This indicates that in order to obtain the oscillations which are continuous and of constant amplitude, one needs to compensate for the energy loss. Nevertheless, it is to be noted that the energy supplied should be precisely controlled and must be equal to that of the energy lost in order to obtain the oscillations with constant amplitude.

**Video Content / Details of website for further learning (if any):**

https://nptel.ac.in/courses/108108111/

**Important Books/Journals for further learning including the page nos.:**


- D.RoyChoudhary, SheilB.Jani, "Linear Integrated Circuits", II edition, New Age, pp. 107-125,, 2015


**Course Faculty**

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Rasipuram - 637 408, Namakkal Dist., Tamil Nadu

Estd. 2000


**L20**

## LECTURE HANDOUTS

**EEE**

**II/III**

**Course Name with Code** :**19EEC03 / Linear Integrated Circuits**

**Course Faculty** : **Mr.R.Suresh**

**Unit** :**III- Waveform Generator** **Date of Lecture:**

**Topic of Lecture:** Oscillators

**Introduction :**An **oscillator** is a circuit which produces a continuous, repeated, alternating waveform without any input. **Oscillators** basically convert unidirectional current flow from a DC source into an alternating waveform which is of the desired frequency, as decided by its circuit components

**Prerequisite knowledge for Complete understanding and learning of Topic:**

Electronic Devices

**Detailed content of the Lecture:**

This is because, if the energy supplied is more than the energy lost, then the amplitude of the oscillations will increase (Figure 2a) leading to a distorted output; while if the energy supplied is less than the energy lost, then the amplitude of the oscillations will decrease (Figure 2b) leading to unsustainable oscillations.

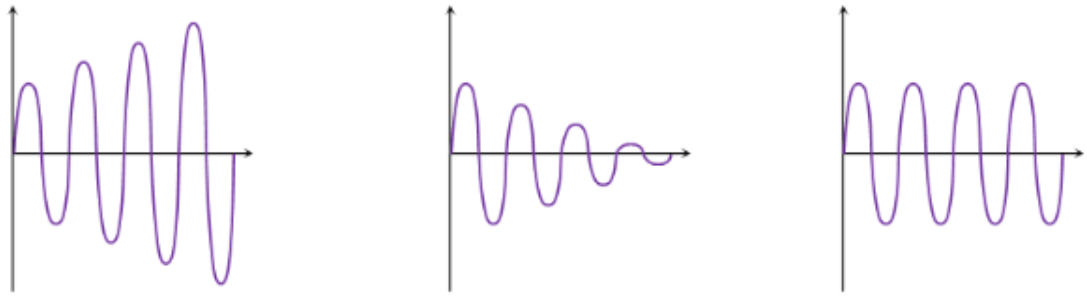


Figure 2 (a) Increasing Oscillations (b) Decaying Oscillations (c) Constant-Amplitude Oscillations

Practically, the **oscillators** are nothing but the amplifier circuits which are provided with a positive or regenerative feedback wherein a part of the output signal is fed back to the input (Figure 3). Here the amplifier consists of an amplifying active element which can be a transistor or an Op-Amp and the back-fed in-phase signal is held responsible to keep-up (sustain) the oscillations by making-up for the losses in the circuit.

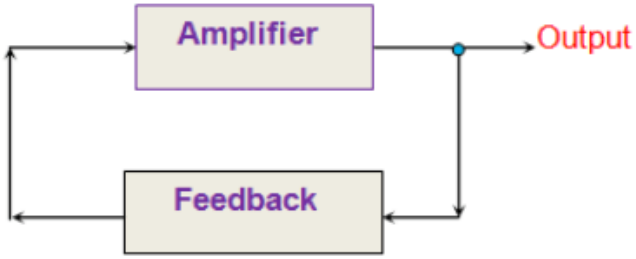


Figure 3 Typical Oscillator

Once the power supply is switched ON, the oscillations will be initiated in the system due to the electronic noise present in it. This noise signal travels around the loop, gets amplified and converges to a single frequency sine wave very quickly. The expression for the closed-loop gain of the oscillator shown in Figure 3 is given as:

$$G = \frac{A}{1 + A\beta}$$

Where A is the voltage gain of the amplifier and β is the gain of the feedback network. Here, if Aβ > 1, then the oscillations will increase in amplitude (Figure 2a); while if Aβ < 1, then the oscillations will be damped (Figure 2b). On the other hand, Aβ = 1 leads to the oscillations which are of constant amplitude (Figure 2c). In other words, this indicates that if the feedback loop gain is small, then the oscillation dies-out, while if the gain of the feedback loop is large, then the output will be distorted; and only if the gain of feedback is unity, then the oscillations will be of constant amplitude leading to self-sustained oscillatory circuit.

**Video Content / Details of website for further learning (if any):**

https://nptel.ac.in/courses/108108111/

**Important Books/Journals for further learning including the page nos.:**


- D.Roy Choudhary, Sheil B.Jani, "Linear Integrated Circuits", II edition, New Age, pp. 107-125,, 2015


**Course Faculty**

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**L21**

## LECTURE HANDOUTS

**EEE**

**II/III**

**Course Name with Code** :**19EEC03 / Linear Integrated Circuits**

**Course Faculty** : **Mr.R.Suresh**

**Unit** :**III- Waveform Generator** **Date of Lecture:**

**Topic of Lecture:** Oscillators

**Introduction :**

An **oscillator** is a circuit which produces a continuous, repeated, alternating waveform without any input. **Oscillators** basically convert unidirectional current flow from a DC source into an alternating waveform which is of the desired frequency, as decided by its circuit components

**Prerequisite knowledge for Complete understanding and learning of Topic:**

Electronic Devices

**Detailed content of the Lecture:**

There are many types of oscillators, but can broadly be classified into two main categories – Harmonic Oscillators (also known as Linear Oscillators) and Relaxation Oscillators.

In a harmonic oscillator, the energy flow is always from the active components to the passive components and the frequency of oscillations is decided by the feedback path.

Whereas in a relaxation oscillator, the energy is exchanged between the active and the passive components and the frequency of oscillations is determined by the charging and discharging time-constants involved in the process. Further, harmonic oscillators produce low-distorted sine-wave outputs while the relaxation oscillators generate non-sinusoidal (saw-tooth, triangular or square) wave-forms.

Oscillators can be also be classified into various types depending on the parameter considered i.e. based on the feedback mechanism, the shape of the output waveform, etc.. These classifications types have been given below:

1. Classification Based on the Feedback Mechanism: Positive Feedback Oscillators and Negative Feedback Oscillators.
2. Classification Based on the Shape of the Output Waveform: Sine Wave Oscillators, Square or Rectangular Wave oscillators, Sweep Oscillators (which produce saw-tooth output waveform), etc.
3. Classification Based on the Frequency of the Output Signal: Low-Frequency Oscillators, Audio Oscillators (whose output frequency is of audio range), Radio Frequency Oscillators, High-Frequency Oscillators, Very High-Frequency Oscillators, Ultra High-Frequency Oscillators, etc.
4. Classification Based on the type of the Frequency Control Used: RC Oscillators, LC Oscillators, Crystal Oscillators (which use a quartz crystal to result in a frequency stabilized output waveform), etc.

5. Classification Based on the Nature of the Frequency of Output Waveform: Fixed Frequency Oscillators and Variable or Tunable Frequency Oscillators.

## Oscillator Applications

Oscillators are a cheap and easy way to generate specific Frequency of a signal. For example, an RC oscillator is used to generate a Low Frequency signal, an LC oscillator is used to generate a High Frequency signal, and an Op-Amp based oscillator is used to generate a stable frequency.

The frequency of oscillation can be varied by varying the component value with potentiometer arrangements.

Some common applications of oscillators include:

- Quartz watches (which uses a crystal oscillator)
- Used in various audio systems and video systems
- Used in various radio, TV, and other communication devices
- Used in computers, metal detectors, stun guns, inverters, ultrasonic and radio frequency applications.
- Used to generate clock pulses for microprocessors and micro-controllers
- Used in alarms and buzzes
- Used in metal detectors, stun guns, inverters, and ultrasonic
- Used to operate decorative lights (e.g. dancing lights)

**Video Content / Details of website for further learning (if any):**

https://nptel.ac.in/courses/108108111/

**Important Books/Journals for further learning including the page nos.:**

- D.RoyChoudhary, SheilB.Jani, "Linear Integrated Circuits", II edition, New Age, pp. 107-125, 2015

**Course Faculty**

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**L22**

## LECTURE HANDOUTS

**EEE**

**II/III**

**Course Name with Code** :**19EEC03 / Linear Integrated Circuits**

**Course Faculty** : **Mr.R.Suresh**

**Unit** :**III- Waveform Generator** **Date of Lecture:**

**Topic of Lecture: sine wave**

**Introduction :**

A **sine wave** is a geometric waveform that oscillates (moves up, down or side-to-side) periodically, and is defined by the function y = sin x. In other words, it is an s-shaped, smooth **wave** that oscillates above and below zero

**Prerequisite knowledge for Complete understanding and learning of Topic:**

Electronic Devices

**Detailed content of the Lecture:**

A sine wave is a geometric waveform that oscillates (moves up, down or side-to-side) periodically, and is defined by the function $y = sin\ x$. In other words, it is an s-shaped, smooth wave that oscillates above and below zero.

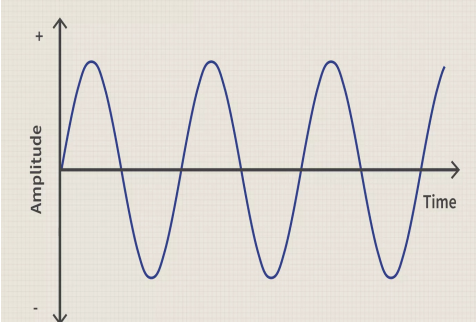
Sine waves are used in technical analysis and trading to help identify patterns and cross-overs related to oscillators.

### Key Takeaways

- A sine wave is an S-shaped waveform defined by the mathematical function y = sin x.
- In finance, market participants may identify cyclical patterns or oscillator signals from sine-wave based functions.
- The sine wave as a technical chart analysis tool is based on advanced mathematics and is designed to indicate whether a market is trending or in a cycle mode.

### Understanding Sine Waves

The sine wave indicator is based on the assumption that markets move in cyclical patterns. After quantifying a cycle, a trader may try to use the pattern to develop a leading indicator. This works extremely well when the market is indeed moving in a cycle. When the market is trending, however, this system fails (and one should adjust for that).




Markets alternate between periods of cycling and trending. Cyclical periods are characterized by price bouncing off support or resistance levels and failed breakouts or overshoots. Trending periods are characterized by new highs or new lows and pull backs that then continue in the direction of the trend, until exhausted.

In technical analysis, oscillators are often used that may have sine-shaped characteristics. An oscillator exists between two extreme values and then builds a trend indicator with the results. The analysts then use the trend indicator to discover short-term overbought or oversold conditions. When the value of the oscillator approaches the upper extreme value, analysts interpret that information to mean that the asset is overbought, and as it approaches the lower extreme, analysts consider the asset to be oversold.

## Sine Waves as Analytical Tools

The sine wave as a technical chart analysis tool is based on advanced mathematics and is designed to indicate whether a market is trending or in a cycle mode. It helps traders identify the start and finish of a trending move as well as possible shifts in the trend.

This leading indicator is also called the MESA indicator and was developed by John Ehlers based on an algorithm that was originally applied to digital signal processing. It consists of two lines, called the Sine Wave and the Lead Wave. When the price is trending, the lines do not cross and usually run parallel and distant from each other.

Line crossovers could indicate turning points and generate buy or sell signals under the right conditions. The indicator can also signal an overbought or oversold market (i.e., unjustifiably high or unjustifiably low), which can have implications on the prevailing trend. Whether used alone or in combination with other techniques or non-correlated indicators (such as moving average-based indicators), the sine waves are very useful for a trader.

The Composite Index of Lagging Indicators resembles a sine wave since the measures that make up the index (i.e. ratios and interest rates) tend to oscillate between a range of values.

**Video Content / Details of website for further learning (if any):**

https://nptel.ac.in/courses/108108111/

**Important Books/Journals for further learning including the page nos.:**


- D.Roy Choudhary, Sheil B.Jani, “Linear Integrated Circuits”, II edition, New Age, pp. 140-143, 2015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**L23**

## LECTURE HANDOUTS

**EEE**

**II/III**

**Course Name with Code** :19EEC03 / Linear Integrated Circuits

**Course Faculty** : Mr.R.Suresh

**Unit** :III- Waveform Generator **Date of Lecture:**

**Topic of Lecture:** Square Wave

**Introduction :**

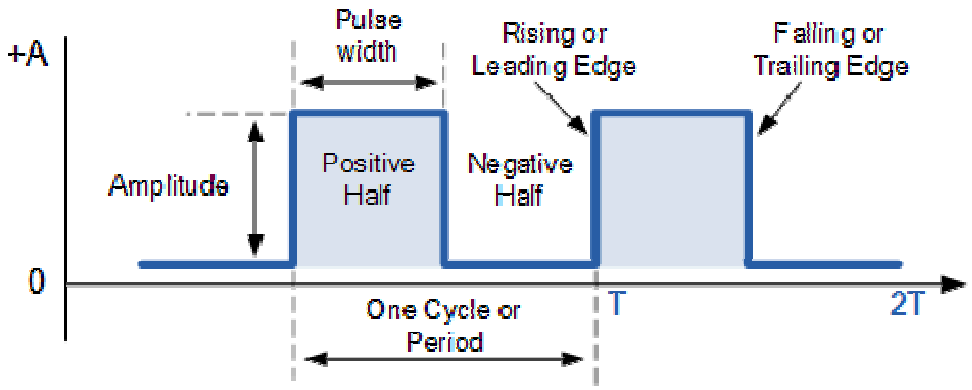
A **square wave** is a non-sinusoidal periodic **waveform** in which the amplitude alternates at a steady frequency between fixed minimum and maximum values, with the same duration at minimum and maximum. In an ideal **square wave**, the transitions between minimum and maximum are instantaneous

**Prerequisite knowledge for Complete understanding and learning of Topic:**

Electronic Devices

**Detailed content of the Lecture:**

### In the A Square Wave Waveform




We know that square shaped electrical waveforms are symmetrical in shape as each half of the cycle is identical, so the time that the pulse width is positive must be equal to the time that the pulse width is negative or zero. When square wave waveforms are used as “clock” signals in digital circuits the time of the positive pulse width is known as the “Duty Cycle” of the period.

Then we can say that for a square wave waveform the positive or “ON” time is equal to the negative or “OFF” time so the duty cycle must be 50%, (half of its period). As frequency is equal to the reciprocal of the period, ( 1/T ) we can define the frequency of a square wave waveform as:

$$\text{Frequency} = \frac{1}{\text{"ON" time} + \text{"OFF" time}}$$

## Electrical Waveforms Example No1

A Square Wave electrical waveform has a pulse width of 10ms, calculate its frequency, ( $f$ ).

For a square wave shaped waveform, the duty cycle is given as 50%, therefore the period of the waveform must be equal to: 10ms + 10ms or 20ms

$$\text{Frequency} = \frac{1}{\text{Period}} = \frac{1}{10\text{mS} + 10\text{mS}} = 50\text{Hz}$$

So to summarise a little about Square Waves. A **Square Wave Waveform** is symmetrical in shape and has a positive pulse width equal to its negative pulse width resulting in a 50% duty cycle. Square wave waveforms are used in digital systems to represent a logic level "1", high amplitude and logic level "0", low amplitude. If the duty cycle of the waveform is any other value than 50%, (half-ON half-OFF) the resulting waveform would then be called a **Rectangular Waveform** or if the "ON" time is really small a **Pulse**.

**Video Content / Details of website for further learning (if any):**

https://nptel.ac.in/courses/108108111/

**Important Books/Journals for further learning including the page nos.:**

- D.RoyChoudhary, SheilB.Jani, "Linear Integrated Circuits", II edition, New Age, pp. 111-113, 2015

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**L24**

## LECTURE HANDOUTS

**EEE**

**II/III**

**Course Name with Code** :19EEC03 / Linear Integrated Circuits

**Course Faculty** : Mr.R.Suresh

**Unit** :III- Waveform Generator **Date of Lecture:**

**Topic of Lecture:** Triangular Wave

**Introduction :**

**Triangular Waveforms** are generally bi-directional non-sinusoidal waveforms that oscillate between a positive and a negative peak value. Although called a triangular waveform, the triangular wave is actually more of a symmetrical linear ramp waveform because it is simply a slow rising and falling voltage signal at a constant frequency or rate.

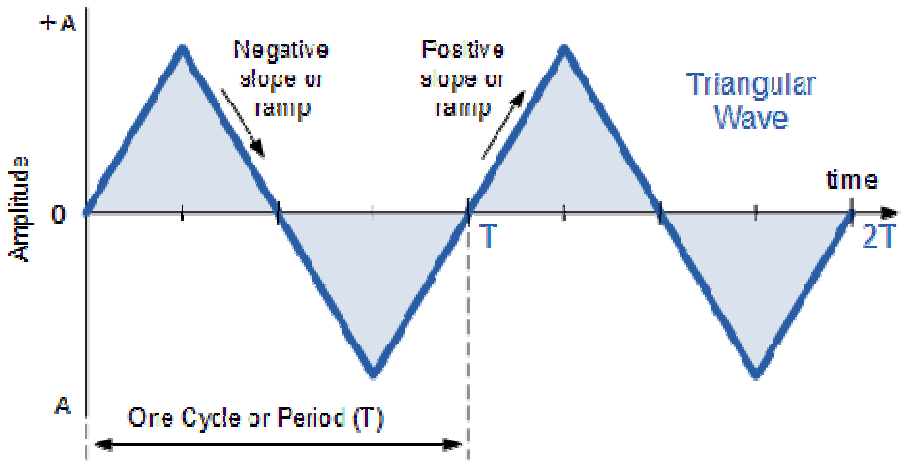
**Prerequisite knowledge for Complete understanding and learning of Topic:**

Electronic Devices

**Detailed content of the Lecture:**

The rate at which the voltage changes between each ramp direction is equal during both halves of the cycle as shown below.

### A Triangular Waveform




Generally, for **Triangular Waveforms** the positive-going ramp or slope (rise), is of the same time duration as the negative-going ramp (decay) giving the triangular waveform a 50% duty cycle. Then any given voltage amplitude, the frequency of the waveform will determine the average voltage level of the wave.

So for a slow rise and slow delay time of the ramp will give a lower average voltage level than a faster rise and decay time. However, we can produce non-symmetrical triangular waveforms by varying either the rising or decaying ramp values to give us another type of waveform known commonly as a **Sawtooth Waveform**.

**Video Content / Details of website for further learning (if any):**

https://nptel.ac.in/courses/108108111/

**Important Books/Journals for further learning including the page nos.:**

- D.Roy Choudhary, Sheil B.Jani, "Linear Integrated Circuits", II edition, New Age, pp. 113-115, 2015

**Course Faculty**

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## LECTURE HANDOUTS

**EEE**

**II/III**

**Course Name with Code** :19EEC03 / Linear Integrated Circuits

**Course Faculty** : Mr.R.Suresh

**Unit** :III- Waveform Generator **Date of Lecture:**

**Topic of Lecture:** Saw Tooth Wave Generation

**Introduction :**

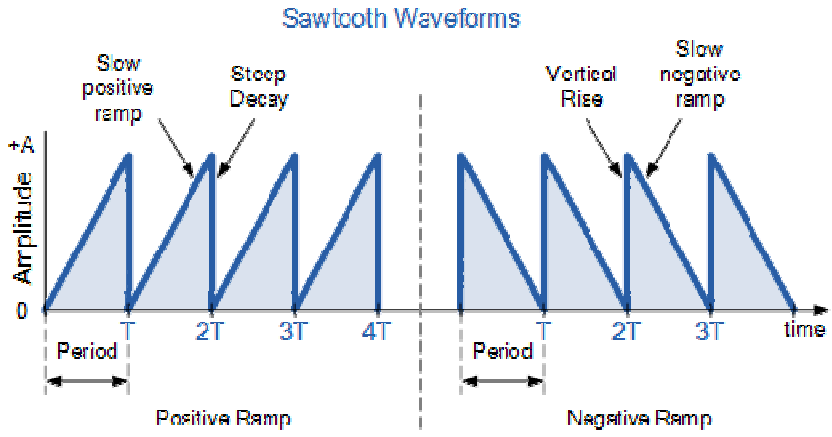
**Sawtooth Waveforms** are another type of periodic waveform. As its name suggests, the shape of the waveform resembles the teeth of a saw blade. Sawtoothed waveforms can have a mirror image of themselves, by having either a slow-rising but extremely steep decay, or an extremely steep almost vertical rise and a slow-decay as shown below.

**Prerequisite knowledge for Complete understanding and learning of Topic:**

Electronic Devices

**Detailed content of the Lecture:**

### Sawtooth Waveforms




The positive ramp **Sawtooth Waveform** is the more common of the two waveform types with the ramp portion of the wave being almost perfectly linear. The Sawtooth waveform is commonly available from most function generators and consists of a fundamental frequency ( $f$ ) and all its integer ratios of harmonics, such as: 1/2, 1/4, 1/6 1/8 … 1/n etc. What this means in practical terms is that the **Sawtoothed Waveform** is rich in harmonics and for music synthesizers and musicians gives the quality of the sound or tonal colour to their music without any distortion.

**Video Content / Details of website for further learning (if any):**

https://nptel.ac.in/courses/108108111/

**Important Books/Journals for further learning including the page nos.:**

- D.RoyChoudhary, SheilB.Jani, "Linear Integrated Circuits", II edition, New Age, pp. 118-120, 2015

**Course Faculty**

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**L26**

## LECTURE HANDOUTS

**EEE**

**II/III**

**Course Name with Code** :**19EEC03 / Linear Integrated Circuits**

**Course Faculty** : **Mr.R.Suresh**

**Unit** :**III- Waveform Generator** **Date of Lecture:**

**Topic of Lecture:** Schmitt Trigger

**Introduction :**

When operating an Op-Amp in the open loop mode where a feedback is not used, for example, in a Basic Comparator Circuit, the very large open loop gain of the Op-Amp will cause the smallest of noise voltage to trigger the comparator.

If the comparator is being used as a Zero Crossing Detector, then such false triggering can cause a lot of problems. It may give a wrong indication of Zero Crossing due to zero crossing of the noise rather than the actual input signals' zero crossing.

To avoid such unnecessary switching between high and low states of the output, a special circuit called Schmitt Trigger is used, which involves a positive feedback.

**Prerequisite knowledge for Complete understanding and learning of Topic:**

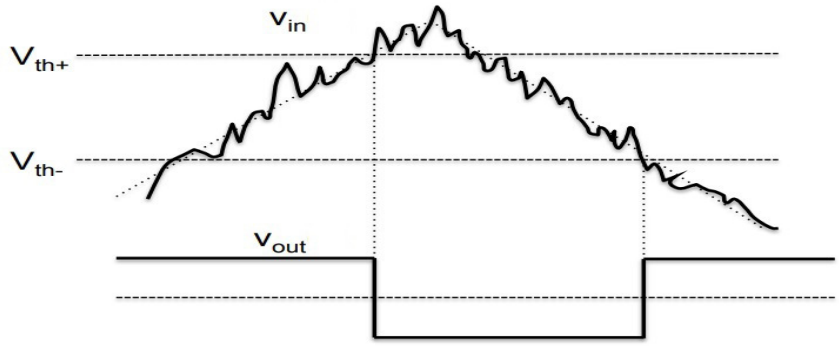
Electronic Devices

**Detailed content of the Lecture:**

Schmitt Trigger was invented by Otto Schmitt early 1930's. It is an electronic circuit that adds hysteresis to the input-output transition threshold with the help of positive feedback. Hysteresis here means it provides two different threshold voltage levels for rising and falling edge.

Essentially, a Schmitt Trigger is a Bi-stable Multivibrator and its output remains in either of the stable states indefinitely. For the output to change from one stable state to other, the input signal must change (or trigger) appropriately.

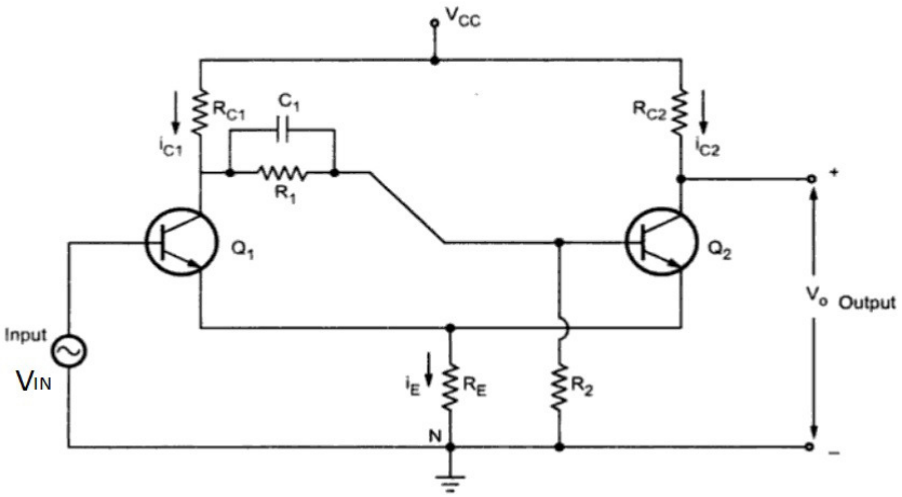
This Bistable operation of the Schmitt Trigger requires an amplifier with positive feedback (or regenerative feedback) with a loop gin greater than one. Hence, Schmitt Trigger is also known as Regenerative Comparator.




For example, if we have a noisy input signal as shown below, the two thresholds of the Schmitt Trigger Circuit will correctly determine the pulses. Hence, the basic function of a Schmitt Trigger is to convert noisy square, sine, triangular or any periodic signals into clean square pulses with sharp leading and trailing edges.

**Schmitt Trigger using Transistors**

As mentioned earlier, a Schmitt Trigger is basically a Bistable Circuit whose output states are controlled by the input signal. Hence, it can be used as a level detecting circuit. The following circuit shows a simple design of Transistor based Schmitt Trigger.




Even though this circuit looks like a typical Bistable Multivibrator circuit, it is actually different as this circuit is missing the coupling from collector of Q2 to input of Q1. Emitters of Q1 and Q2 are connected to each other and grounded through $R_E$. Also, $R_E$ acts as a feedback path.

***Operation of the Circuit***

When $V_{IN}$ is zero, Q1 is cut-off and Q2 is in saturation. As a result, the output voltage $V_O$ is LOW. If $V_{CE(SAT)}$ is assumed to be 0, then the voltage across $R_E$ is given by:

$$(V_{CC} \times R_E) / (R_E + R_{C2})$$

This voltage is also the emitter voltage of Q1. So, for Q1 to conduct, the input voltage $V_{IN}$ must greater than sum of the emitter voltage and 0.7 V i.e.

$$V_{IN} = (V_{CC} \times R_E) / (R_E + R_{C2}) + 0.7$$

When the $V_{IN}$ is greater than this voltage, Q1 starts conducting and Q2 is cutoff due to regenerative action. As a result, the output $V_O$ goes HIGH. Now the voltage across the $R_E$ changes to a new value and is given by:

$(V_{CC} \times R_E) / (R_E + R_{C1})$

Transistor Q1 will conduct as long as the input voltage $V_{IN}$ is greater than or equal to the following:

$V_{IN} = (V_{CC} \times R_E) / (R_E + R_{C1}) + 0.7$

If $V_{IN}$ falls below this value, then Q1 comes out of saturation and the rest of the circuit operates is due to regenerative action of Q1 going to cutoff and Q2 to saturation.

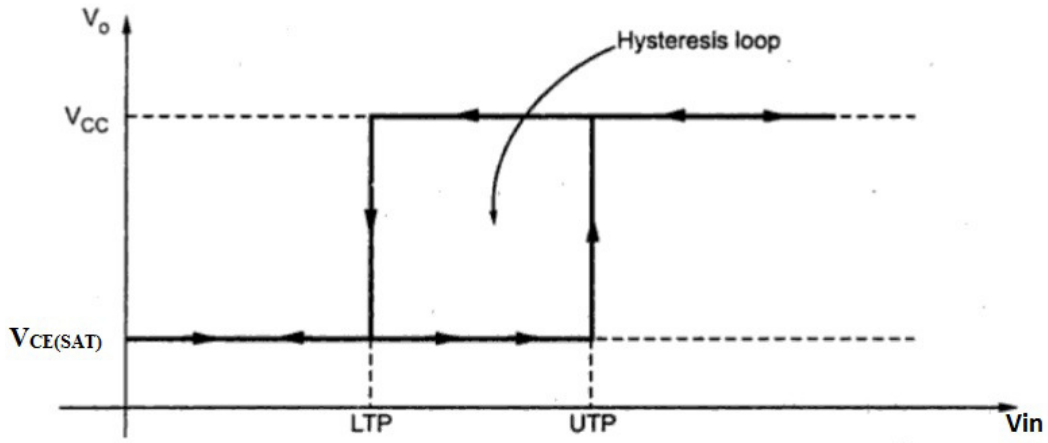
The output states HIGH and LOW are dependent on the input voltage levels given by the equations

$(V_{CC} \times R_E) / (R_E + R_{C1}) + 0.7$ and $(V_{CC} \times R_E) / (R_E + R_{C2}) + 0.7$

The transfer characteristics of a Schmitt Trigger exhibit hysteresis and are governed by the Lower Trip point (Lower Threshold Voltage) and Upper Trip point (Upper Threshold Voltage) given by $V_{LT}$ and $V_{UT}$.

$V_{LT} = (V_{CC} \times R_E) / (R_E + R_{C1}) + 0.7$

$V_{UT} = (V_{CC} \times R_E) / (R_E + R_{C2}) + 0.7$




By changing the values of $R_{C1}$ and $R_{C2}$, the amount of hysteresis can be controlled while the value of $R_E$ can be used to increase the Upper Threshold Voltage.

**Video Content / Details of website for further learning (if any):**

https://nptel.ac.in/courses/108108111/

**Important Books/Journals for further learning including the page nos.:**

- D.Roy Choudhary, Sheil B.Jani, "Linear Integrated Circuits", II edition, New Age, pp. 125-129, 2015

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**L27**

## LECTURE HANDOUTS

**EEE**

**II/III**

**Course Name with Code** :19EEC03 / Linear Integrated Circuits

**Course Faculty** : Mr.R.Suresh

**Unit** :III- Waveform Generator **Date of Lecture:**

**Topic of Lecture:** Window Detector

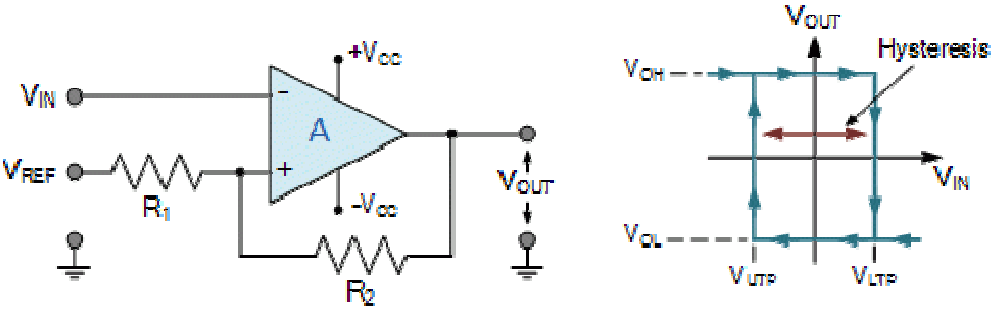
**Introduction :**

A *window detector* circuit, also called *window comparator* circuit or dual edge limit *detector* circuits is used to determine whether an unknown input is between two precise reference threshold voltages. It employs two comparators to detect over-voltage or under-voltage.

**Prerequisite knowledge for Complete understanding and learning of Topic:**

Electronic Devices

**Detailed content of the Lecture:**




The **Op-amp comparator** compares one analogue voltage level with another analogue voltage level, or some preset reference voltage, $V_{REF}$ and produces an output signal based on this voltage comparison. In other words, the op-amp voltage comparator compares the magnitudes of two voltage inputs and determines which is the largest of the two.

We have seen in previous tutorials that the operational amplifier can be used with negative feedback to control the magnitude of its output signal in the linear region performing a variety of different functions. We have also seen that the standard operational amplifier is characterised by its open-loop gain $A_O$ and that its output voltage is given by the expression: $V_{OUT} = A_O(V+ - V-)$ where V+ and V- correspond to the voltages at the non-inverting and the inverting terminals respectively.

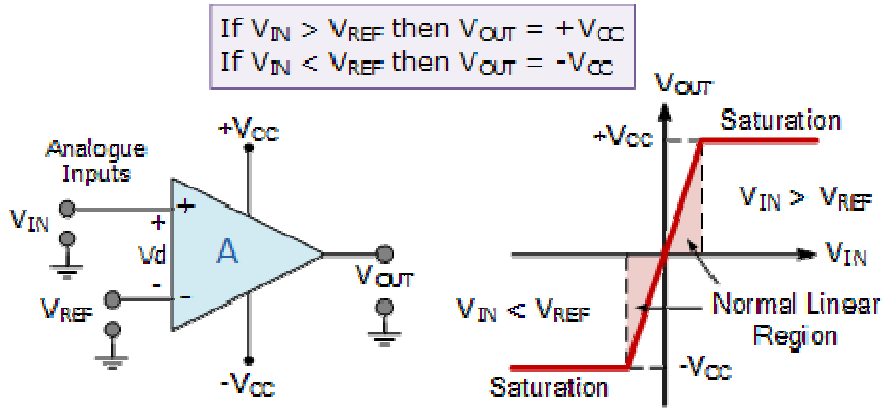
*Voltage comparators* on the other hand, either use positive feedback or no feedback at all (open-loop mode) to switch its output between two saturated states, because in the open-loop mode the amplifiers voltage gain is basically equal to $A_{VO}$. Then due to this high open loop gain, the output from the comparator swings either fully to its positive supply rail, +Vcc or fully to its negative supply rail, -Vcc on the application of varying input signal which passes some preset threshold value.

The open-loop op-amp comparator is an analogue circuit that operates in its non-linear region as changes in the two analogue inputs, V+ and V- causes it to behave like a digital *bistable* device as

triggering causes it to have two possible output states, +Vcc or -Vcc. Then we can say that the voltage comparator is essentially a 1-bit analogue to digital converter, as the input signal is analogue but the output behaves digitally.

Consider the basic **op-amp voltage comparator** circuit below.

## Op-amp Comparator Circuit




With reference to the op-amp comparator circuit above, lets first assume that $V_{IN}$ is less than the DC voltage level at $V_{REF}$, ( $V_{IN} < V_{REF}$ ). As the non-inverting (positive) input of the comparator is less than the inverting (negative) input, the output will be LOW and at the negative supply voltage, -Vcc resulting in a negative saturation of the output.

If we now increase the input voltage, $V_{IN}$ so that its value is greater than the reference voltage $V_{REF}$ on the inverting input, the output voltage rapidly switches HIGH towards the positive supply voltage, +Vcc resulting in a positive saturation of the output. If we reduce again the input voltage $V_{IN}$, so that it is slightly less than the reference voltage, the op-amp's output switches back to its negative saturation voltage acting as a threshold detector.

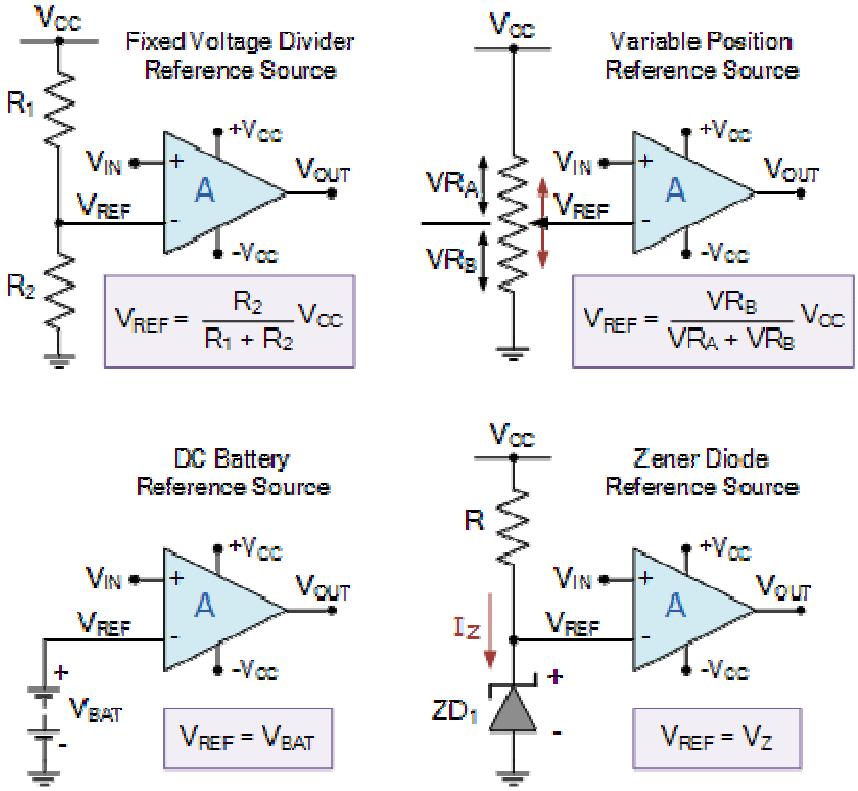
Then we can see that the op-amp voltage comparator is a device whose output is dependant on the value of the input voltage, $V_{IN}$ with respect to some DC voltage level as the output is HIGH when the voltage on the non-inverting input is greater than the voltage on the inverting input, and LOW when the non-inverting input is less than the inverting input voltage. This condition is true regardless of whether the input signal is connected to the inverting or the non-inverting input of the comparator.

We can also see that the value of the output voltage is completely dependent on the op-amps power supply voltage. In theory due to the op-amps high open-loop gain the magnitude of its output voltage could be infinite in both directions, ($\pm\infty$). However practically, and for obvious reasons it is limited by the op-amps supply rails giving $V_{OUT}$ = +Vcc or $V_{OUT}$ = -Vcc.

We said before that the basic op-amp comparator produces a positive or negative voltage output by comparing its input voltage against some preset DC reference voltage.

Generally, a resistive voltage divider is used to set the input reference voltage of a comparator, but a battery source, zener diode or potentiometer for a variable reference voltage can all be used as shown.

## Comparator Reference Voltages




In theory the comparators reference voltage can be set to be anywhere between 0v and the supply voltage but there are practical limitations on the actual voltage range depending on the op-amp comparator being device used.

## Positive and Negative Voltage Comparators

A basic op-amp comparator circuit can be used to detect either a positive or a negative going input voltage depending upon which input of the operational amplifier we connect the fixed reference voltage source and the input voltage too. In the examples above we have used the inverting input to set the reference voltage with the input voltage connected to the non-inverting input.

But equally we could connect the inputs of the comparator the other way around inverting the output signal to that shown above. Then an op-amp comparator can be configured to operate in what is called an inverting or a non-inverting configuration.

**Video Content / Details of website for further learning (if any):**

https://nptel.ac.in/courses/108108111/

**Important Books/Journals for further learning including the page nos.:**


- D.Roy Choudhary, Sheil B.Jani, "Linear Integrated Circuits", II edition, New Age, pp. 132-139, 2015


**Course Faculty**

# MUTHAYAMMAL ENGINEERING COLLEGE

(An Autonomous Institution)

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Rasipuram - 637 408, Namakkal Dist., Tamil Nadu

Estd. 2000


**L28**

## LECTURE HANDOUTS

**EEE**

**II/III**

**Course Name with Code** :**19EEC03 / Linear Integrated Circuits**

**Course Faculty** : **Mr.R.Suresh**

**Unit** :**IV- D/A & A/D Convertors and Phase Locked Loop** **Date of Lecture:**

**Topic of Lecture:** Analog to Digital Converter

**Introduction :Analogue-to-Digital Converters**, (ADCs) allow micro-processor controlled circuits, Arduinos, Raspberry Pi, and other such digital logic circuits to communicate with the real world. In the real world, analogue signals have continuously changing values which come from various sources and sensors which can measure sound, light, temperature or movement, and many digital systems interact with their environment by measuring the analogue signals from such transducers.

**Prerequisite knowledge for Complete understanding and learning of Topic:**

Electronic Devices

**Detailed content of the Lecture:**

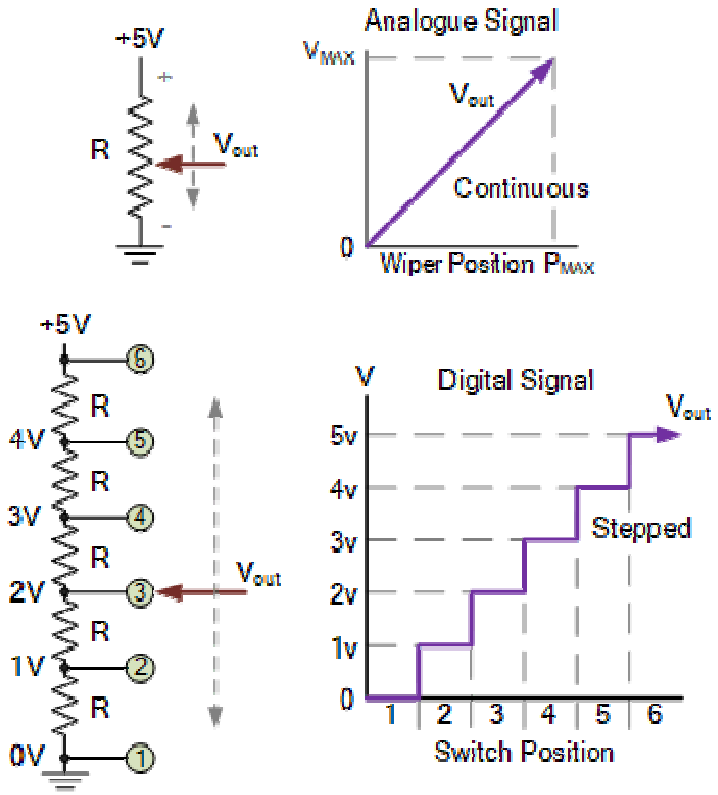
While analogue signals can be continuous and provide an infinite number different voltage values, digital circuits on the other hand work with binary signal which have only two discrete states, a logic "1" (HIGH) or a logic "0" (LOW). So it is necessary to have an electronic circuit which can convert between the two different domains of continuously changing analogue signals and discrete digital signals, and this is where *Analogue-to-Digital Converters* (A/D) come in.

Basically an analogue to digital converter takes a snapshot of an analogue voltage at one instant in time and produces a digital output code which represents this analogue voltage. The number of binary digits, or bits used to represent this analogue voltage value depends on the resolution of an A/D converter.

For example a 4-bit ADC will have a resolution of one part in 15, $(2^4 - 1)$ whereas an 8-bit ADC will have a resolution of one part in 255, $(2^8 - 1)$. Thus an analogue to digital converter takes an unknown continuous analogue signal and converts it into an "n"- bit binary number of $2^n$ bits.

But first let us remind ourselves of the differences between an analogue (or analog) signal and a digital signal as shown:

### Analogue and Digital Signals




Here we can see that as the wiper terminal of the potentiometer is rotated between between 0 volts and $V_{MAX}$, it produces a continuous output signal (or voltage) which has an infinite number of output values relative to the wiper position. As the potentiometers wiper is adjusted from one position to the next, there is no sudden or step change between the two voltage levels thereby producing a continuously variable output voltage. Examples of analogue signals include temperature, pressure, liquid levels and light intensity.

For a digital circuit the potentiometer wiper has been replaced by a single rotary switch which is connected in turn to each junction of the series resistor chain, forming a basic potential divider network. As the switch is rotated from one position (or node) to the next the output voltage, $V_{OUT}$ changes quickly in discrete and distinctive voltage steps representing multiples of 1.0 volts on each switching action or step as shown.

So for example, the output voltage will be 2 volts, 3 volts, 5 volts, etc. but NOT 2.5V, 3.1V or 4.6V. Finer output voltage levels could easily be produced by using a multi-positional switch and increasing the number of resistive elements within the potential divider network, therefore increasing the number of discrete switching steps.

Then we can see that the major differences between an analogue signal and a digital signal is that an "Analogue" quantity is continuously changing over time while a "Digital" quantity has discrete (step by step) values. "LOW" to "HIGH" or "HIGH" to "LOW".

So how can we convert a continously changing signal with an infinite number of values to one which has distinct values or steps for use by a digital circuit.

## Analogue-to-Digital Converter

The process of taking an analogue voltage signal and converting it into an equivalent digital signal can be done in many different ways, and while there are many analogue-to-digital converter chips such as the ADC08xx series available from various manufacturers, it is possible to build a simple ADC using discrete components. One simple and easy way is by using parallel encoding, also known as *flash*, *simultaneous*, or *multiple comparator* converters in which comparators are used to detect different voltage levels and output their switching state to an encoder.

| **Video Content / Details of website for further learning (if any):** |
| --- |
| https://nptel.ac.in/courses/108108111/ |
| **Important Books/Journals for further learning including the page nos.:**<br>• D.RoyChoudhary, SheilB.Jani, "Linear Integrated Circuits", II edition, New Age, pp. 166-165, 2015 |

**Course Faculty**

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**L29**

## LECTURE HANDOUTS

**EEE**

**II/III**

**Course Name with Code** :**19EEC03 / Linear Integrated Circuits**

**Course Faculty** : **Mr.R.Suresh**

**Unit** :**IV- D/A & A/D Convertors and Phase Locked Loop** **Date of Lecture:**

**Topic of Lecture:** Digital to Analog

**Introduction :**

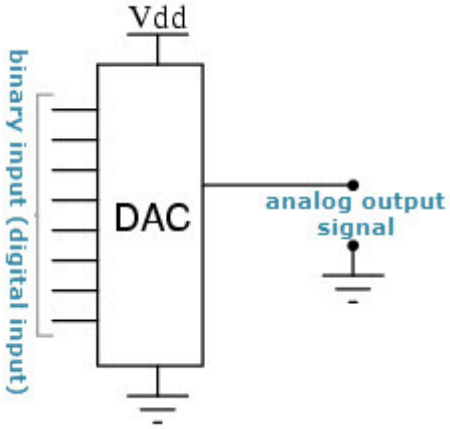
Digital to Analog Converter (DAC) is a device that transforms digital data into an analog signal. According to the Nyquist-Shannon sampling theorem, any sampled data can be reconstructed perfectly with bandwidth and Nyquist criteria.

**Prerequisite knowledge for Complete understanding and learning of Topic:**

Electronic Devices

**Detailed content of the Lecture:**

A DAC can reconstruct sampled data into an analog signal with precision. The digital data may be produced from a microprocessor, Application Specific Integrated Circuit (ASIC), or Field Programmable Gate Array (FPGA), but ultimately the data requires the conversion to an analog signal in order to interact with the real world.



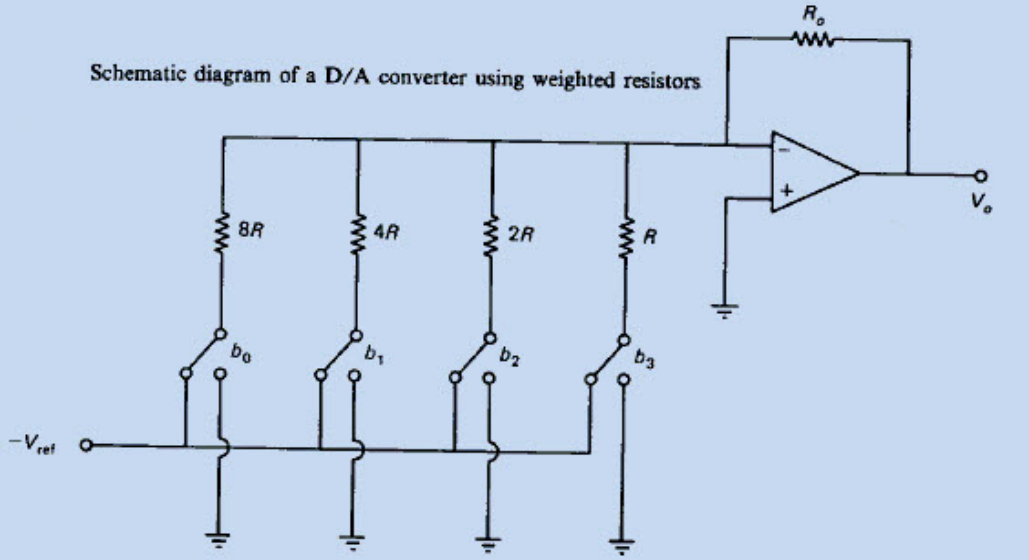

### D/A Converter Architectures

There are two methods commonly used for digital to analog conversion: Weighted Resistors method and the other one is using the R-2R ladder network method.

### DAC using Weighted Resistors method

The below shown schematic diagram is DAC using weighted resistors. The basic operation of DAC is the ability to add inputs that will ultimately correspond to the contributions of the various bits of the

digital input. In the voltage domain, that is if the input signals are voltages, the addition of the binary bits can be achieved using the inverting summing amplifier shown in the below figure.




In the voltage domain, that is if the input signals are voltages, the addition of the binary bits can be achieved using the inverting summing amplifier shown in the above figure.

The input resistors of the op-amp have their resistance values weighted in a binary format. When the receiving binary 1 the switch connects the resistor to the reference voltage. When the logic circuit receives binary 0, the switch connects the resistor to ground. All the digital input bits are simultaneously applied to the DAC.

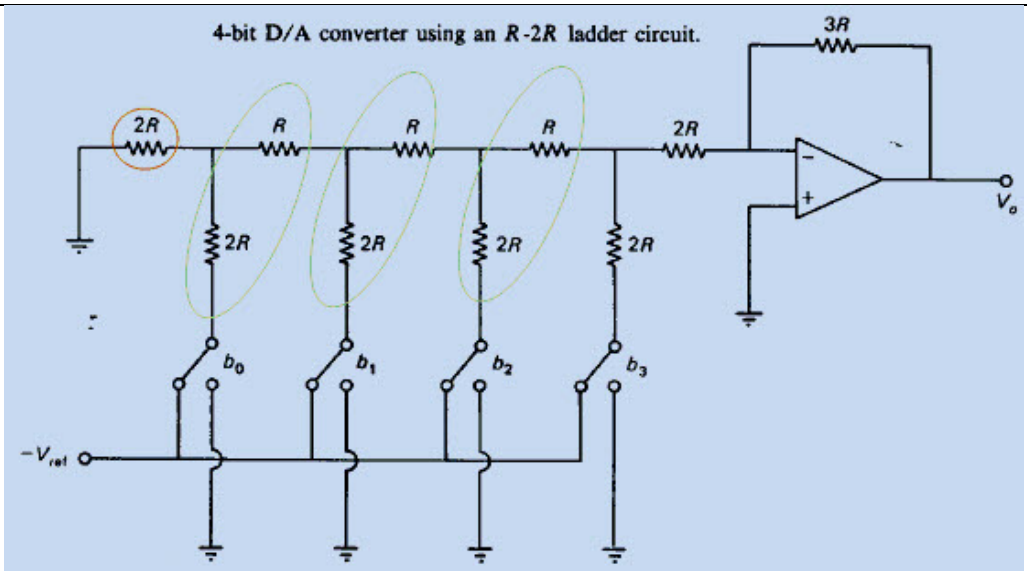
The DAC generates analog output voltage corresponding to the given digital data signal. For the DAC the given digital voltage is b3 b2 b1 b0 where each bit is a binary value (0 or 1). The output voltage produced at output side is

$$V0=R0/R\ (b3+b2/2+b1/4+b0/8)\ Vref$$

As the number of bits is increasing in the digital input voltage, the range of the resistor values becomes large and accordingly, the accuracy becomes poor.

## R-2R Ladder Digital to Analog Converter (DAC)

The R-2R ladder DAC constructed as a binary-weighted DAC that uses a repeating cascaded structure of resistor values R and 2R. This improves the precision due to the relative ease of producing equal valued-matched resistors (or current sources).




The above figure shows the 4-bit R-2R ladder DAC. In order to achieve high-level accuracy, we have chosen the resistor values as R and 2R. Let the binary value B3 B2 B1 B0, if b3=1, b2=b1=b0=0, then the circuit is shown in the figure below it is a simplified form of the above DAC circuit. The output voltage is V0=3R(i3/2)= Vref/2

**Video Content / Details of website for further learning (if any):**

https://nptel.ac.in/courses/108108111/

**Important Books/Journals for further learning including the page nos.:**

- D.RoyChoudhary, SheilB.Jani, "Linear Integrated Circuits", II edition, New Age, pp. 169-172, 2015

**Course Faculty**

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**L30**

## LECTURE HANDOUTS

**EEE**

**II/III**

**Course Name with Code** :**19EEC03 / Linear Integrated Circuits**

**Course Faculty** : **Mr.R.Suresh**

**Unit** :**IV- D/A & A/D Convertors and Phase Locked Loop** **Date of Lecture:**

**Topic of Lecture:** Sample Circuits

**Introduction :**

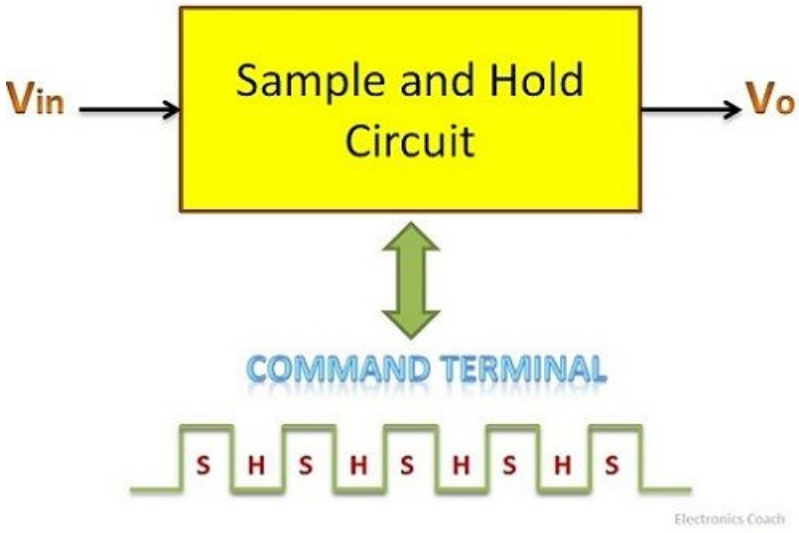
The **Sample and Hold circuit** is an electronic circuit which creates the samples of voltage given to it as input, and after that, it holds these samples for the definite time. The time during which sample and hold circuit generates the sample of the input signal is called **sampling time.** Similarly, the time duration of the circuit during which it holds the sampled value is called **holding time.**

**Prerequisite knowledge for Complete understanding and learning of Topic:**

Electronic Devices

**Detailed content of the Lecture:**

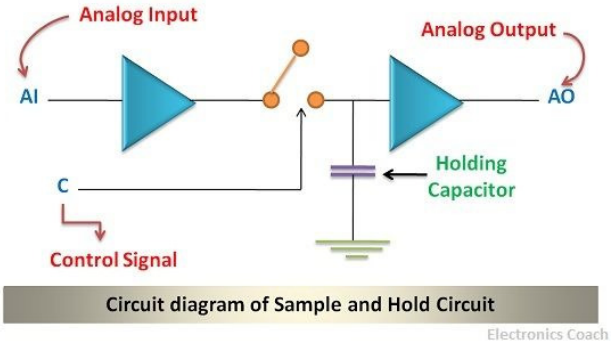
Sampling time is generally between **1µs to 14 µs** while the holding time can assume any value as required in the application.It will not be wrong to say that capacitor is the heart of sample and hold circuit. This is because the capacitor present in it charges to its peak value when the switch is opened, i.e. during sampling and holds the sampled voltage when the switch is closed.




## Circuit Diagram of Sample and Hold Circuit

The diagram below shows the circuit of the sample and hold circuit with the help of an Operational Amplifier. It is evident from the circuit diagram that two OP-AMPS are connected via a switch. When the switch is closed sampling process will come into the picture and when the switch is opened holding

effect will be there.




The capacitor connected to the second operational amplifier is nothing but a holding capacitor.

**Significance**

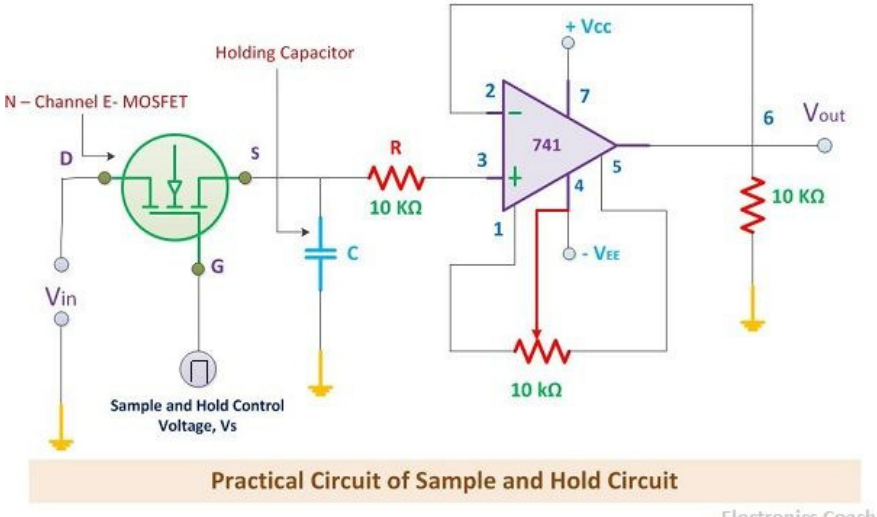
Now, you all are aware that what is the sample and hold circuit. But what are the driving forces which have turned us in the direction to use the sample and hold circuit? To understand this, we need to enter into communication realm. We all know digital communication is better than analogue communication, but why? What is wrong with analogue communication?

The **noise interference** is the real culprit. It makes analogue communication less efficient and less reliable. Thus, in digital communication, we need digital signals. But naturally, all the signals are analogue. This is the turning point where we need a sample and hold circuit.

With the help of sample and hold circuit we can take samples of the analogue signal, followed by a capacitor. It holds these sample for a particular period. As a consequence of this, a constant signal is generated this can be converted into the digital signal with the help of analogue to digital converters.

## Working of Sample and Hold Circuit

The working of sample and hold circuit can be easily understood with the help of working of its components. The main components which a sample and hold circuit involves is an **N-channel Enhancement type MOSFET**, a **capacitor** to store and hold the electric charge and a high precision **Operational amplifier**.




The N-channel Enhancement MOSFET will be used a switching element. The input voltage is applied through its drain terminal and control voltage will be applied through its gate terminal. When the positive pulse of the control voltage is applied, the MOSFET will be switched to ON state. And it acts as a closed switch. On the contrary, when the control voltage is zero then the MOSFET will be switched to OFF state and acts as the open switch.

When the MOSFET acts as a closed switch, then the analogue signal applied to it through the drain terminal will be fed to the capacitor. The capacitor will then charge to its peak value. When the MOSFET switch is opened, then the capacitor stops charging. Due to the high impedance operational amplifier connected at the end of the circuit, the capacitor will experience high impedance due to this it cannot get discharged.

**Video Content / Details of website for further learning (if any):**

https://nptel.ac.in/courses/108108111/

**Important Books/Journals for further learning including the page nos.:**


- D.Roy Choudhary, Sheil B.Jani, "Linear Integrated Circuits", II edition, New Age, pp. 186-189, 2015


**Course Faculty**

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**L31**

## LECTURE HANDOUTS

**EEE**

**II/III**

**Course Name with Code** :**19EEC03 / Linear Integrated Circuits**

**Course Faculty** : **Mr.R.Suresh**

**Unit** :**IV- D/A & A/D Convertors and Phase Locked Loop** **Date of Lecture:**

**Topic of Lecture:**Hold Circuits

**Introduction :**

**Hold Circuit** takes samples from the analog input signal and hold them for particular period of time and then outputs the sampled part of input signal. This circuit is only useful for sampling few microseconds of input signal.

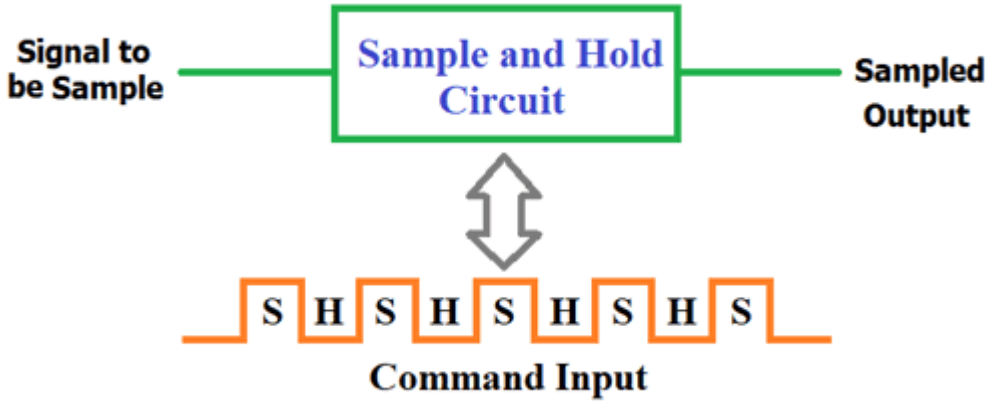
**Prerequisite knowledge for Complete understanding and learning of Topic:**

Electronic Devices

**Detailed content of the Lecture:**

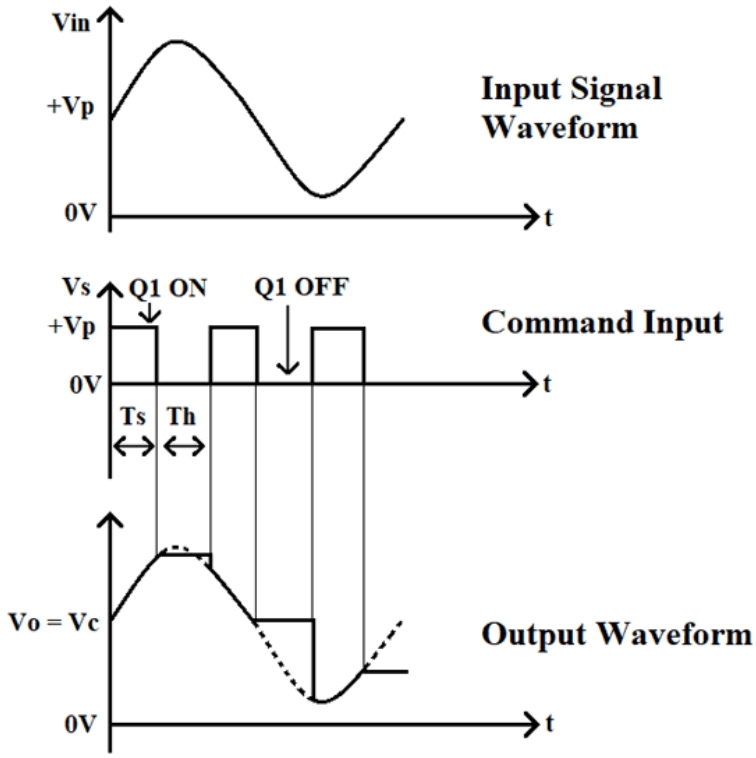
A Sample and Hold circuit consist of switching devices, capacitor and an operational amplifier. Capacitor is the heart of the **Sample and Hold Circuit** because it is the one who holds the sampled input signal and provide it at output according to command input. This circuit is mostly used in Analog to Digital Converters to remove certain variations in input signal, which may corrupt conversion process.

A typical **block diagram of Sample and hold circuit** is mentioned below:

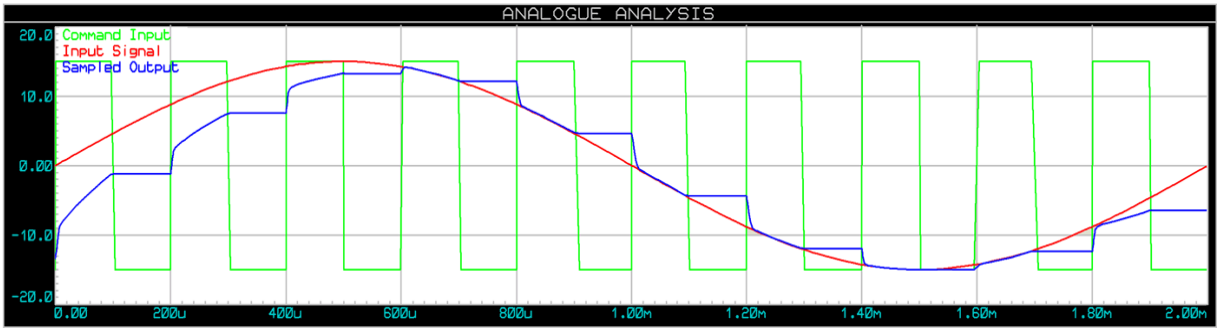



Generally applied input voltage signal is a continuously changing analog signal. Command input is provided to trigger the sampling and holding of input signal. **Command input** is nothing but a on/off signal to start/stop sampling of input signal, it is generally PWM. The sampling and holding process is depends upon the command input. When the switch is closed the signal is sampled and when its open the circuit holds the output signal. The On/OFF condition of switch is controlled by command input.

The ideal **input and output waveform of the sample and hold circuit** is given below:




It can be clearly understood from the above diagram that this circuit takes samples of input signal for the time Command Input is high and replicate the same sample at the output. And when the command input is LOW, it keeps the last voltage level of sampled signal.




## Working of Sample and Hold Circuit

As you can in the circuit diagram, we have used 2N4339 N-channel JFET, an op-amp, and a capacitor. A command input (a PWM input) is connected to the Gate terminal of the 2N4339 transistor. As you can in the circuit diagram, we have used 2N4339 N-channel JFET, an op-amp, and a capacitor. A command input (a PWM input) is connected to the Gate terminal of the 2N4339 transistor. A diode 1N4007 is also connected between command input and 2N4339 N-channel JFET.

Now, the question is why the diode is connected in reverse condition? Let me give you a brief introduction about 2N4339. 2N4339 is an N-channel JFET with low noise and high gain. 2N4339 conducts (turn ON) only when gate-to-source voltage is in range of -0.3v to -50v (max). Now, we have set the initial voltage of command input to -15V and pulsed voltage to 15V. So, whenever the command input voltage is negative the diode will be forward biased which cause the transistor to turns ON and vice versa.

The Op-amp 741 is used as a voltage follower here, because voltage follower generally has a high input impedance and a low output impedance. This is used when the input signal is of low current becuase voltage follower can supply sufficient current to the next stage.

So, whenever the command input is HIGH the transistor works as closed switch and at this moment the capacitor starts charging to its peak value and stores the sample of input signal for the time transistor is in on state. Now when the command input is LOW the transistor works as open switch and the capacitor will experience high impedance and due to this it cannot get discharged and holds the charge for a particular period of time. This time is known as **Holding Period**. And, the time during which the circuit samples the input signal is called as the **Sampling Period**.

### Some Applications of Sample and Hold Circuit

- ADCs (Analog-to-Digital Conversion)
- DACs (Digital-to-Analog Conversion)
- In Analog Demultiplexing
- In Linear Systems

**Video Content / Details of website for further learning (if any):**

https://nptel.ac.in/courses/108108111/

**Important Books/Journals for further learning including the page nos.:**


- D.Roy Choudhary, Sheil B.Jani, "Linear Integrated Circuits", II edition, New Age, pp. 193-196, 2015


**Course Faculty**

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## LECTURE HANDOUTS

**EEE**

**II/III**

**Course Name with Code** :**19EEC03 / Linear Integrated Circuits**

**Course Faculty** : **Mr.R.Suresh**

**Unit** :**IV- D/A & A/D Convertors and Phase Locked Loop** **Date of Lecture:**

**Topic of Lecture:** Voltage Controlled Oscillator

**Introduction :**

A **voltage-controlled oscillator** (**VCO**) is an electronic **oscillator** whose **oscillation** frequency is **controlled** by a **voltage** input. The applied input **voltage** determines the instantaneous **oscillation** frequency.

**Prerequisite knowledge for Complete understanding and learning of Topic:**

Electronic Devices

**Detailed content of the Lecture:**

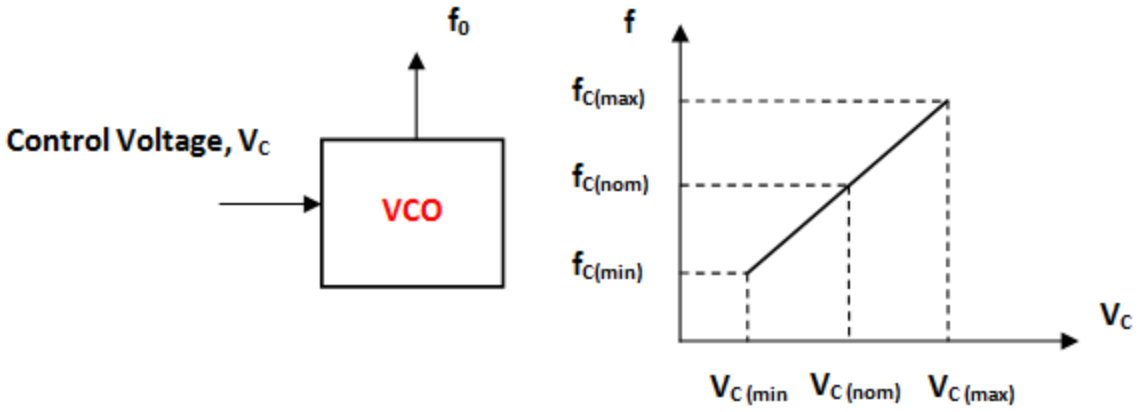
***Voltage controlled oscillator*** (VCO), from the name itself it is clear that the output instantaneous frequency of the oscillator is controlled by the input voltage. It is a kind of oscillator which can produce output signal frequency over a large range (few Hertz-hundreds of Giga Hertz) depending on the input DC voltage given to it.

## Frequency Control in Voltage Controlled Oscillator

Many forms of **VCO**s are generally used. It can be of RC oscillator or multi vibrator type or LC or crystal oscillator type. However; if it is of RC oscillator type, the oscillation frequency of output signal will be in inversely proportional to capacitance as

$$f = \frac{1}{(2\pi RC)}$$

In the case of LC oscillator, the oscillation frequency of output signal will be So, we can say that as the input voltage or control voltage increases, the capacitance get reduced. Hence, the control voltage and frequency of oscillations are directly proportional. That is, when one increases, the other will increase.




The figure above represents the basic working of **voltage controlled oscillator**. Here, we can see that at nominal control voltage represented by $V_{C(nom)}$, the oscillator works at its free running or normal frequency, $f_{C(nom)}$. As the control voltage decreases from nominal voltage, the frequency also decreases and as the nominal control voltage increases, the frequency also gets higher. The varactors diodes which are variable capacitance diodes (available in different capacitance range) are implemented for getting this variable voltage. For low frequency oscillators, the charging rate of capacitors is altered using voltage controlled current source to get the variable voltage.

## Types of Voltage Controlled Oscillator

The VCOs can be categorized based on the output waveform:

- Harmonic Oscillators
- Relaxation Oscillators

The output waveform produced by harmonic oscillators is sinusoidal. This can often referred as linear **voltage controlled oscillator**. The examples are LC and Crystal oscillators. Here, the capacitance of the varactor diode is varied by the voltage which is across the diode. This in turns alters the capacitance of the LC circuit. Hence, the output frequency will change. Advantages are frequency stability with reference to power supply, noise and temperature, Accuracy in control of frequency. The main drawback is this type of oscillators cannot be implemented effortlessly on monolithic ICs.

### Relaxation Oscillators

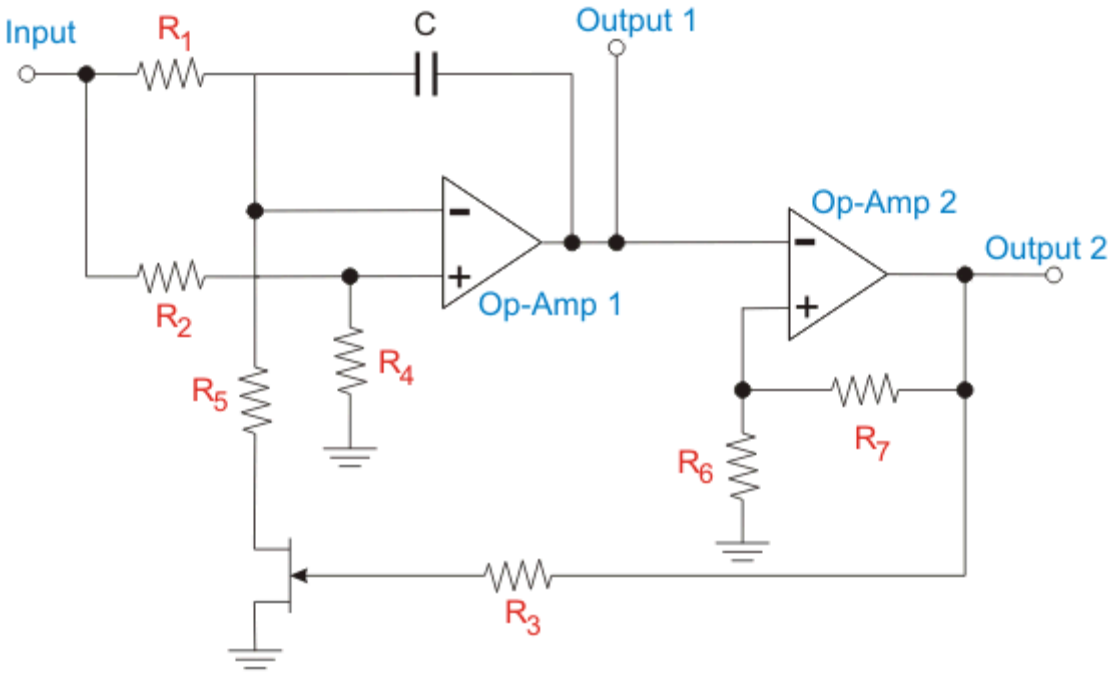
The output waveform produced by harmonic oscillators is saw tooth. This type can give a large range of frequency using reduced quantity of components. Mainly it can be used in monolithic ICs. The relaxation oscillators can possess the following topologies:

- Delay-based ring VCOs
- Grounded capacitor VCOs
- Emitter-Coupled VCOs

Here; in delay-based ring VCOs, the gain stages are attached together in a ring form. As the name implies, the frequency is related to the delay in every single stage. The second and third type VCOs works almost similarly. The time period taken in each stage is directly related to the charging and discharging time of capacitor.

## Working Principle of Voltage Controlled Oscillator (VCO)

**VCO** circuits can be designed by means of many voltage control electronic components such as varactor diodes, transistors, Op-amps etc. Here, we are going to discuss about the working of a VCO using Op-amps. The circuit diagram is shown below.




The output waveform of this VCO will be square wave. As we know the output frequency is related to the control voltage. In this circuit the first Op-amp will function as an integrator. The voltage divider arrangement is implemented here. Because of this, the half of the control voltage that is given as input is given to the positive terminal of the Op-amp 1. The same level of voltage is maintained at the negative terminal. This is to sustain the voltage drop across the resistor, $R_1$ as half of the control voltage.

When the MOSFET is in on condition, the current flowing from the $R_1$ resistor passes through the MOSFET. The $R_2$ have half the resistance, same voltage drop and twice the current as that of $R_1$. So, the extra current charges the connected capacitor. The Op-amp 1 should provide a gradually increasing output voltage to supply this current.

When the MOSFET is in off condition, the current flowing from the $R_1$resistor passes through the capacitor, get discharged. The output voltage obtained from the Op-amp 1 at this time will be falling. As a result, a triangular waveform is generated as the output of Op-amp 1. The Op-amp 2 will operate as Schmitt trigger. The input to this Op-amp is triangular wave which is the output of the Op-amp 1. If the input voltage is higher than the threshold level, the output from the Op-amp 2 will be $V_{CC}$. If the input voltage is less than the threshold level, the output from the Op-amp 2 will be zero. Therefore, the output of the Op-amp 2 will be square wave.

**Video Content / Details of website for further learning (if any):**

https://nptel.ac.in/courses/108108111/

**Important Books/Journals for further learning including the page nos.:**


- D.RoyChoudhary, SheilB.Jani, "Linear Integrated Circuits", II edition, New Age, pp. 195-197, 2015


**Course Faculty**

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Rasipuram - 637 408, Namakkal Dist., Tamil Nadu

Estd. 2000


**L33**

## LECTURE HANDOUTS

**EEE**

**II/III**

**Course Name with Code** :**19EEC03 / Linear Integrated Circuits**

**Course Faculty** : **Mr.R.Suresh**

**Unit** :**IV- D/A & A/D Convertors and Phase Locked Loop** **Date of Lecture:**

**Topic of Lecture:** Phase Locked Loop

**Introduction :**

A *phase-locked loop* or *phase lock loop* (*PLL*) is a control system that generates an output signal whose *phase* is related to the *phase* of an input signal. There are several different types; the simplest is an electronic circuit consisting of a variable frequency oscillator and a *phase* detector in a feedback *loop*

**Prerequisite knowledge for Complete understanding and learning of Topic:**

Electronic Devices

**Detailed content of the Lecture:**

The phase locked loop or PLL is a particularly useful circuit block that is widely used in radio frequency or wireless applications.

In view of its usefulness, the phase locked loop or PLL is found in many wireless, radio, and general electronic items from mobile phones to broadcast radios, televisions to Wi-Fi routers, walkie talkie radios to professional communications systems and vey much more.

## Phase locked loop, PLL applications

The phase locked loop take in a signal to which it locks and can then output this signal from its own internal VCO. At first sight this may not appear particularly useful, but with a little ingenuity, it is possible to develop a large number of phase locked loop applications.

Some phase lock loop applications include:

- ***FM demodulation:*** One major phase locked loop application is that of a FM demodulator. With PLL chips now relatively cheap, this PLL applications enables high quality audio to be demodulated from an FM signal.
- ***AM demodulation:*** Phase locked loops can be used in the synchronous demodulation of amplitude modulated signals. Using this approach, the PLL locks onto the carrier so that a reference within the receiver can be generated. As this corresponds exactly to the frequency of the carrier, it can be mixer with the incoming signal to synchronous demodulate the AM.
- ***Indirect frequency synthesizers:*** Use within a frequency synthesizer is one of the most important phase locked loop applications. Although direct digital synthesis is also used, indirect

frequency synthesis forms one of the major phase locked loop applications.

- ***Signal recovery:*** The fact that the phase locked loop is able to lock to a signal enables it to provide a clean signal, and remember the signal frequency if there is a short interruption. This phase locked loop application is used in a number of areas where signals may be interrupted for short periods of time, for example when using pulsed transmissions.
- ***Timing distribution:*** Another phase locked loop application is in the distribution precisely timed clock pulses in digital logic circuits and system, for example within a microprocessor system.

The linear plot can also be represented in the form of a circle. The beginning of the cycle can be represented as a particular point on the circle and as a time progresses the point on the waveform moves around the circle. Thus a complete cycle is equivalent to 360° or 2π radians. The instantaneous position on the circle represents the phase at that given moment relative to the beginning of the cycle.

Phase angle of points on a sine wave

The concept of phase difference takes this concept a little further. Although the two signals we looked at before have the same frequency, the peaks and troughs do not occur in the same place.

There is said to be a phase difference between the two signals. This phase difference is measured as the angle between them. It can be seen that it is the angle between the same point on the two waveforms. In this case a zero crossing point has been taken, but any point will suffice provided that it is the same on both.

This phase difference can also be represented on a circle because the two waveforms will be at different points on the cycle as a result of their phase difference. The phase difference measured as an angle: it is the angle between the two lines from the centre of the circle to the point where the waveform is represented.

Phase difference between signals

When there two signals have different frequencies it is found that the phase difference between the two signals is always varying. The reason for this is that the time for each cycle is different and accordingly they are moving around the circle at different rates.

It can be inferred from this that the definition of two signals having exactly the same frequency is that the phase difference between them is constant. There may be a phase difference between the two signals. This only means that they do not reach the same point on the waveform at the same time. If the phase difference is fixed it means that one is lagging behind or leading the other signal by the same amount, i.e. they are on the same frequency.

## Phase locked loop basics

A phase locked loop, PLL, is basically of form of servo loop. Although a PLL performs its actions on a radio frequency signal, all the basic criteria for loop stability and other parameters are the same. In this way the same theory can be applied to a phase locked loop as is applied to servo loops.

Basic phase locked loop basic diagram

A basic phase locked loop, PLL, consists of three basic elements:

- ***Phase comparator / detector:*** As the name implies, this circuit block within the PLL compares the phase of two signals and generates a voltage according to the phase difference between the two signals. This circuit can take a variety of forms. . . . . *Read more about the* ***phase detector*** ;

- ***Voltage controlled oscillator, VCO:*** The voltage controlled oscillator is the circuit block that generates the radio frequency signal that is normally considered as the output of the loop. Its frequency can be controlled over the operational frequency band required for the loop. . . . . *Read more about the* ***voltage controlled oscillator, VCO.***
- ***Loop filter:*** This filter is used to filter the output from the phase comparator in the phase locked loop, PLL. It is used to remove any components of the signals of which the phase is being compared from the VCO line, i.e. the reference and VCO input. It also governs many of the characteristics of the loop including the loop stability, speed of lock, etc. . . . . *Read more about the* ***PLL loop filter.***

**Video Content / Details of website for further learning (if any):**

https://nptel.ac.in/courses/108108111/

**Important Books/Journals for further learning including the page nos.:**

- D.Roy Choudhary, Sheil B.Jani, "Linear Integrated Circuits", II edition, New Age, pp. 201-205, 2015

**Course Faculty**

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**L34**

## LECTURE HANDOUTS

**EEE**

**II/III**

**Course Name with Code** :**19EEC03 / Linear Integrated Circuits**

**Course Faculty** : **Mr.R.Suresh**

**Unit** :**IV- D/A & A/D Convertors and Phase Locked Loop** **Date of Lecture:**

**Topic of Lecture:** Operating Principles

**Introduction :** A *phase-locked loop* or *phase lock loop* (*PLL*) is a control system that generates an output signal whose *phase* is related to the *phase* of an input signal. There are several different types; the simplest is an electronic circuit consisting of a variable frequency oscillator and a *phase* detector in a feedback *loop*.

**Prerequisite knowledge for Complete understanding and learning of Topic:**
Electronic Devices

**Detailed content of the Lecture:**

### Phase locked loop operation

The basic concept of the operation of the PLL is relatively simple, although the mathematical analysis and many elements of its operation are quite complicated

The diagram for a basic phase locked loop shows the three main element of the PLL: phase detector, voltage controlled oscillator and the loop filter.

In the basic PLL, reference signal and the signal from the voltage controlled oscillator are connected to the two input ports of the phase detector. The output from the phase detector is passed to the loop filter and then filtered signal is applied to the voltage controlled oscillator.

Phase locked loop diagram showing voltages

The Voltage Controlled Oscillator, VCO, within the PLL produces a signal which enters the phase detector. Here the phase of the signals from the VCO and the incoming reference signal are compared and a resulting difference or error voltage is produced. This corresponds to the phase difference between the two signals.

The error signal from the phase detector passes through a low pass filter which governs many of the properties of the loop and removes any high frequency elements on the signal. Once through the filter the error signal is applied to the control terminal of the VCO as its tuning voltage. The sense of any change in this voltage is such that it tries to reduce the phase difference and hence the frequency between the two signals. Initially the loop will be out of lock, and the error voltage will pull the frequency of the VCO towards that of the reference, until it cannot reduce the error any further and the

loop is locked.

When the PLL, phase locked loop, is in lock a steady state error voltage is produced. By using an amplifier between the phase detector and the VCO, the actual error between the signals can be reduced to very small levels. However some voltage must always be present at the control terminal of the VCO as this is what puts onto the correct frequency.

The fact that a steady error voltage is present means that the phase difference between the reference signal and the VCO is not changing. As the phase between these two signals is not changing means that the two signals are on exactly the same frequency.

The phase locked loop, PLL is a very useful building block, particularly for radio frequency applications. The PLL forms the basis of a number of RF systems including the indirect frequency synthesizer, a form of FM demodulator and it enables the recovery of a stable continuous carrier from a pulse waveform. In this way, the phase locked loop, PLL is an essential RF building tool.

## Phase Detector: digital, linear, mixer . .

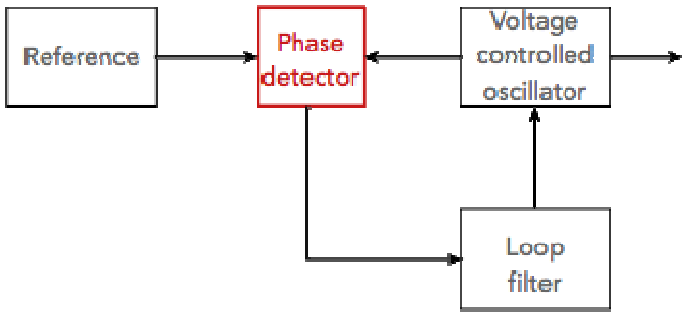
The phase detector is a key element of a phase locked loop and many other circuits. There are several types ranging from digital to analogue mixer and more.

The phase sensitive detector can be used in a number of circuits – anywhere that it is necessary to detect the phase between two signals. One of the main areas where phase detectors are used is within phase locked loops, although this is by no means the only one. The phase detector enables phase differences to be detected and the resultant "error" voltage to be produced.

There are different types of phase detector. They can be categorised in a variety of ways, but one is given below:

- Phase only sensitive detectors
- Phase / frequency detectors

Phase sensitive and phase-frequency detectors can be used in different ways and they are therefore described separately.




## Phase only sensitive detectors

Phase detectors that are only sensitive to phase are the most straightforward form of phase detector. As the name indicates their output is only dependent upon the phase difference between the two signals. When the phase difference between the two incoming signals is steady, they produce a constant voltage. When there is a frequency difference between the two signals, they produce a varying voltage at a frequency equal to the frequency difference.

The difference frequency product is the one used to give the phase difference.

However it is quite possible that the difference frequency signal will fall outside the pass-band of the loop filter, and hence the overall phase locked loop. If this occurs then no error voltage pass through the PLL loop filter and on to the Voltage Controlled Oscillator, VCO, to bring it into lock. This means that there only is a limited range over which the phase locked loop can be brought into lock. This range is called the capture range. Once in lock the loop can generally be pulled over a much wider frequency band.

Apart from using a phase frequency detector, there are several ways in which this problem can be overcome. The oscillator must be steered close to the reference oscillator frequency. This can be achieved in a number of ways. One is to reduce the tuning range of the oscillator so that the difference product will always fall within the pass-band of the loop filter. In other instances another tune voltage can be combined with the feedback from the loop to ensure that the oscillator is in the correct region. This is approach is often adopted in microprocessor systems where the correct voltage can be calculated for any given circumstance.

**Video Content / Details of website for further learning (if any):**

https://nptel.ac.in/courses/108108111/

**Important Books/Journals for further learning including the page nos.:**


- D.Roy Choudhary, Sheil B.Jani, “Linear Integrated Circuits”, II edition, New Age, pp. 217-225 2015


**Course Faculty**

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**L35**

## LECTURE HANDOUTS

**EEE**

**II/III**

**Course Name with Code** :**19EEC03 / Linear Integrated Circuits**

**Course Faculty** : **Mr.R.Suresh**

**Unit** :**IV- D/A & A/D Convertors and Phase Locked Loop** **Date of Lecture:**

**Topic of Lecture:** Applications of PLL

**Introduction :**

**Applications of Phase-Locked Loop**

- **FM demodulation** networks for FM operations.
- It is used in motor speed controls and tracking filters.
- It is used in frequency shifting decodes for **demodulation** carrier frequencies.
- It is used in time to digital converters.
- It is used for Jitter reduction, skew suppression, clock recovery.

**Prerequisite knowledge for Complete understanding and learning of Topic:**

Electronic Devices

**Detailed content of the Lecture:**

The phase locked loop or PLL is a particularly useful circuit block that is widely used in radio frequency or wireless applications.

In view of its usefulness, the phase locked loop or PLL is found in many wireless, radio, and general electronic items from mobile phones to broadcast radios, televisions to Wi-Fi routers, walkie talkie radios to professional communications systems and vey much more.

## Phase locked loop, PLL applications

The phase locked loop take in a signal to which it locks and can then output this signal from its own internal VCO. At first sight this may not appear particularly useful, but with a little ingenuity, it is possible to develop a large number of phase locked loop applications.

Some phase lock loop applications include:

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- ***AM demodulation:*** Phase locked loops can be used in the synchronous demodulation of amplitude modulated signals. Using this approach, the PLL locks onto the carrier so that a

reference within the receiver can be generated. As this corresponds exactly to the frequency of the carrier, it can be mixer with the incoming signal to synchronous demodulate the AM.

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**Important Books/Journals for further learning including the page nos.:**


- D.RoyChoudhary, SheilB.Jani, "Linear Integrated Circuits", II edition, New Age, pp. 107-125, 2015


**Course Faculty**

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**L36**

## LECTURE HANDOUTS

**EEE**

**II/III**

**Course Name with Code** :19EEC03 / Linear Integrated Circuits

**Course Faculty** : Mr.R.Suresh

**Unit** :IV- D/A & A/D Convertors and Phase Locked Loop **Date of Lecture:**

**Topic of Lecture: Applications of PLL**

**Introduction :**

**Applications of Phase-Locked Loop**

- **FM demodulation** networks for FM operations.
- It is used in motor speed controls and tracking filters.
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- It is used for Jitter reduction, skew suppression, clock recovery.

**Prerequisite knowledge for Complete understanding and learning of Topic:**

Electronic Devices

**Detailed content of the Lecture:**

## Phase locked loop basic concepts - phase

The key to the operation of a phase locked loop, PLL, is the phase difference between two signals, and the ability to detect it. The information about the error in phase or the phase difference between the two signals is then used to control the frequency of the loop.

To understand more about the concept of phase and phase difference, it is possible to visualise two waveforms, normally seen as sine waves, as they might appear on an oscilloscope. If the trigger is fired at the same time for both signals they will appear at different points on the screen.

The linear plot can also be represented in the form of a circle. The beginning of the cycle can be represented as a particular point on the circle and as a time progresses the point on the waveform moves around the circle. Thus a complete cycle is equivalent to 360° or 2π radians. The instantaneous position on the circle represents the phase at that given moment relative to the beginning of the cycle.

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**Video Content / Details of website for further learning (if any):**

https://nptel.ac.in/courses/108108111/

**Important Books/Journals for further learning including the page nos.:**

- D.RoyChoudhary, SheilB.Jani, "Linear Integrated Circuits", II edition, New Age, pp. 107-125, 2015

**Course Faculty**

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**L37**

## LECTURE HANDOUTS

**EEE**

**II/III**

**Course Name with Code** :**19EEC03 / Linear Integrated Circuits**

**Course Faculty** : **Mr.R.Suresh**

**Unit** :**V- Special ICs** **Date of Lecture:**

**Topic of Lecture:** IC555 Timer

**Introduction :**

**Special Function ICs**

Browse Circuit Specialists' sweeping selection of quality integrated circuits (ICs) made by Sprague and Exar, two of the top producers of microchips. Used in virtually all electronic equipment today, ICs have revolutionized the realm of electronics. ICs are remarkably compact — having literally up to several billion transistors and other electronic components in an area about the size of your fingernail — and are significantly smaller than discrete circuits made from independent components.

**Prerequisite knowledge for Complete understanding and learning of Topic:**

Electronic Devices

**Detailed content of the Lecture:**

Manufacturers have also developed special-purpose ICs that handle tasks needed to implement both closed-loop motion control and motor speed control. Presently, three chips are available for closed-loop control, one for multiaxis contouring, and a few others for motor speed control.

A general-purpose motion-control IC called the HCTL-1000 is aimed at dc, brushless dc, and stepper motors. The TTL-compatible chip is powered by a single 5-V power supply. Position and velocity control are provided by comparing the host computer-command signal with feedback data from an incremental encoder. The encoder feedback is decoded into quadrature counts and a 24-bit counter keeps track of position. As a result, neither analog compensation nor velocity feedback is necessary.

On-chip software allows a choice of four control modes: position control, proportional velocity control, trapezoidal profiling, and integral velocity control.

In the position-control mode, the motor moves from one point to another without velocity profiling. Proportional velocity control regulates motor speed using only gain for compensation. Dynamic pole and zero-lead compensation is not used. Actual motor velocity is compared to the specified velocity, and the error calculated.

The trapezoidal mode is used for point-to-point control with velocity control. The final position, acceleration, and maximum velocity are specified. The controller then computes the signal profile needed to conform to these requirements. Motor velocity is monitored during the position change. If maximum velocity is reached before the motor moves half way to the target position, the velocity

versus time waveform is trapezoidal. Otherwise it is triangular.

Continuous velocity control is provided by the integral velocity control mode. Here, velocity and acceleration can be changed at any time to profile velocity in time. Once the specified velocity is reached, it is maintained until the command is changed.

Another closed-loop controller, called the GL-1200, produces precise motor control using an external 10-MHz clock which times the circuit output. The chip compares signals generated by a two-channel incremental encoder with the specified position to generate a 12-bit error signal. The error signal provides motor position control. An interesting feature of the GL-1200 is that it calculates the derivative of the position error, and uses that value for system damping. Because the derivative is proportional to velocity, the need for velocity feedback from a tachometer is eliminated.

Recently developed servocontrol chips, called the LM628 and LM629, contain PID filtering functions. Filter constants can be changed on commands from a microprocessor during a move.

The host programs required velocity, acceleration, and position. The host can also program the coefficients of the digital filter used to provide gain, and compensate for following error and motor time constants. The host can interrogate the chip and read the position register and obtain other status information. The servo IC can interrupt the host in the event of critical situations as well, such as if position error exceeds certain bounds (as might occur if the motor stalls, for example).

During a move, a profile generator on the servo chip sends a position signal to a digital summing node. The required position is compared once per sample interval to the actual motor position. The resulting error signal goes through filtering before being sent to the digital/analog converter.

Several years ago, two chips were developed specifically to control simultaneous movement along two axes. There are two basic problems that these chips are designed to solve. To illustrate, consider a milling machine that is to make a 45° cut, relative to the *X* and *Y* axis. Unless the motors driving the mill table finish at exactly the same time, the cut will not be a straight line. Instead, it might have a slight curve or actually resemble a staircase.

The other difficulty has to do with maintaining constant cutting-head speed. Actual cutting speed depends on the velocity in both the *X* and *Y* directions. In the example, if the cutting speed is specified as 10 ipm, and the head is moved in the *X* and *Y* directions at this speed, the actual speed would be 14.14 ipm.

The two chips, the KM3701 and KM3702, both are CMOS devices and can be obtained on PC-compatible plug-in boards as well as separately. The KM3701 microcontroller generates interpolation pulses for the *X* and *Y* axis. The information used to calculate the interpolation pulses is received from an external processor. These pulses can be used to control stepping motors in open-loop systems, or the KM3702 in closed-loop designs. The KM3702 is a motion-control chip that generates an output signal proportional to the difference between the specified position and the actual position.

Interpolation pulses are calculated from an algorithm stored on the chip. A feature that differentiates the KM3701 from other interpolation chips is its capacity to generate pulses for parabolic, logarithmic, and exponential functions. This feature allows it to closely approximate complex curves such as those in a wing spar, for example.

Several firms have developed chips for speed control. An example is the LS7263. Intended for speed regulation of three-phase, brushless dc motors, the circuit uses a 3.58-MHz crystal time base to produce ± 0.1% speed control. Speed corrections are made by measuring the tachometer input and varying each winding's drive signal. The chip provides positive braking by shorting the windings together. This places an electrical load on the motor and slows it down.

Overcurrent protection for the windings, drivers, and power supply is provided. This protection circuit uses a fractional-value resistor, connected between the positive supply and the driver's emitters.

| |
|---|
| A potentiometer is connected between the driver and ground, with the wiper wired to the IC's overcurrent input. The wiper tailors the activation current for a particular motor. |
| **Video Content / Details of website for further learning (if any):**<br><br>https://nptel.ac.in/courses/108108111/ |
| **Important Books/Journals for further learning including the page nos.:**<br>• D.RoyChoudhary, SheilB.Jani, "Linear Integrated Circuits", II edition, New Age, pp. 255-257, 2015 |

**Course Faculty**

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L38

## LECTURE HANDOUTS

**EEE**

**II/III**

**Course Name with Code** :**19EEC03 / Linear Integrated Circuits**

**Course Faculty** : **Mr.R.Suresh**

**Unit** :**V- Special ICs** **Date of Lecture:**

**Topic of Lecture:** IC555 Timer

**Introduction :** ne such device that has been around since the early days of IC's and has itself become something of an industry "standard" is the **555 Timer Oscillator** which is more commonly called the **"555 Timer"**.

**Prerequisite knowledge for Complete understanding and learning of Topic:**
Electronic Devices

**Detailed content of the Lecture:**

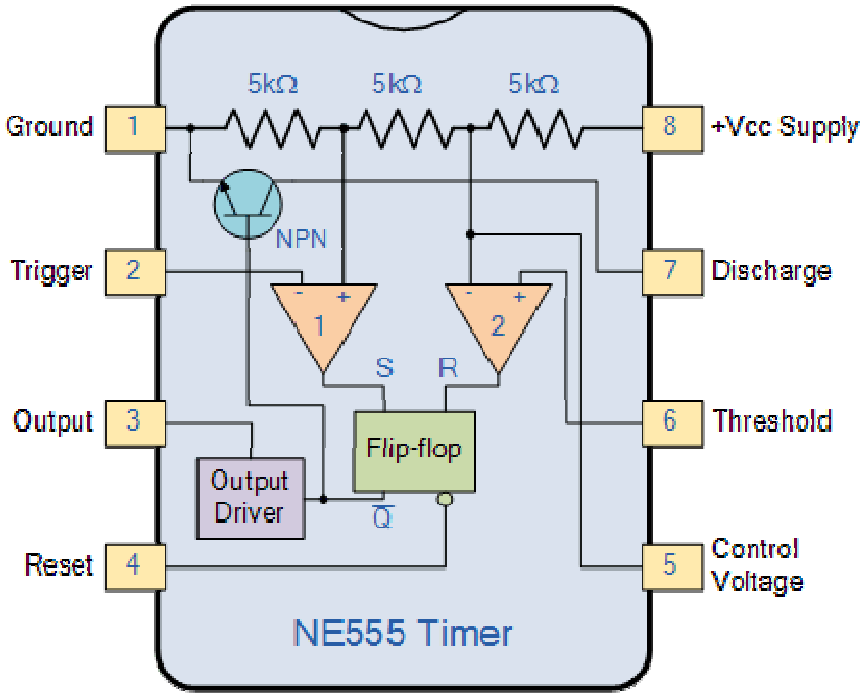
The basic **555 timer** gets its name from the fact that there are three internally connected 5kΩ resistors which it uses to generate the two comparators reference voltages. The 555 timer IC is a very cheap, popular and useful precision timing device which can act as either a simple timer to generate single pulses or long time delays, or as a relaxation oscillator producing a string of stabilised waveforms of varying duty cycles from 50 to 100%.

The 555 timer chip is extremely robust and stable 8-pin device that can be operated either as a very accurate Monostable, Bistable or AstableMultivibrator to produce a variety of applications such as one-shot or delay timers, pulse generation, LED and lamp flashers, alarms and tone generation, logic clocks, frequency division, power supplies and converters etc, in fact any circuit that requires some form of time control as the list is endless.

The single 555 Timer chip in its basic form is a Bipolar 8-pin mini Dual-in-line Package (DIP) device consisting of some 25 transistors, 2 diodes and about 16 resistors arranged to form two comparators, a flip-flop and a high current output stage as shown below. As well as the 555 Timer there is also available the NE556 Timer Oscillator which combines TWO individual 555's within a single 14-pin DIP package and low power CMOS versions of the single 555 timer such as the 7555 and LMC555 which use MOSFET transistors instead.

A simplified "block diagram" representing the internal circuitry of the **555 timer** is given below with a brief explanation of each of its connecting pins to help provide a clearer understanding of how it works.

## 555 Timer Block Diagram




- • Pin 1. –**Ground**, The ground pin connects the 555 timer to the negative (0v) supply rail.
- • Pin 2. –**Trigger**, The negative input to comparator No 1. A negative pulse on this pin "sets" the internal Flip-flop when the voltage drops below 1/3Vcc causing the output to switch from a "LOW" to a "HIGH" state.
- • Pin 3. –**Output**, The output pin can drive any TTL circuit and is capable of sourcing or sinking up to 200mA of current at an output voltage equal to approximately Vcc – 1.5V so small speakers, LEDs or motors can be connected directly to the output.
- • Pin 4. –**Reset**, This pin is used to "reset" the internal Flip-flop controlling the state of the output, pin 3. This is an active-low input and is generally connected to a logic "1" level when not used to prevent any unwanted resetting of the output.
- • Pin 5. –**Control Voltage**, This pin controls the timing of the 555 by overriding the 2/3Vcc level of the voltage divider network. By applying a voltage to this pin the width of the output signal can be varied independently of the RC timing network. When not used it is connected to ground via a 10nF capacitor to eliminate any noise.
- • Pin 6. –**Threshold**, The positive input to comparator No 2. This pin is used to reset the Flip-flop when the voltage applied to it exceeds 2/3Vcc causing the output to switch from "HIGH" to "LOW" state. This pin connects directly to the RC timing circuit.
- • Pin 7. –**Discharge**, The discharge pin is connected directly to the Collector of an internal NPN transistor which is used to "discharge" the timing capacitor to ground when the output at pin 3 switches "LOW".
- • Pin 8. –**Supply +Vcc**, This is the power supply pin and for general purpose TTL 555 timers is between 4.5V and 15V.

The **555 Timers** name comes from the fact that there are three 5kΩ resistors connected together internally producing a voltage divider network between the supply voltage at pin 8 and ground at pin 1. The voltage across this series resistive network holds the negative inverting input of comparator two at 2/3Vcc and the positive non-inverting input to comparator one at 1/3Vcc.

The two comparators produce an output voltage dependent upon the voltage difference at their inputs which is determined by the charging and discharging action of the externally connected RC

network. The outputs from both comparators are connected to the two inputs of the flip-flop which in turn produces either a “HIGH” or “LOW” level output at Q based on the states of its inputs. The output from the flip-flop is used to control a high current output switching stage to drive the connected load producing either a “HIGH” or “LOW” voltage level at the output pin.

The most common use of the 555 timer oscillator is as a simple astable oscillator by connecting two resistors and a capacitor across its terminals to generate a fixed pulse train with a time period determined by the time constant of the RC network. But the 555 timer oscillator chip can also be connected in a variety of different ways to produce Monostable or Bistablemultivibrators as well as the more common AstableMultivibrator.

**Video Content / Details of website for further learning (if any):**

https://nptel.ac.in/courses/108108111/

**Important Books/Journals for further learning including the page nos.:**


- D.RoyChoudhary, SheilB.Jani, “Linear Integrated Circuits”, II edition, New Age, pp. 257-261, 2015


**Course Faculty**

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**L39**

## LECTURE HANDOUTS

**EEE**

**II/III**

**Course Name with Code** :19EEC03 / Linear Integrated Circuits

**Course Faculty** : Mr.R.Suresh

**Unit** :V- Special ICs **Date of Lecture:**

**Topic of Lecture:** Monostable Modes of Operation

**Introduction :**

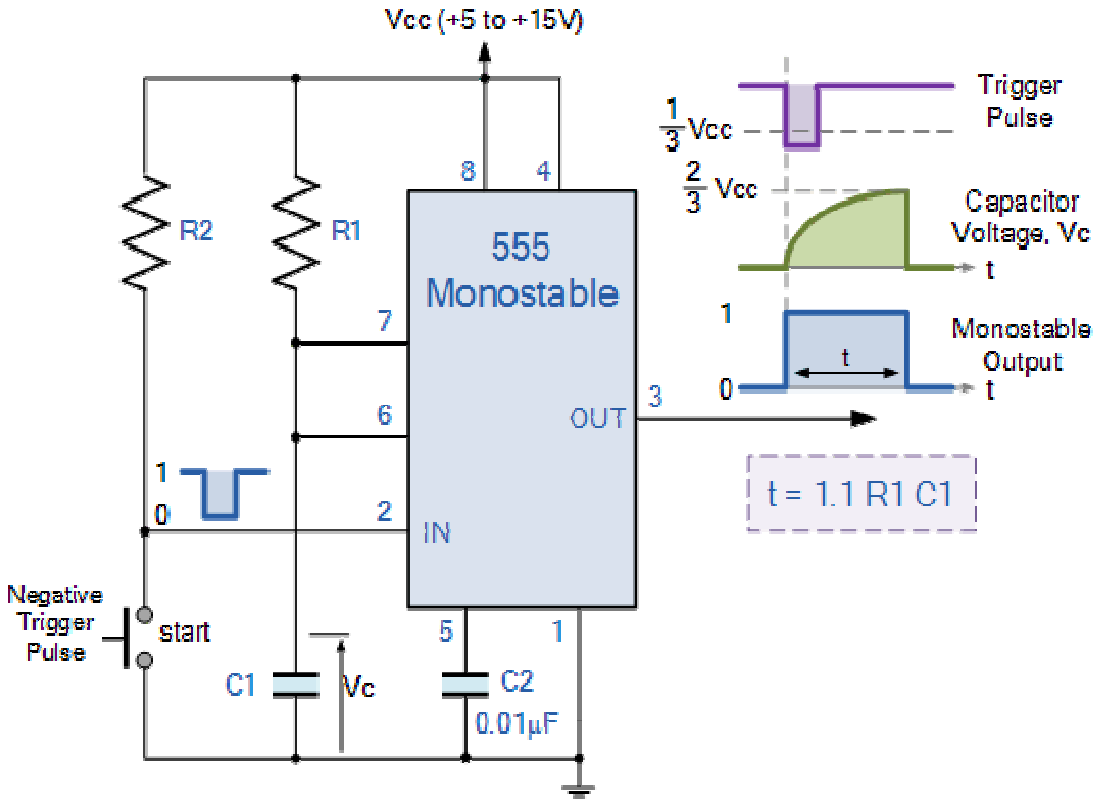
The operation and output of the **555 timer monostable** is exactly the same as that for the transistorised one we look at previously in the Monostable Multivibrators tutorial. The difference this time is that the two transistors have been replaced by the 555 timer device. Consider the 555 timer monostable circuit below.

**Prerequisite knowledge for Complete understanding and learning of Topic:**

Electronic Devices

**Detailed content of the Lecture:**

### Monostable 555 Timer



When a negative ( 0V ) pulse is applied to the trigger input (pin 2) of the Monostable configured 555 Timer oscillator, the internal comparator, (comparator No1) detects this input and "sets" the state of the flip-flop, changing the output from a "LOW" state to a "HIGH" state. This action in turn turns "OFF" the discharge transistor connected to pin 7, thereby removing the short circuit across the external timing capacitor, C1.

This action allows the timing capacitor to start to charge up through resistor, R1 until the voltage across the capacitor reaches the threshold (pin 6) voltage of 2/3Vcc set up by the internal voltage divider network. At this point the comparators output goes "HIGH" and "resets" the flip-flop back to its original state which in turn turns "ON" the transistor and discharges the capacitor to ground through pin 7. This causes the output to change its state back to the original stable "LOW" value awaiting another trigger pulse to start the timing process over again. Then as before, the Monostable Multivibrator has only "ONE" stable state.

The **Monostable 555 Timer** circuit triggers on a negative-going pulse applied to pin 2 and this trigger pulse must be much shorter than the output pulse width allowing time for the timing capacitor to charge and then discharge fully. Once triggered, the 555 Monostable will remain in this "HIGH" unstable output state until the time period set up by the $R_1$ x $C_1$ network has elapsed. The amount of time that the output voltage remains "HIGH" or at a logic "1" level, is given by the following time constant equation.

$$\tau = 1.1 R_1 C_1$$

Where, t is in seconds, R is in Ω and C in Farads.

**Video Content / Details of website for further learning (if any):**

https://nptel.ac.in/courses/108108111/

**Important Books/Journals for further learning including the page nos.:**


- D.Roy Choudhary, Sheil B.Jani, "Linear Integrated Circuits", II edition, New Age, pp. 172-175, 2015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## LECTURE HANDOUTS

**EEE**

**II/III**

**Course Name with Code** :**19EEC03 / Linear Integrated Circuits**

**Course Faculty** : **Mr.R.Suresh**

**Unit** :**V- Special ICs** **Date of Lecture:**

**Topic of Lecture:** Astable Modes of Operation

**Introduction :**

Regenerative switching circuits such as **Astable Multivibrators** are the most commonly used type of relaxation oscillator because not only are they simple, reliable and ease of construction they also produce a constant square wave output waveform.

**Prerequisite knowledge for Complete understanding and learning of Topic:**

Electronic Devices

**Detailed content of the Lecture:**

Unlike the Monostable Multivibrator or the Bistable Multivibrator we looked at in the previous tutorials that require an "external" trigger pulse for their operation, the **Astable Multivibrator** has automatic built in triggering which switches it continuously between its two unstable states both set and reset.

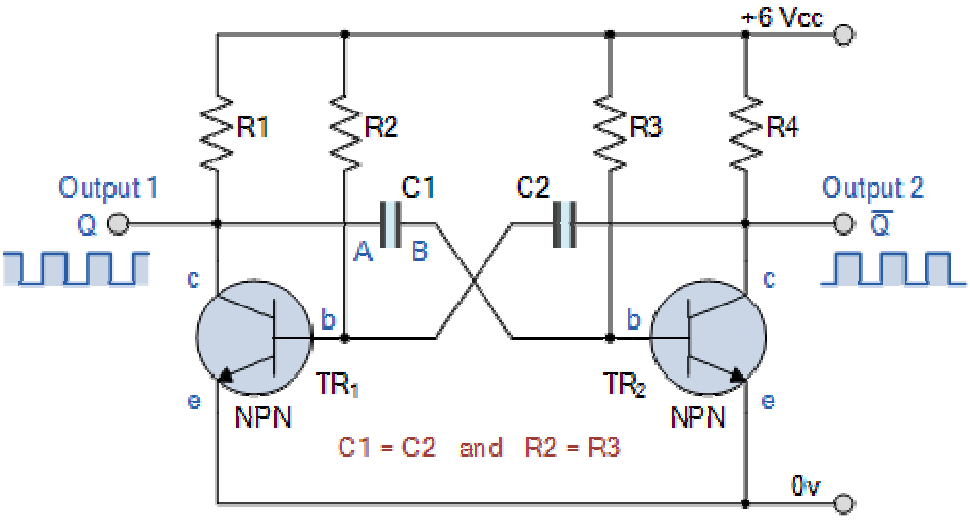
The **Astable Multivibrator** is another type of cross-coupled transistor switching circuit that has **NO** stable output states as it changes from one state to the other all the time. The astable circuit consists of two switching transistors, a cross-coupled feedback network, and two time delay capacitors which allows oscillation between the two states with no external triggering to produce the change in state.

In electronic circuits, astable multivibrators are also known as **Free-running Multivibrator** as they do not require any additional inputs or external assistance to oscillate. Astable oscillators produce a continuous square wave from its output or outputs, (two outputs no inputs) which can then be used to flash lights or produce a sound in a loudspeaker.

The basic transistor circuit for an **Astable Multivibrator** produces a square wave output from a pair of grounded emitter cross-coupled transistors. Both transistors either NPN or PNP, in the multivibrator are biased for linear operation and are operated as Common Emitter Amplifiers with 100% positive feedback.

This configuration satisfies the condition for oscillation when: ( $\beta A = 1\angle 0^o$ ). This results in one stage conducting "fully-ON" (Saturation) while the other is switched "fully-OFF" (cut-off) giving a very high level of mutual amplification between the two transistors. Conduction is transferred from one stage to the other by the discharging action of a capacitor through a resistor as shown below.

## Basic Astable Multivibrator Circuit




Assume a 6 volt supply and that transistor, $TR_1$ has just switched "OFF" (cut-off) and its collector voltage is rising towards Vcc, meanwhile transistor $TR_2$ has just turned "ON". Plate "A" of capacitor C1 is also rising towards the +6 volts supply rail of Vcc as it is connected to the collector of $TR_1$ which is now cut-off. Since $TR_1$ is in cut-off, it conducts no current so there is no volt drop across load resistor $R_1$.

The other side of capacitor, C1, plate "B", is connected to the base terminal of transistor $TR_2$ and at 0.6v because transistor $TR_2$ is conducting (saturation). Therefore, capacitor C1 has a potential difference of +5.4 volts across its plates, (6.0 – 0.6v) from point A to point B.

Since $TR_2$ is fully-on, capacitor $C_2$ starts to charge up through resistor $R_2$ towards Vcc. When the voltage across capacitor $C_2$ rises to more than 0.6v, it biases transistor $TR_1$ into conduction and into saturation.

The instant that transistor, $TR_1$ switches "ON", plate "A" of the capacitor which was originally at Vcc potential, immediately falls to 0.6 volts. This rapid fall of voltage on plate "A" causes an equal and instantaneous fall in voltage on plate "B" therefore plate "B" of C1 is pulled down to -5.4v (a reverse charge) and this negative voltage swing is applied the base of $TR_2$ turning it hard "OFF". One unstable state.

Transistor $TR_2$ is driven into cut-off so capacitor C1 now begins to charge in the opposite direction via resistor R3 which is also connected to the +6 volts supply rail, Vcc. Thus the base of transistor $TR_2$ is now moving upwards in a positive direction towards Vcc with a time constant equal to the C1 x R3 combination.

However, it never reaches the value of Vcc because as soon as it gets to 0.6 volts positive, transistor $TR_2$ turns fully "ON" into saturation. This action starts the whole process over again but now with capacitor C2 taking the base of transistor $TR_1$ to -5.4v while charging up via resistor R2 and entering the second unstable state.

Then we can see that the circuit alternates between one unstable state in which transistor $TR_1$ is "OFF" and transistor $TR_2$ is "ON", and a second unstable in which $TR_1$ is "ON" and $TR_2$ is "OFF" at a rate determined by the RC values. This process will repeat itself over and over again as long as the supply voltage is present.

The amplitude of the output waveform is approximately the same as the supply voltage, Vcc with the time period of each switching state determined by the time constant of the RC networks connected

across the base terminals of the transistors. As the transistors are switching both “ON” and “OFF”, the output at either collector will be a square wave with slightly rounded corners because of the current which charges the capacitors. This could be corrected by using more components as we will discuss later.

If the two time constants produced by C2 x R2 and C1 x R3 in the base circuits are the same, the mark-to-space ratio ( t1/t2 ) will be equal to one-to-one making the output waveform symmetrical in shape. By varying the capacitors, C1, C2 or the resistors, R2, R3 the mark-to-space ratio and therefore the frequency can be altered.

We saw in the RC Discharging tutorial that the time taken for the voltage across a capacitor to fall to half the supply voltage, 0.5Vcc is equal to 0.69 time constants of the capacitor and resistor combination. Then taking one side of the astable multivibrator, the length of time that transistor $TR_2$ is “OFF” will be equal to 0.69T or 0.69 times the time constant of C1 x R3. Likewise, the length of time that transistor $TR_1$ is “OFF” will be equal to 0.69T or 0.69 times the time constant of C2 x R2 and this is defined as.

**Video Content / Details of website for further learning (if any):**

https://nptel.ac.in/courses/108108111/

**Important Books/Journals for further learning including the page nos.:**


- D.Roy Choudhary, Sheil B.Jani, “Linear Integrated Circuits”, II edition, New Age, pp. 291-956, 2015


**Course Faculty**

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## LECTURE HANDOUTS

**EEE**

**II/III**

**Course Name with Code** :19EEC03 / Linear Integrated Circuits

**Course Faculty** : Mr.R.Suresh

**Unit** :V- Special ICs **Date of Lecture:**

**Topic of Lecture:** Voltage Regulators

**Introduction :**

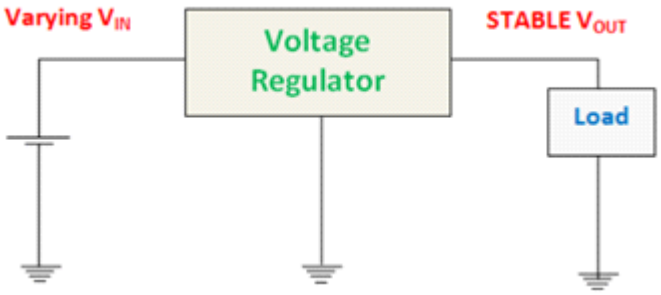
A **voltage regulator** is an electronic or electrical device that can sustain the voltage of power supply within suitable limits. The electrical equipment connected to the voltage source should bear the value of the voltage. The source voltage should be in a certain range which is acceptable for the connected pieces of equipment. This purpose is fulfilled by implementing a voltage regulator.

**Prerequisite knowledge for Complete understanding and learning of Topic:**

Electronic Devices

**Detailed content of the Lecture:**

A voltage regulator – as the same suggests – regulates the voltage, regardless of the adjustments in the input voltage or connected load. It works as a shield for protective devices from damage. It can regulate both AC or DC voltages, depending on its design.




## Types of Voltage Regulators

There are two main types of voltage regulators available:

- Linear Voltage Regulators
- Switching Voltage Regulators

These can be further classified into more specific voltage regulators, as discussed below.

### Linear Voltage Regulator

This type of voltage regulator performs as a voltage divider. It employs FET in Ohmic region. The steady output is sustained by varying the resistance of voltage regulator with respect to the load.

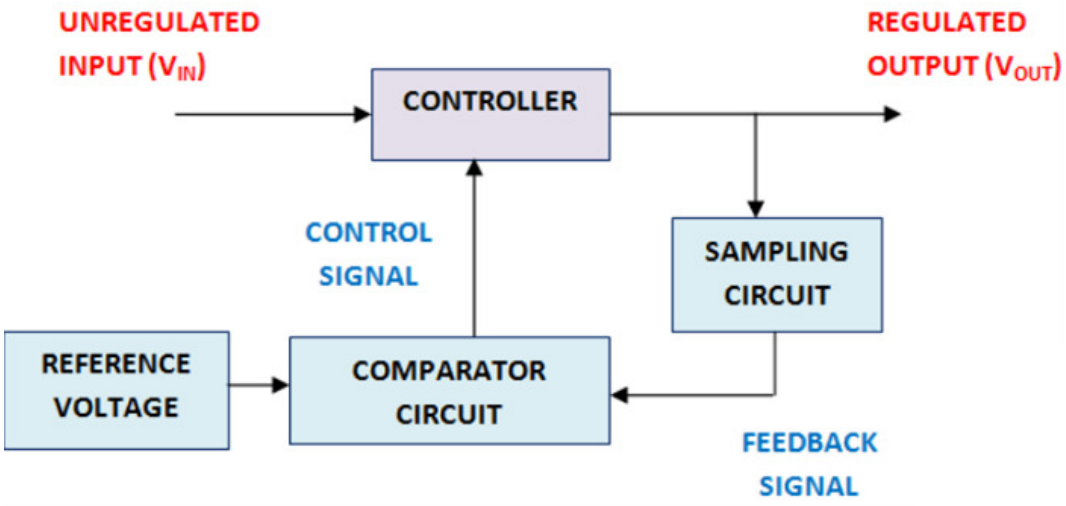
Generally, these types of voltage regulator are of two types:

- Series voltage regulator
- Shunt voltage regulator

It implements a variable element positioned in series with the connected load. The steady output is sustained by varying the resistance of this element with respect to the load. They are of two types that are briefed below.

## Discrete Transistor Series Voltage Regulator

Here from the block diagram, we can see an unregulated input is first fed into a controller. It actually controls the input voltage magnitude and given to the output. This output is given to the feedback circuit. It is sampled by the sampling circuit and given to the comparator. There it is compared by the reference voltage and given back to the output.

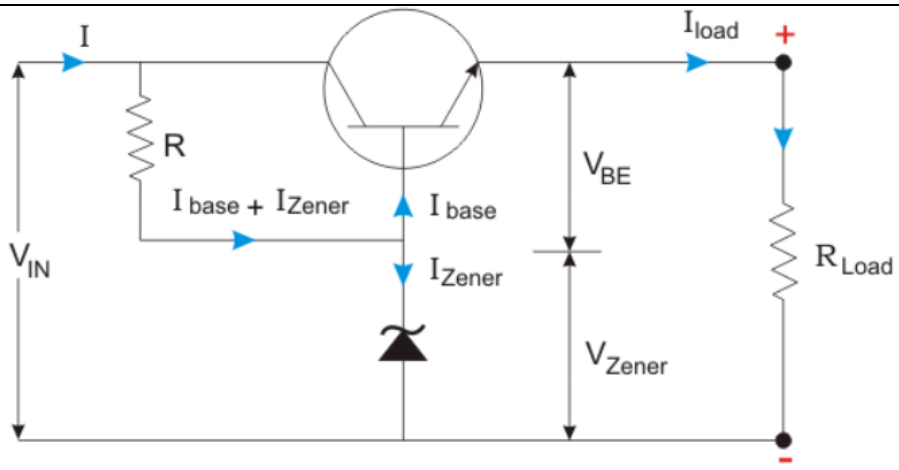



Here, the comparator circuit will give a control signal to the controller whenever there is an increase or decrease in the output voltage. Thus, the controller will reduce or increase the voltage to the acceptable range so that a sustained voltage will get as the output.

## Zener Diode as Voltage Regulator

When a Zener diode is used as a voltage regulator, it is known as a Zener controlled transistor series voltage regulator or an emitter follower voltage regulator. Here, the transistor used is emitter follower (see figure below). The emitter and the collector terminals of the series pass transistor used here are in series with respect to load. The variable element is a transistor and the Zener diode will supply the reference voltage.

$$V_{OUT} = V_{Zener} + V_{BE}$$




## Shunt Voltage Regulator

The **shunt voltage regulator** provides a way from the supply voltage reaching to the ground with the help of variable resistance. From the load, the current is shunted away from the load to the ground. We can simply say that this regulator can absorb current and it is less efficient compared to the series voltage regulator. The applications include error amplifiers, voltage monitoring, precision current limiters, etc. They are of two types that are briefed below.

### *Discrete Transistor Shunt Voltage Regulator*

Here, the current is shunted away from the load. The controller will shunt a portion of the total current that is developed by the unregulated input which is given to the load. The voltage regulation takes place across the load.

Here, the comparator circuit will give a control signal to the controller whenever there is an increase or decrease in the output voltage because of the variation in load. Thus, the controller will shunt the extra current from the load so as to get a sustained voltage as the output

**Video Content / Details of website for further learning (if any):**

https://nptel.ac.in/courses/108108111/

**Important Books/Journals for further learning including the page nos.:**

- D.Roy Choudhary, Sheil B.Jani, "Linear Integrated Circuits", II edition, New Age, pp. 307-309, 2015

**Course Faculty**

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**L42**

## LECTURE HANDOUTS

**EEE**

**II/III**

**Course Name with Code** :**19EEC03 / Linear Integrated Circuits**

**Course Faculty** : **Mr.R.Suresh**

**Unit** :**V- Special ICs** **Date of Lecture:**

**Topic of Lecture:** Fixed Voltage Regulators

**Introduction :**

The function of a **voltage regulator** is to maintain a constant DC voltage at the output irrespective of voltage fluctuations at the input and (or) variations in the load current. In other words, voltage regulator produces a regulated DC output voltage. Voltage regulators are also available in Integrated Circuits (IC) forms. These are called as **voltage regulator ICs**.

**Prerequisite knowledge for Complete understanding and learning of Topic:**

Electronic Devices

**Detailed content of the Lecture:**

## Types of Voltage Regulators

There are **two types** of voltage regulators –

- Fixed voltage regulator
- Adjustable voltage regulator

This chapter discusses about these two types of voltage regulators one by one.

### Fixed voltage regulator

A **fixed voltage regulator** produces a fixed DC output voltage, which is either positive or negative. In other words, some fixed voltage regulators produce positive fixed DC voltage values, while others produce negative fixed DC voltage values.

**78xx** voltage regulator ICs produce positive fixed DC voltage values, whereas, 79xx voltage regulator ICs produce negative fixed DC voltage values.

The following points are to be noted while working with **78xx** and **79xx** voltage regulator ICs –

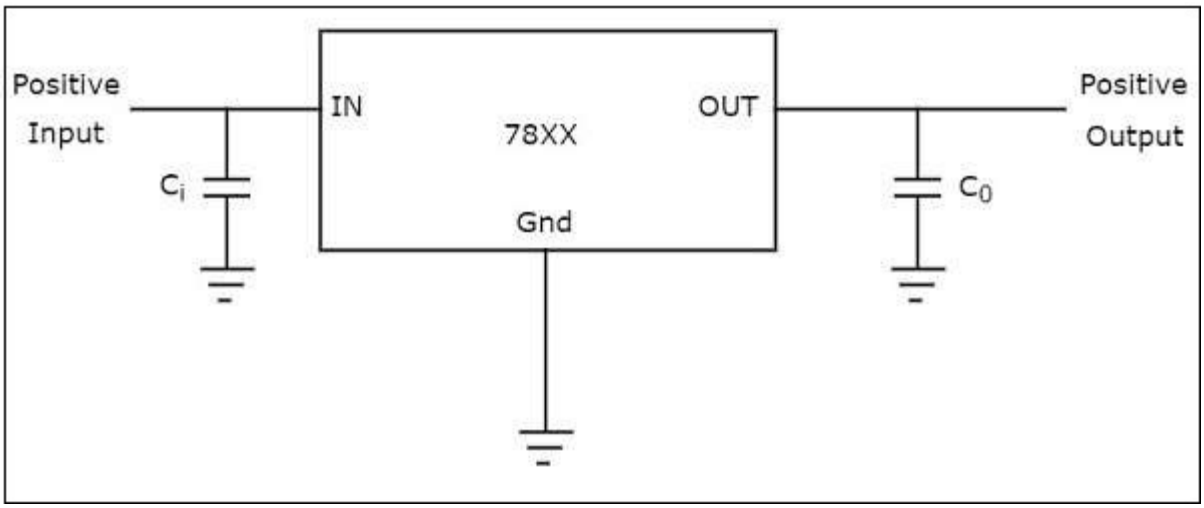
- "xx" corresponds to a two-digit number and represents the amount (magnitude) of voltage that voltage regulator IC produces.
- Both 78xx and 79xx voltage regulator ICs have **3 pins** each and the third pin is used for collecting the output from them.
- The purpose of the first and second pins of these two types of ICs is different –
    - The first and second pins of **78xx** voltage regulator ICs are used for connecting the input and ground respectively.

- The first and second pins of **79xx** voltage regulator ICs are used for connecting the ground and input respectively.

### Examples

- 7805 voltage regulator IC produces a DC voltage of +5 volts.
- 7905 voltage regulator IC produces a DC voltage of -5 volts.

The following figure shows how to produce a **fixed positive voltage** at the output by using a fixed positive voltage regulator with necessary connections.




In the above figure that shows a fixed positive voltage regulator, the input capacitor $C_i$ is used to prevent unwanted oscillations and the output capacitor, $C_0$ acts as a line filter to improve transient response.

**Note –** an get a **fixed negative voltage** at the output by using a fixed negative voltage regulator with suitable connections.

### Adjustable voltage regulator

An adjustable voltage regulator produces a DC output voltage, which can be adjusted to any other value of certain voltage range. Hence, adjustable voltage regulator is also called as a **variable voltage regulator**.

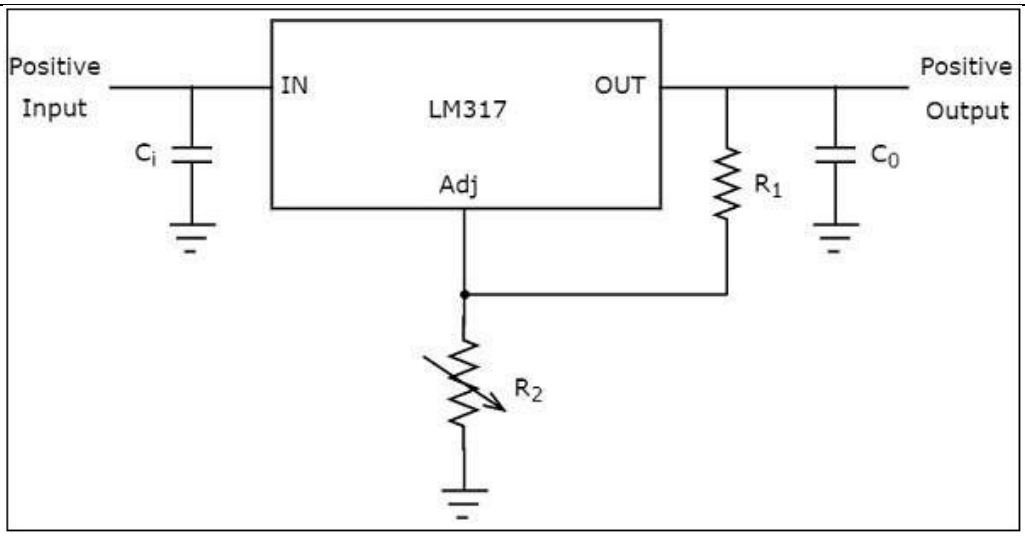
The DC output voltage value of an adjustable voltage regulator can be either positive or negative.

### LM317 voltage regulator IC

**LM317** voltage regulator IC can be used for producing a desired positive fixed DC voltage value of the available voltage range.

LM317 voltage regulator IC has 3 pins. The first pin is used for adjusting the output voltage, second pin is used for collecting the output and third pin is used for connecting the input.

The adjustable pin (terminal) is provided with a variable resistor which lets the output to vary between a wide range.




The above figure shows an unregulated power supply driving a LM 317 voltage regulator IC, which is commonly used. This IC can supply a load current of 1.5A over an adjustable output range of 1.25 V to 37 V.

**Video Content / Details of website for further learning (if any):**

https://nptel.ac.in/courses/108108111/

**Important Books/Journals for further learning including the page nos.:**

- D.Roy Choudhary, Sheil B.Jani, "Linear Integrated Circuits", II edition, New Age, pp. 223-227, 2015

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## LECTURE HANDOUTS

**EEE**

**II/III**

**Course Name with Code** :19EEC03 / Linear Integrated Circuits

**Course Faculty** : Mr.R.Suresh

**Unit** :V- Special ICs **Date of Lecture:**

**Topic of Lecture:** Adjustable Voltage Regulators

**Introduction :**

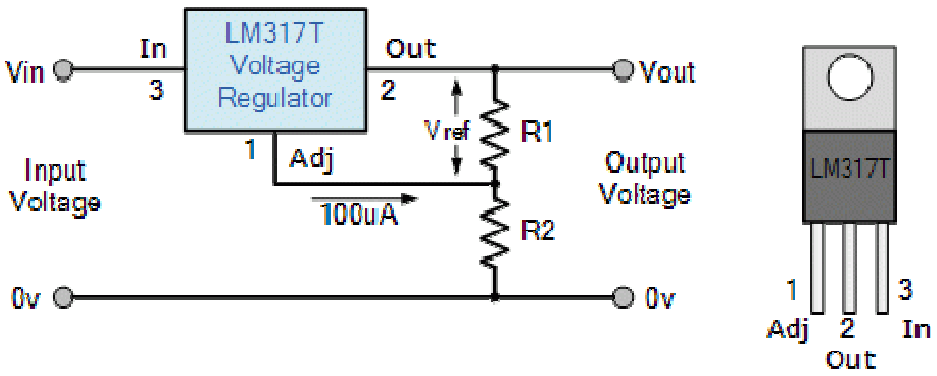
Continuing on from our tutorial about converting an ATX PSU to a bench power supply, one very good addition to this is the LM317T positive voltage regulator.

The LM317T is an adjustable 3-terminal positive voltage regulator capable of supplying different DC voltage outputs other than the fixed voltage power supply of +5 or +12 volts, or as a variable output voltage from a few volts up to some maximum value all with currents of about 1.5 amperes.

**Prerequisite knowledge for Complete understanding and learning of Topic:**

Electronic Devices

**Detailed content of the Lecture:**




With the aid of a small bit of additional circuitry added to the output of the PSU we can have a bench power supply capable of a range of fixed or variable voltages either positive or negative in nature. In fact this is more simple than you may think as the transformer, rectification and smoothing has already been done by the PSU beforehand all we need to do is connect our additional circuit to the +12 volt yellow wire output. But firstly, lets consider a fixed voltage output.

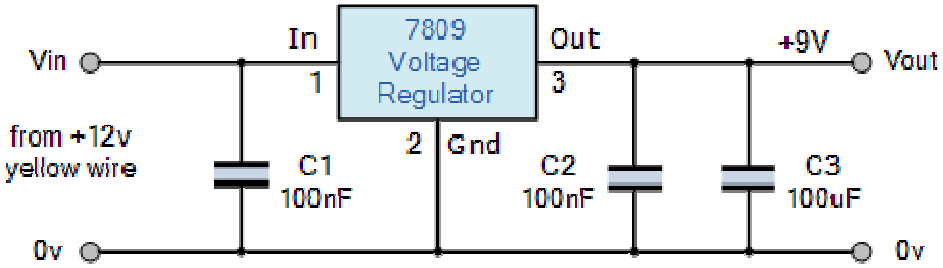
### Fixed 9v Power Supply

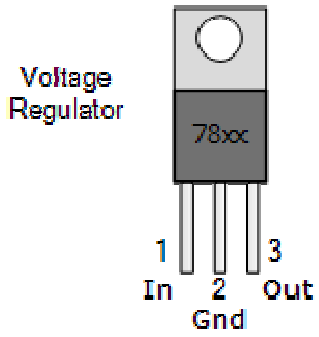
There are a wide variety of 3-terminal voltage regulators available in a standard TO-220 package with the most popular fixed voltage regulator being the 78xx series positive regulators which range from the very common 7805, +5V fixed voltage regulator to the 7824, +24V fixed voltage regulator. There is also a 79xx series of fixed negative voltage regulators which produce a complementary negative voltage from -5 to -24 volts but in this tutorial we will only use the positive **78xx** types.

The fixed 3-terminal regulator is useful in applications were an adjustable output is not required making the output power supply simple, but very flexible as the voltage it outputs is dependant only upon the chosen regulator. They are called 3-terminal voltage regulators because they only have three terminals to connect to and these are the **Input**, **Common** and **Output** respectively.

The input voltage to the regulator will be the +12v yellow wire from the PSU (or separate transformer supply), and is connected between the input and common terminals. The stabilised +9 volts is taken across the output and common as shown.

### Voltage Regulator Circuit




| Type | Min Input Voltage | Output Voltage |
|---|---|---|
| 7805 | 7V | +5V |
| 7806 | 8V | +6V |
| 7808 | 10V | +8V |
| 7809 | 11V | +9V |
| 7812 | 15V | +12V |
| 7815 | 18V | +15V |
| 7818 | 22V | +18V |
| 7824 | 30V | +24V |

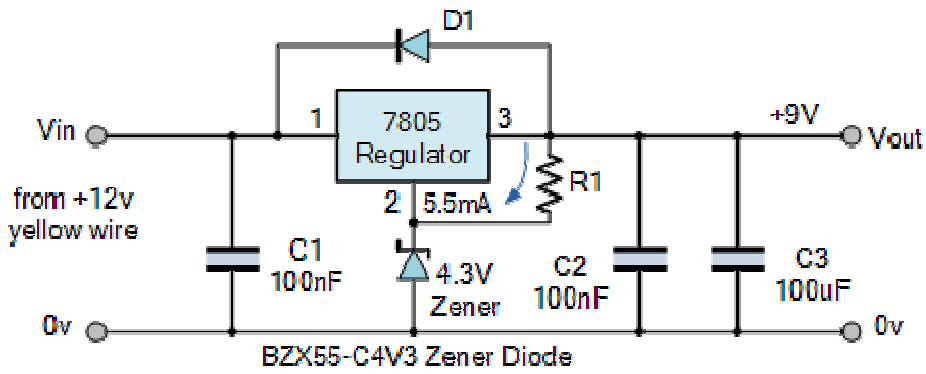
So suppose we want an output voltage of +9 volts from our PSU bench power supply, then all we have to do is connect a +9v voltage regulator to the +12V yellow wire. As the PSU has already done the rectification and smoothing to the +12v output, the only additional components required are a capacitor across the input and another across the output.

These additional capacitors aid in the stability of the regulator and can be anywhere between 100nF and 330nF. The additional 100uF output capacitor helps smooth out the inherent ripple content giving it a good transient response. This large value capacitor placed across the output of a power supply circuit is commonly called a “Smoothing Capacitor”.

These **78xx** series regulators give a maximum output current of about 1.5 amps at fixed stabilised voltages of 5, 6, 8, 9, 12, 15, 18 and 24V respectively. But what if we wanted an output voltage of +9V but only had a 7805, +5V regulator?. The +5V output of the 7805 is referenced to the “ground, Gnd” or “0v” terminal.

If we increased this pin-2 terminal voltage from 0V to 4V then the output would also rise by an additional 4 volts providing there was sufficient input voltage. Then by placing a small 4 volt (nearest preferred value of 4.3V) Zener diode between pin-2 of the regulator and ground, we can make a 7805 5V regulator produce a +9 volts output voltage as shown.

## Increasing The Output Voltage




So how does it work. The 4.3V Zener diode requires a reverse bias current of around 5mA to maintain an output with the regulator taking about 0.5mA. This total current of 5.5mA is supplied via resistor "R1" from the output pin-3.

So the value of the resistor required for a 7805 regulator will be R = 5V/5.5mA = 910 Ohm. The feedback diode, D1 connected across the input to output terminals is for protection and prevents the regulator from being reverse biased when the input supply voltage is switched OFF while the output supply remains ON or active for a short period of time due to a large inductive load such as a solenoid or motor.

Then we can use 3-terminal voltage regulators and a suitable Zener diode to produce a variety of fixed output voltages from our previous bench power supply ranging from +5V up to +12V. But we can improve on this design by replacing the fixed voltage regulator with a variable voltage regulator such as the **LM317T**.

**Video Content / Details of website for further learning (if any):**

https://nptel.ac.in/courses/108108111/

**Important Books/Journals for further learning including the page nos.:**

- D.Roy Choudhary, Sheil B.Jani, "Linear Integrated Circuits", II edition, New Age, pp. 333-339, 2015

**Course Faculty**

# MUTHAYAMMAL ENGINEERING COLLEGE

(An Autonomous Institution)

(Approved by AICTE, New Delhi, Accredited by NAAC & Affiliated to Anna University)

Rasipuram - 637 408, Namakkal Dist., Tamil Nadu

Estd. 2000


**L44**

## LECTURE HANDOUTS

**EEE**

**II/III**

**Course Name with Code** :**19EEC03 / Linear Integrated Circuits**

**Course Faculty** : **Mr.R.Suresh**

**Unit** :**V- Special ICs** **Date of Lecture:**

**Topic of Lecture:** Switching Regulators

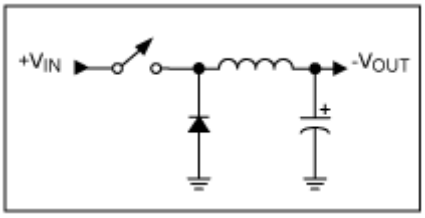
**Introduction :** A **switching regulator** is a circuit that uses a power **switch**, an inductor, and a diode to transfer energy from input to output. The power **switch**, usually a Field Effect Transistor (FET), is turned on and off by a **switching** controller IC that monitors the output of the **switching regulator** in a feedback control loop

**Prerequisite knowledge for Complete understanding and learning of Topic:**
Electronic Devices

**Detailed content of the Lecture:**

A switching regulator is a circuit that uses a power switch, an inductor, and a diode to transfer energy from input to output. The power switch, usually a Field Effect Transistor (FET), is turned on and off by a switching controller IC that monitors the output of the switching regulator in a feedback control loop. This ensures that it maintains a constant output under normal operating conditions. In some switching regulators, the FET is a discrete component, external to the switching controller. In other versions, the FET and controller are in the same IC.

The basic components of the switching circuit can be rearranged to form a step-down (buck)converter, a step-up (boost) converter, or an inverter (fly back). These designs are shown in Figures 1, 2, 3, and 4 respectively, where Figures 3 and 4 are the same except for the transformer and the diode polarity.



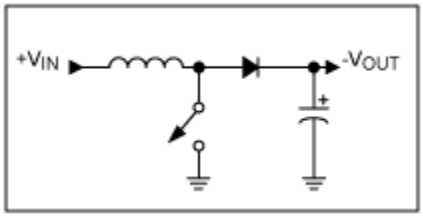




*Figure 1. Buck converter topology. Figure 2. Simple boost converter.*

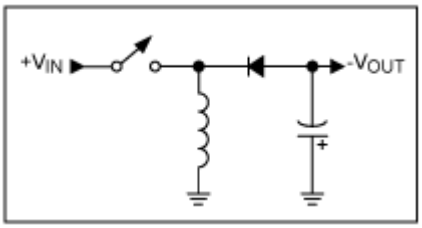



*Figure 3. Inverting topology.*

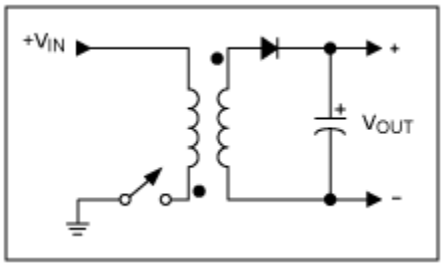



*Figure 4. Transformer flyback topology.*

Switching regulators offer three main advantages compared to linear regulators. First, switching efficiency can be much better. Second, because less energy is lost in the transfer, smaller components and less thermal management are required. Third, the energy stored by an inductor in a switching regulator can be transformed to output voltages that can be greater than the input (boost), negative (inverter), or can even be transferred through a transformer to provide electrical isolation with respect to the input . Given the advantages of switching regulators, one might wonder where can linear regulators be used? Linear regulators provide lower noise and higher bandwidth; their simplicity can sometimes offer a less expensive solution. There are, admittedly, disadvantages with switching regulators. They can be noisy and require energy management in the form of a control loop that requires a switching controller. Fortunately, the solution to these control problems is integrated in modern switching controller IC's

**Video Content / Details of website for further learning (if any):**

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- D.Roy Choudhary, Sheil B.Jani, "Linear Integrated Circuits", II edition, New Age, pp. 221-223, 2015

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**L45**

## LECTURE HANDOUTS

**EEE**

**II/III**

**Course Name with Code** :**19EEC03 / Linear Integrated Circuits**

**Course Faculty** : **Mr.R.Suresh**

**Unit** :**V- Special ICs** **Date of Lecture:**

**Topic of Lecture:** Switching Regulators

**Introduction :**Linear voltage regulators are generally much more efficient and easier to use than equivalent voltage regulator circuits made from discrete components such a zener diode and a resistor, or transistors and even op-amps.

**Prerequisite knowledge for Complete understanding and learning of Topic:**
Electronic Devices

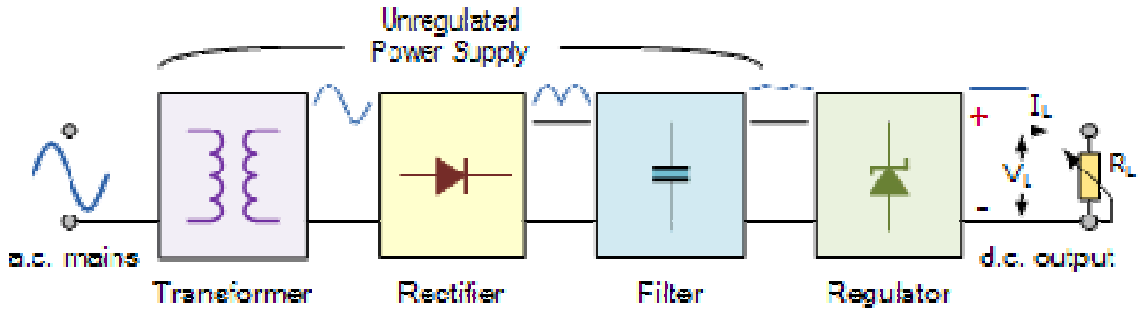
**Detailed content of the Lecture:**

The most popular linear and fixed output voltage regulator types are by far the 78… positive output voltage series, and the 79… negative output voltage series. These two types of complementary voltage regulators produce a precise and stable voltage output ranging from about 5 volts up to about 24 volts for use in many electronic circuits.

There is a wide range of these three-terminal fixed voltage regulators available each with its own built-in voltage regulation and current limiting circuits. This allows us to create a whole host of different power supply rails and outputs, either single or dual supply, suitable for most electronic circuits and applications. There are even variable voltage linear regulators available as well providing an output voltage which is continually variable from just above zero to a few volts below its maximum voltage output.

Most d.c. power supplies comprise of a large and heavy step-down mains transformer, diode rectification, either full-wave or half-wave, a filter circuit to remove any ripple content from the rectified d.c. producing a suitably smooth d.c. voltage, and some form of voltage regulator or stabiliser circuit, either linear or switching to ensure the correct regulation of the power supplies output voltage under varying load conditions. Then a typical d.c. power supply would look something like this:

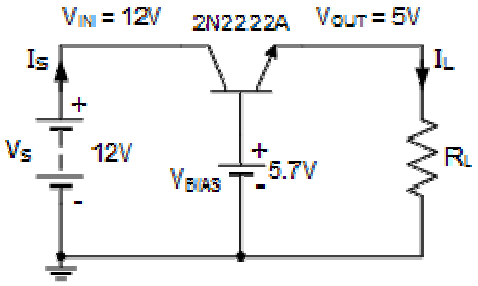
## Typical DC Power Supply




These typical power supply designs contain a large mains transformer (which also provides isolation between the input and output) and a dissipative series regulator circuit. The regulator circuit could consist of a single zener diode or a three-terminal linear series regulator to produce the required output voltage. The advantage of a linear regulator is that the power supply circuit only needs an input capacitor, output capacitor and some feedback resistors to set the output voltage.

Linear voltage regulators produce a regulated DC output by placing a continuously conducting transistor in series between the input and the output operating it in its linear region (hence the name) of its current-voltage (i-v) characteristics. Thus the transistor acts more like a variable resistance which continually adjusts itself to whatever value is needed to maintain the correct output voltage. Consider this simple series pass transistor regulator circuit below:

## Series Transistor Regulator Circuit




Here this simple emitter-follower regulator circuit consists of a single NPN transistor and a DC biasing voltage to set the required output voltage. As an emitter follower circuit has unity voltage gain, applying a suitable biasing voltage to the transistors base, a stabilised output is obtained from the emitter terminal. Since a transistor provides current gain, the output load current will be much higher than the base current and higher still if a Darlington transistor arrangement is used.

Also, providing that the input voltage is sufficiently high enough to get the desired output voltage, the output voltage is controlled by the transistors base voltage and in this example is given as 5.7 volts to produce a 5 volt output to the load as approximately 0.7 volts is dropped across the transistor between the base and emitter terminals. Then depending upon the value of the base voltage, any value of emitter output voltage can be obtained.

While this simple series regulator circuit will work, the downside to this is that the series transistor is continually biased in its linear region dissipating power in the form of heat as a result of its V*I product, since all the load current must pass through the series transistor, resulting in poor efficiency, wasted power and continuous heat generation.

Also, one of the disadvantages that series voltage regulators have is that, their maximum continuous output current rating is limited to just a few amperes or so, so are generally used in applications where

low power outputs are required. When higher output voltage or current power supplies are required, the normal practice is to use a switching regulator commonly known as a *switch-mode power supply* to convert the mains voltage into whatever higher power output is required.

**Video Content / Details of website for further learning (if any):**

https://nptel.ac.in/courses/108108111/

**Important Books/Journals for further learning including the page nos.:**

- D.RoyChoudhary, SheilB.Jani, "Linear Integrated Circuits", II edition, New Age, pp. 225-227, 2015

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