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Rasipuram - 637 408, Namakkal Dist., Tamil Nadu

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LECTURE HANDOUTS

MDE

II /III

Course Name with Code : **19MDC04 – LOGIC CIRCUITS FOR CLINICAL ENGINEERS**

Course Faculty : **Mrs.M.Birunda**

Unit : **I - IC FABRICATION AND OPERATIONAL AMPLIFIER**

Date of Lecture: 18.08.2021

Topic of Lecture: Introduction to Integrated Circuits- & Classification of IC's

Introduction :

An integrated circuit or monolithic integrated circuit (also referred to as an IC, a chip, or a microchip) is a set of electronic circuits on one small flat piece (or "chip") of semiconductor material that is normally silicon.

Prerequisite knowledge for Complete understanding and learning of Topic:

Basic Analog electronics and Electronic Devices, and Circuit theory

Introduction to Integrated Circuits- & Classification of IC's:

The concept of IC was first introduced in the year 1958. Due to its small dimension, low cost, and very high reliability even the common man is familiar with its applications like smart phones and laptops. All IC's consist of both active and passive components and the connections between them are so small that it may be impossible to see them even though a microscope. All the components (active and passive) are interconnected through fabrication process.

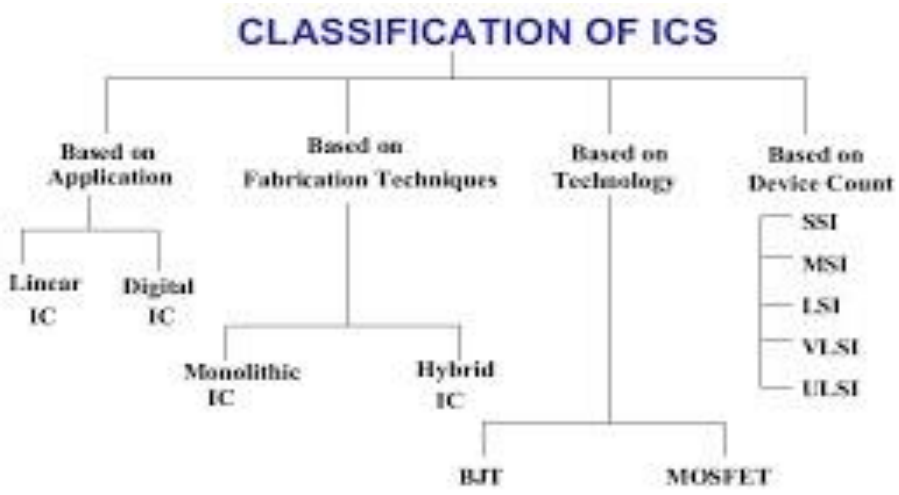
Advantages of Integrated Circuits

1. Miniature in size. As fabrication process is used for the integration of active and passive components on to a silicon chip, the IC becomes a lot smaller. When compared to a discrete circuit, it may be at least a thousand times smaller.
2. Due to small size, the weight of the IC also reduces, when compared to the discrete circuit.
3. To produce hundreds of discrete circuits on a PCB for the same logic takes more time and increase the cost factor. But for the production of hundreds of IC's the cost of production will be very low and less time consuming.
4. The PCB consisting soldered joints will be less reliable. This problem is omitted in IC's because of no soldered joints, with fewer interconnections, and thus highly reliable.
5. The small size of IC's causes lesser power consumption and lesser power loss.
6. In a discrete circuitry, if a single transistor becomes faulty, the whole circuit may fail to work. This transistor has to be desoldered and replaced. It is difficult to find out which component has failed. This problem can be omitted in an IC by replacing an entire IC as it is low in cost.
7. Increased operating speed because of absence of parasitic capacitance effect.
8. As the IC's are produced in bulk the temperature coefficients and other parameters will be closely matching.

9. Improved functional performance as more complex circuits can be fabricated for achieving better characteristics.
10. All IC's are tested for operating ranges in very low and very high temperatures.
11. As all the components are fabricated very close to each other in an IC, they are highly suitable for small signal operation, as there won't be any stray electrical pickup.
12. As all the components are fabricated inside the chip, there will not be any external projections.

Disadvantages of Integrated Circuits

1. Some complex IC's maybe costly. If such integrated circuits are used roughly and become faulty, they have to be replaced by a new one. They cannot be repaired as the individual components inside the IC are too small.
2. The power rating for most of the IC's does not exceed more than 10 watts. Thus it is not possible to manufacture high power IC's.
3. Some components like transformers and inductors cannot be integrated into an IC. They have to be connected externally to the semiconductor pins.
4. High grade P-N-P assembly is not possible.
5. The IC will not work properly if wrongly handled or exposed to excessive heat.
6. It is difficult to achieve low temperature coefficient.
7. It is difficult to fabricate an IC with low noise.
8. It is not possible to fabricate capacitors that exceed a value of 30pF. Thus, high value capacitors are to be connected externally to the IC.
9. There is a large value of saturation resistance of transistors.



Video Content / Details of website for further learning (if any):

https://www.youtube.com/watch?v=lpXNCwsnxjM

Important Books/Journals for further learning including the page nos.:

Linear Integrated Circuits by Ray choudray T1

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Course Name with Code : 19MDC04 – LOGIC CIRCUITS FOR CLINICAL ENGINEERS

Course Faculty : Mrs.M.Birunda

Unit : I - IC FABRICATION AND OPERATIONAL AMPLIFIER

Date of Lecture: 18.08.2021

Topic of Lecture: Basic IC Fabrication Planar Process-Fabrication of Diode and BJT

Introduction :

The active and passive components such as resistors, diodes, transistors etc and external connections are usually fabricated in on extremely tiny single chip of silicon. ... In IC chips, the fabrication of circuit elements such as transistors, diodes, capacitors etc. and their interconnections are done at same time.

Prerequisite knowledge for Complete understanding and learning of Topic:

Basic Analog electronics and Electronic Devices, and Circuit theory

Introduction to IC

Basic IC Fabrication Planar Process-Fabrication of Diode and BJT:

The planar process is a manufacturing process used in the semiconductor industry to build individual components of a transistor, and in turn, connect those transistors together. It is the primary process by which silicon integrated circuit chips are built. The process utilizes the surface passivation and thermal oxidation methods.

P-layer Substrate Manufacture

The silicon is then cut into thin slices with high precision using a diamond saw. After cutting hundreds of them each wafer is polished and cleaned to form a P-type substrate layer.

N-type Epitaxial Growth

The epitaxial groth process of a low resistive N-type over a high resistive P-type is to be carried out. This is done by placing the n-type layer on top of the P-type and heating.

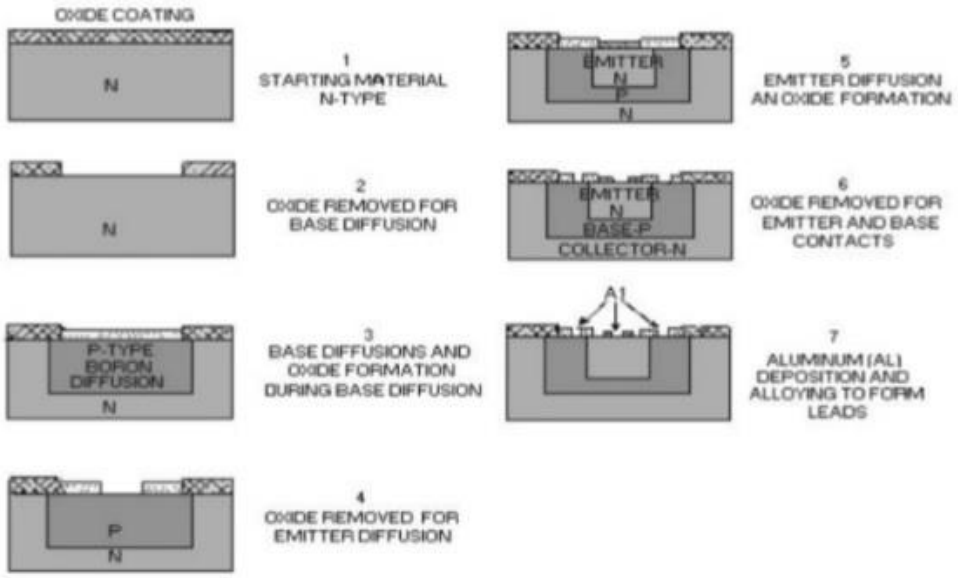
The Silicon Dioxide Insulation Layer

This layer is required contamination of the N-layer epitaxy.

Photolithographic Process for SiO2

To diffuse the impurities with the N-type epitaxial region, the silicon dioxide layer has to be etched in selected areas. Thus openings must be brought at these areas through photolithographic process. In this process, the SiO2 layer is coated with a thin layer of a photosensitive material called photoresist.

Fabrication of transistor :



Isolation Diffusion

To get a proper time period for allowing a P-type impurity to penetrate into the N-type epitaxial layer, isolation diffusion is to be carried out. By this process, the P-type impurity will travel through the openings in SiO2 layer, and the N-type layer and thus reach the P-type substrate, Isolation junctions are used to isolate between various components of the IC.

Base Diffusion

This process is done to create a new layer of SiO2 over the wafer. P-regions are formed under regulated environments by diffusing P-type impurities

Emitter Diffusion

Masking and etching process is again carried out to form a layer of silicon dioxide over the entire surface and opening of the P-type region. The transistor emitters, the cathode regions for diodes, and junction capacitors are grown by diffusion using N-type impurities

Aluminium Metallization

The windows made in the N-region after creating a silicon dioxide layer are then deposited with aluminium on the top surface.

Scribing and Mounting

After the metallization process, the silicon wafer is then scribed with a diamond tipped tool and separated into individual chips.

Video Content / Details of website for further learning (if any):

https://www.youtube.com/watch?v=35jWSQXku74

Important Books/Journals for further learning including the page nos.:

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Course Name with Code : 19MDC04 – LOGIC CIRCUITS FOR CLINICAL ENGINEERS

Course Faculty : Mrs.M.Birunda

Unit : I - IC FABRICATION AND OPERATIONAL AMPLIFIER

Date of Lecture:

Topic of Lecture: Fabrication of Diode and BJT

Introduction :

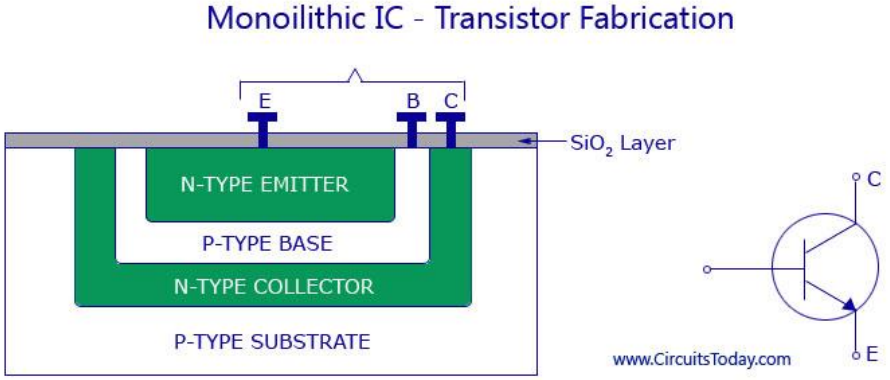
The fabrication of the transistor is the process of creating the transistor that is used in electrical and electronics circuit. It is a photo-lithographic or chemical process of creating the transistor on the wafer of semiconductor material. Two commonly used techniques for Diode Fabrication Process and Packaging are the alloy method and the diffusion method. To construct an alloy diode, a pn-junction is formed by melting a tiny pellet of aluminum (or some other p-type impurity) on the surface of an n-type crystal.

Prerequisite knowledge for Complete understanding and learning of Topic:

Introduction to IC, Basic IC fabrication process steps.

Fabrication of Diode and BJT:

The fabrication process of a transistor is shown in the figure below. A P-type substrate is first grown and then the collector, emitter, and base regions are diffused on top of it as shown in the figure. The surface terminals for these regions are also provided for connection.



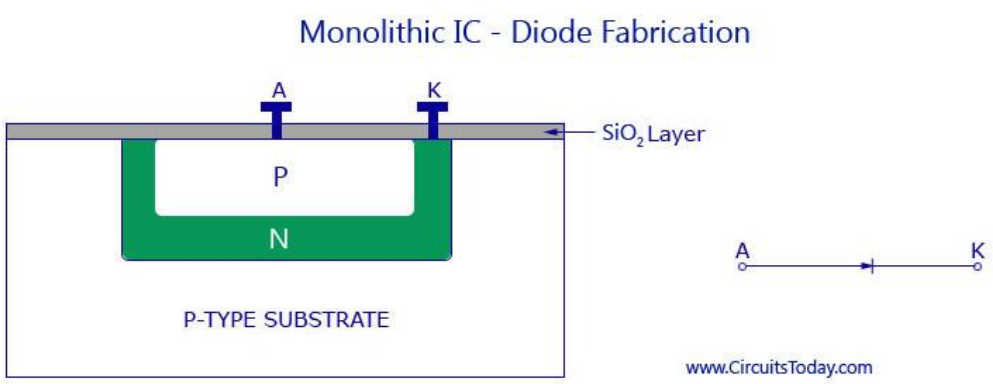
Monoilithic IC - Transistor Fabrication

Both transistors and diodes are fabricated by using the epitaxial planar diffusion process that is explained earlier. In case of discrete transistors, the P-type substrate is considered as the collector. `But this is not possible in monolithic IC's, as all the transistors connected on one P-

type substrate would have their collectors connected together. This is why separate collector regions are diffused into the substrate. Even though separate collector regions are formed, they are not completely isolated from the substrate. For proper functioning of the circuit it is necessary that the P-type substrate is always kept negative with respect to the transistor collector. This is achieved by connecting the substrate to the most negative terminal of the circuit supply. The unwanted or parasitic junctions, even when reverse-biased, can still affect the circuit performance adversely. The junction reverse leakage current can cause a serious problem in circuits operating at very low current levels. The capacitance of the reverse-biased junction may affect the circuit high-frequency performance, and the junction break down voltage imposes limits on the usable level of supply voltage. All these adverse effects can be reduced to the minimum if highly resistive material is employed for the substrate. If the substrate is very lightly doped, it will behave almost as an insulator.

Diodes

They are also fabricated by the same diffusion process as transistors are. The only difference is that only two of the regions are used to form one P-N junction. In figure, collector-base junction of the transistor is used as a diode. Anode of the diode is formed during the base diffusion of the transistor and the collector region of the transistor becomes the cathode of the diode. For high speed switching emitter base junction is used as a diode.



Video Content / Details of website for further learning (if any):

https://www.khanacademy.org/science/electrical-engineering/ee-amplifiers/ee-opamp/v/ee-opamp-intro

Important Books/Journals for further learning including the page nos.:

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Course Name with Code : 19MDC04 – LOGIC CIRCUITS FOR CLINICAL ENGINEERS

Course Faculty : Mrs.M.Birunda

Unit : I - IC FABRICATION AND OPERATIONAL AMPLIFIER

Date of Lecture:

Topic of Lecture: Operational Amplifier: Basic Information of op-amp

Introduction :

An Operational Amplifier or op-amp is a voltage amplifying device designed to be used with external feedback components such as resistors and capacitors between its output and input terminals. It is a high-gain electronic voltage amplifier with a differential input and usually a single-ended output.

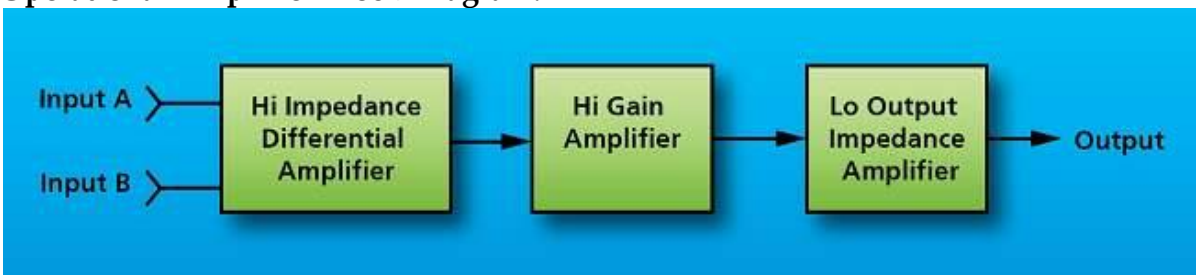
Prerequisite knowledge for Complete understanding and learning of Topic:

Transistor operation as a differential amplifier

Operational Amplifier: Basic Information of op-amp :

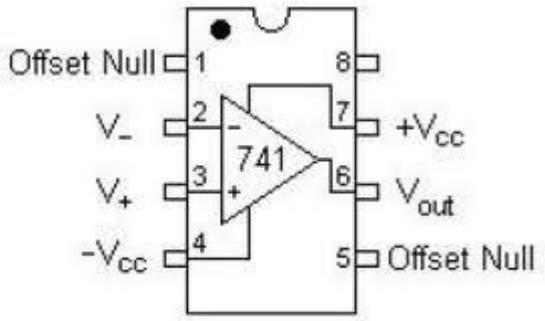
Operational Amplifiers, also known as Op-amps, are basically a voltage amplifying device designed to be used with components like capacitors and resistors, between its in/out terminals. They are essentially a core part of analog devices. Feedback components like these are used to determine the operation of the amplifier. The amplifier can perform many different operations (resistive, capacitive, or both), giving it the name Operational Amplifier.

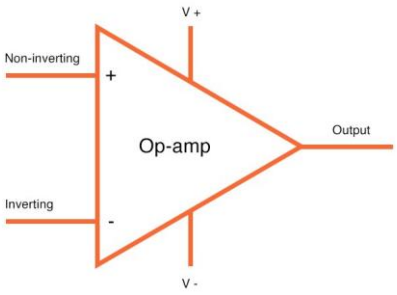
Operational Amplifier Block Diagram:



OPAMP Pin Configuration:

Op-amps are linear devices that are ideal for DC amplification and are used often in signal conditioning, filtering or other mathematical operations (add, subtract, integration and d3.8.ifferentiation).





The operational amplifier is arguably the most useful single device in analog electronic circuitry. With only a handful of external components, it can be made to perform a wide variety of analog signal processing tasks. It is also quite affordable, most general-purpose amplifiers selling for under a dollar apiece. Modern designs have been engineered with durability in mind as well: several "op-amps" are manufactured that can sustain direct short-circuits on their outputs without damage.

One key to the usefulness of these little circuits is in the engineering principle of feedback, particularly negative feedback, which constitutes the foundation of almost all automatic control processes. The principles presented in this section, extend well beyond the immediate scope of electronics. It is well worth the electronics student's time to learn these principles and learn them well.

Video Content / Details of website for further learning (if any):

https://www.youtube.com/watch?v=kiiA6WTCQn0

Important Books/Journals for further learning including the page nos.:

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II / IV

Course Name with Code : 19MDC04 – LOGIC CIRCUITS FOR CLINICAL ENGINEERS

Course Faculty : Mrs.M.Birunda

Unit : I - IC FABRICATION AND OPERATIONAL AMPLIFIER

Date of Lecture:

Topic of Lecture: Ideal Op Amp

Introduction :

An Operational Amplifier or op-amp is a voltage amplifying device designed to be used with external feedback components such as resistors and capacitors between its output and input terminals. It is a high-gain electronic voltage amplifier with a differential input and usually a single-ended output.

Prerequisite knowledge for Complete understanding and learning of Topic:

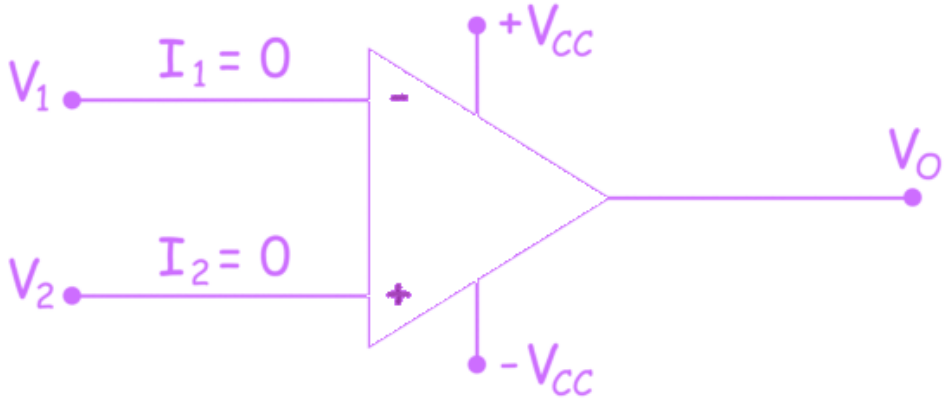
Basics of operational amplifier, Operation of Transistor as a differential amplifier.

Ideal Op Amp

We know that, the input resistance of an op amp must be very high where as the output resistance should be quite low. An op amp should also have very high open loop gain. In ideal cases, the input resistance and open loop gain of an op amp should be infinity whereas the output resistance would be zero. So an **ideal op amp** should have following characteristics.

Characteristic	Value
Open Loop Gain (A)	∝
Input Resistance	∝
Output Resistance	0
Bandwith of Operation	∝
Offset Voltage	0

So, an **ideal op amp** is defined as, a differential amplifier with infinite open loop gain, infinite input resistance and zero output resistance. The **ideal op amp** has zero input current. This is because of infinite input resistance. As the input resistance of **ideal op amp** is infinite, an open circuit exists at input, hence current at both input terminals is zero.



There is no current through the input resistance, there will be no voltage drop between the input terminals. Hence no offset voltage appears across the inputs of an **ideal operational amplifier**.
If v1 and v2 are the voltages of inverting and non-inverting terminals of op amp, and v1 = v2 then in ideal

Video Content / Details of website for further learning (if any):

https://www.allaboutcircuits.com/video-lectures/op-amps-internal-circuitry/

Important Books/Journals for further learning including the page nos.:

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Course Faculty : Mrs.M.Birunda

Unit : I - IC FABRICATION AND OPERATIONAL AMPLIFIER

Date of Lecture:

Topic of Lecture: Operational Amplifier Internal Circuit

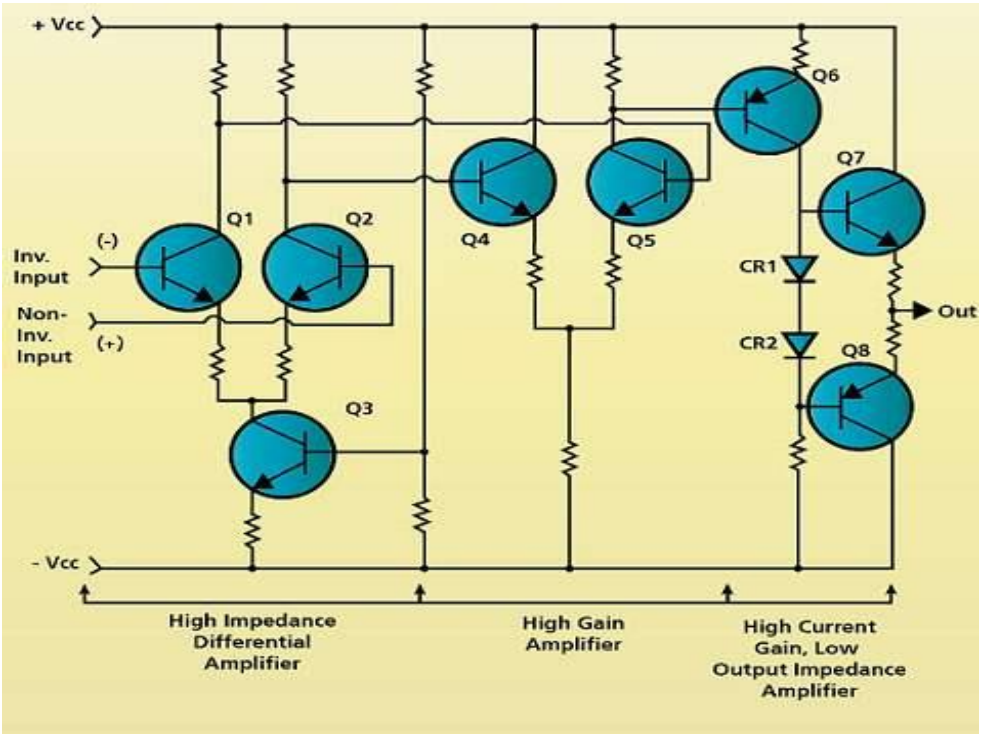
Introduction :

An Operational Amplifier or op-amp is a voltage amplifying device designed to be used with external feedback components such as resistors and capacitors between its output and input terminals. It is a high-gain electronic voltage amplifier with a differential input and usually a single-ended output.

Prerequisite knowledge for Complete understanding and learning of Topic:

Basic Analog electronics, Operation of Transistor as a differential amplifier, Constant current source.

Operational Amplifier Internal Circuit :



- The input signals to the inverting and non-inverting terminals are directly coupled to high impedance, differential amplifier composed of transistors Q` and Q.

- Transistor Q senses the negative and positive supply voltages and functions as a constant current source to regulate against voltage supply variations.
- Transistors Q? and Qr form another differential amplifier to provide additional voltage gain. Transistor Qq controls the biasing of transistors Qo and Qp, which are connected as emitter-followers to provide a high current gain and low output impedance.
- Diodes CR` and CR provide temperature stability.
- The actual operating characteristics of an op amp come very close to the characteristics of an "ideal amplifier.

Video Content / Details of website for further learning (if any):

https://www.allaboutcircuits.com/video-lectures/op-amps-internal-circuitry/

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II / IV

Course Name with Code : 19MDC04 – LOGIC CIRCUITS FOR CLINICAL ENGINEERS

Course Faculty : Mrs.M.Birunda

Unit : I - IC FABRICATION AND OPERATIONAL AMPLIFIER

Date of Lecture:

Topic of Lecture: Differential Amplifier

Introduction :

A differential amplifier is designed to give the difference between two input signals. When a differential amplifier is driven at one of the inputs, the output appears at both the collector outputs

Prerequisite knowledge for Complete understanding and learning of Topic:

Basic Analog electronics and Electronic Devices, and Circuit theory, Transistor operation

Differential Amplifier :

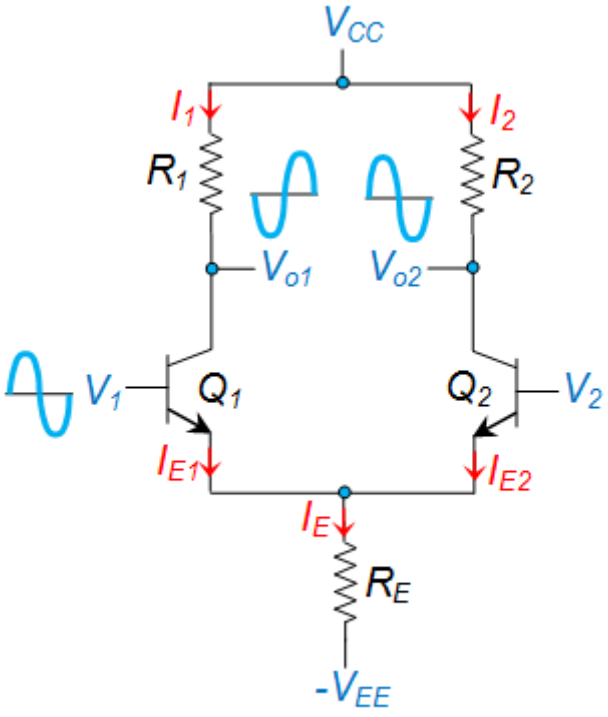

Figure 1 A BJT Differential Amplifier

Figure 1 shows such a circuit made of two BJTs (Q1 and Q2) and two power supplies of opposite polarity viz., VCC and –VEE which uses three resistors among which two are the collector

resistors, RC1 and RC2 (one for each transistor) while one is the emitter resistor RE common to both transistors.

Here the input signals (V1 and V2) are applied to the base of the transistors while the output is collected across their collector terminals (Vo1 and Vo2).

$$V_0 = A_d(V_1 - V_2)$$

Where V1 and V2 represent the voltages applied at its inverting and non-inverting input terminals (can be taken in any order) and Ad refers to its differential gain. As per this equation, the output of the OpAmp must be zero when the voltages applied at its terminals are equal to each other. However practically it will not be so as the gain will not be same for both of the inputs.

Video Content / Details of website for further learning (if any):

https://www.youtube.com/watch?v=tC43ztgutwo

Important Books/Journals for further learning including the page nos.:

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LECTURE HANDOUTS | **L 08**

MDE | **II / IV**

Course Name with Code : **19MDC04 – LOGIC CIRCUITS FOR CLINICAL ENGINEERS**

Course Faculty : **Mrs.M.Birunda**

Unit : **I - IC FABRICATION AND OPERATIONAL AMPLIFIER**

Date of Lecture:

Topic of Lecture: Analysis of current sources-Widlar

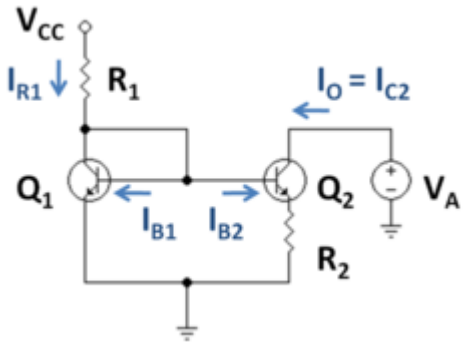
Introduction :

A Widlar current source is a modification of the basic two-transistor current mirror that incorporates an emitter degeneration resistor for only the output transistor, enabling the current source to generate low currents using only moderate resistor values.

Prerequisite knowledge for Complete understanding and learning of Topic:

Basic Analog electronics and Electronic Devices, and Circuit theory, Basic constant current s working and its necessity

Analysis of current sources-Widlar :



$$V_B = V_{BE1} = V_{BE2} + (\beta_2 + 1) I_{B2} R_2$$

$$\Rightarrow \frac{1}{R_2}(V_{BE1} - V_{BE2}) = (\beta_2 + 1) I_{B2} \ ,$$

$$(\beta_2 + 1) I_{B2} = \left(1 + \frac{1}{\beta_2}\right) I_{C2} = \frac{1}{R_2}(V_{BE1} - V_{BE2})$$

$$= \frac{V_T}{R_2}[\ln(I_{C1} I_{S2}) - \ln(I_{C2} I_{S1})] = \frac{V_T}{R_2} \ln\left(\frac{I_{C1} I_{S2}}{I_{C2} I_{S1}}\right) ,$$

Finding the current with given resistor values

$$
\begin{aligned}
I_{R1} &= I_{C1} + I_{B1} + I_{B2} \\
&= I_{C1} + \frac{I_{C1}}{\beta_1} + \frac{I_{C2}}{\beta_2} \\
&= \frac{1}{R_1}\left(V_{CC} - V_{BE1}\right)
\end{aligned}
$$

$$
I_{C1} = \frac{\beta_1}{\beta_1 + 1}\left(\frac{V_{CC} - V_{BE1}}{R_1} - \frac{I_{C2}}{\beta_2}\right)
$$

$$
V_{BE1} = V_{\mathrm{T}} \ln\left(\frac{I_{C1}}{I_{S1}}\right).
$$

$$
I_{C2} = \frac{V_{\mathrm{T}}}{\left(1 + \frac{1}{\beta_2}\right) R_2} \ln\left(\frac{I_{C1}}{I_{C2}}\right)
$$

These three relations are a nonlinear, implicit determination for the currents that can be solved by iteration.

- We guess starting values for I_{C1} and I_{C2}.
- We find a value for V_{BE1}:

$$
V_{BE1} = V_{\mathrm{T}} \ln\left(\frac{I_{C1}}{I_{S1}}\right)
$$

$$
I_{C1} = \frac{\beta_1}{\beta_1 + 1}\left(\frac{V_{CC} - V_{BE1}}{R_1} - \frac{I_{C2}}{\beta_2}\right)
$$

$$
I_{C2} = \frac{V_{\mathrm{T}}}{\left(1 + \frac{1}{\beta_2}\right) R_2} \ln\left(\frac{I_{C1}}{I_{C2}}\right).
$$

Video Content / Details of website for further learning (if any):

https://www.youtube.com/watch?v=B6yus5h8Sek

Important Books/Journals for further learning including the page nos.:

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LECTURE HANDOUTS

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II / IV

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Course Faculty : Mrs.M.Birunda

Unit : I - IC FABRICATION AND OPERATIONAL AMPLIFIER

Date of Lecture:

Topic of Lecture: Wilson Current Sources

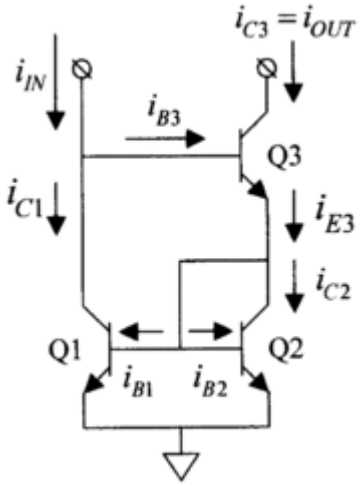
Introduction :

A Wilson current mirror or Wilson current source, named after George Wilson, is an improved mirror circuit configuration designed to provide a more constant current source or sink. It provides a much more accurate input to output current gain.

Prerequisite knowledge for Complete understanding and learning of Topic:

Basic Analog electronics and Electronic Devices, and Circuit theory, Basic constant current s working and its necessity

Wilson Current Sources :



- There are three principal metrics of how well a current mirror will perform as part of a larger circuit. The first measure is the static error, the difference between the input and output currents expressed as a fraction of the input current.
- Minimizing this difference is critical in such applications of a current mirror as the differential to single-ended output signal conversion in a differential amplifier stage because this difference controls the common mode and power supply rejection ratios.
- The second measure is the output impedance of the current source or equivalently its inverse, the output conductance.
- This impedance affects stage gain when a current source is used as an active load and

affects common mode gain when the source provides the tail current of a differential pair.

- The last metric is the pair of minimum voltages from the common terminal, usually a power rail connection, to the input and output terminals that are required for proper operation of the circuit.

The Wilson current mirror has the particular advantages over alternatives that:

- . The static error, the input-output current difference, is reduced to very small levels attributable almost entirely to random device mismatches while the output impedance is raised by a factor of {\displaystyle \scriptstyle {\frac {\beta }{2}}} simultaneously
- The circuit uses minimum resources. It does not require additional bias voltages or large area resistors as do cascaded or resistively degenerated mirrors.
- The low impedance of its input and internal nodes makes it possible to bias the circuit for operation at frequencies up to {\displaystyle \scriptstyle {\frac {f_{T}}{10}}}.
- The four-transistor version of the circuit has extended linearity for operation at high currents.

The Wilson current mirror has the limitations that:

- The minimum potentials from input or output to the common rail connection that are needed for proper operation are higher than for the standard two-transistor mirror. This reduces the headroom available to generate the input current and limits the compliance of the output.
- This mirror uses feedback to raise the output impedance in such a way that the output transistor contributes collector current fluctuation noise to the output. All three transistors of the Wilson current mirror add noise to the output.
- For stable, low-noise operation it may be necessary to modify the circuit to eliminate this effect.
- In some applications of a current mirror, particularly for biasing and active load applications, it is advantageous to produce multiple current sources from a single input reference current.
- This is not possible in the Wilson configuration while maintaining an accurate match of the input current to the output currents.{\displaystyle V_{BE1}=V_{\text{T}}\ln \left({\frac {I_{C1}}{I_{S1}}}\right)\ .}

Video Content / Details of website for further learning (if any):

https://www.youtube.com/watch?v=CiXfrsx0--Q

Important Books/Journals for further learning including the page nos.:

Linear Integrated Circuits by Ray choudray T1

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LECTURE HANDOUTS

L 10

MDE

II / IV

Course Name with Code : 19MDC04 – LOGIC CIRCUITS FOR CLINICAL ENGINEERS

Course Faculty : Mrs.M.Birunda

Unit : II - Characteristics of OP Amp and Applications

Date of Lecture:

Topic of Lecture: Characteristics of Op- Amp - DC Characteristics

Introduction :

Operational Amplifier: The operational amplifier is a direct-coupled high gain amplifier. It is a versatile multi-terminal device that can be used to amplify dc as well as ac input signals. It was originally designed for performing mathematical operations such as addition, subtraction, multiplication and integration and is abbreviated as op-amp.

Prerequisite knowledge for Complete understanding and learning of Topic:

Operational Amplifier

Dc characteristics:

An ideal op- amp draws no current from the source and its response is also independent of temperature. However, a real op-amp does not work this way. Current is taken from the source into the op-amp inputs. Also the inputs respond differently to current and voltage due to mismatch in transistors. A real op-amp also shifts its operation with temperature. These non- ideal dc characteristics that add error components to the dc output voltage are:

1. Input bias current
2. Input offset current
3. Input offset voltage
4. Thermal drift

1. Input bias current:

It is defined as the average value of the base currents entering into the input terminals of an op-amp during the input bias current. The op-amp input is a differential amplifier, which may be made of BJT or FET. In either case, the input transistors must be biased into their linear region by supplying currents into the bases by the external circuit.

In an ideal op-amp we assume that no current is drawn from the input terminals. However, practically, input terminals do conduct a small value of dc current to bias the input transistors.

The base currents entering into the inverting and non-inverting terminals are shown as IB^ (-) and IB^ (+) respectively.

Even though both the transistors are identical, IB^ (-) and IB^ (+) are not exactly equal due to internal imbalances between the two inputs.

IB= IB^ (+) + IB^ (-)/ 2 ,

Where IB^ (+) – bias current at non- inverting terminal IB (-) - bias current at inverting

terminal

Input bias current compensation:

- IB for BJT is 500Ma
- IB for FET is 50pA

By introducing compensation resistor at the non-inverting input terminal we can able to reduce the input bias current.

$$Rcomp=R1/\ Rf= (R1*\ Rf)\ /\ (R1+Rf)$$

2. Input offset current:

Bias current compensation will work efficiently if both the bias currents IB^ (+) and IB^ (-) are equal. The input transistors cannot be made identical. Hence there will be difference in bias currents. This difference is called as input offset current Ios and can be written as

$$|\ Ios\ |\ =\ IB^{\wedge}\ (+)\ -\ IB^{\wedge}\ (-)$$

The absolute value sign indicates that there is no way to predict which of the bias currents will be larger.

Input offset current for BJT is 200nA.

Input offset current for FET is 10pA.

The effect of Ios can be minimized by having the feedback resistor value to be small.

3. Input offset voltage:

In spite of the use of the above compensation techniques, it is found that the output voltage may still not be zero with zero input voltage. This is due to unavoidable imbalances inside the op-amp and one may have to apply a small voltage at the input terminals to make output voltage zero. This voltage is called input offset voltage Vios. This is the voltage required to be applied at the input for making output voltage to zero volts.

The voltage V2 at negative terminal is

$$V2 =R\ 1.V0/R1+Rf\ Or$$

$$V0 = (R1 +Rf)V2/R1 = (1+\ Rf/R1)V2$$

Since VOS = |Vi –V2| and

Vi = 0 VOS = |0 –V2| = V2

4. Thermal drift:

Bias current, offset current and offset voltage change with temperature. A circuit carefully mulled at 25 degree Celsius may not remain so when the temperature rises to 35 degree Celsius. This is called drift. Often, offset current drift is expressed in nA/0C and offset voltage drift in mV/0C. These indicate the change in offset for each degree Celsius change in temperature.

Video Content / Details of website for further learning (if any):

https://www.youtube.com/watch?v=uyOfonR_rEw

Important Books/Journals for further learning including the page nos.:

Linear Integrated Circuits Sixth Edition Ganesh Babu T.R,Suseela B,SCITECH Publication

"Understanding Single-Ended, Pseudo-Differential and Fully-Differential ADC Inputs". Maxim Application Note 1108. Archived from the original on 2007-06-26. Retrieved November 10, 2007.

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LECTURE HANDOUTS

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MDE

II / IV

Course Name with Code : 19MDC04 – LOGIC CIRCUITS FOR CLINICAL ENGINEERS

Course Faculty : Mrs.M.Birunda

Unit : II - Characteristics of OP Amp and Applications

Date of Lecture:

Topic of Lecture: AC Characteristics, Frequency Response – Frequency Compensation, Slew rate

Introduction :

Operational Amplifier: The operational amplifier is a direct-coupled high gain amplifier.

It is a versatile multi-terminal device that can be used to amplify dc as well as ac input signals. It was originally designed for performing mathematical operations such as addition, subtraction, multiplication and integration and is abbreviated as op-amp.

Prerequisite knowledge for Complete understanding and learning of Topic:

Operational Amplifier

Detailed content of the Lecture:

Ac characteristics:

For small signal sinusoidal applications the a.c. characteristics are

1. Frequency response
2. Slew rate

1. Frequency response:

An ideal op-amp has infinite band width that is open loop gain is 90dB with d.c.signal and this gain should remain the same through audio and radio frequency.

But practically op-amp gain decreases at high frequency. This is due to a capacitive component in the equivalent circuit of op-amp.

Due to R0C, the gain decreases by 20 dB per decay and the frequency is said to be brake or corner frequency and is given by

$$f1 = 1/ (2*3.14*R0*C)$$

$$|A| = A0*L/ (1+ (f/f1) ^2)$$

2. Slew rate:

The slew rate is defined as the maximum rate of change of output voltage caused by a step input voltage and is usually specified in V/μs. for e.g. A 1V/μs slew rate means that the output rises or falls by 1V in one 1μs.

The rate of change of output voltage due to the step input voltage and is usually specified as V/micro sec.

For example: 1V/micro sec. slew rate denotes the output rises or falls by 1 volts in 1 micro seconds. The rate at which the voltage across the capacitor dVc/dt is given by dVc/dt = I/C

Slew rate SR $dVc/dt|_{max} = Imax/ C$

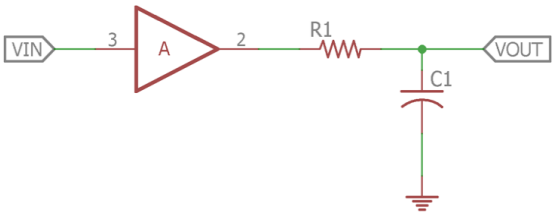
For IC741
Imax= 15 micro amps, C= 30 Pico farad Slew rate = 0.5V/ micro sec.

Frequency Compensation

However, all techniques are categorized into two basic types of compensation technique. The first one is external compensation across the op-amp and the second one is the internal compensation technique.

1. Dominant pole Compensation

This technique uses a simple RC network connected across the output of the operational amplifier circuit. A sample dominant pole compensation circuit is shown below.



This works great to overcome the instability issue. The RC network creates a pole at unity or 0dB gain that dominates or cancels out other high-frequency poles effect. The transfer function of the dominant pole configuration is –

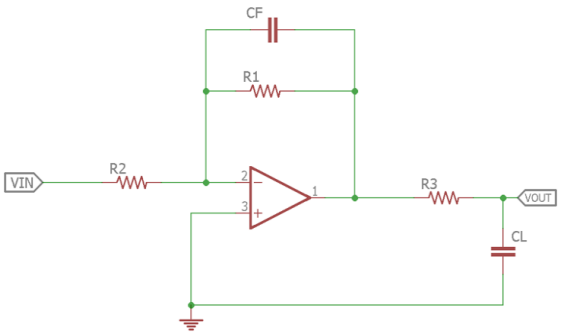
$$A(s) = \frac{A \times \omega 1 \times \omega 2 \times \omega 3}{(s+\omega 1) \times (s+\omega 2) \times (s+\omega 3)}$$

Where, A(s)is the uncompensated transfer function, A is the open-loop gain, ω1, ω2, and ω3 are the frequencies where the gain roll-off at -20dB, -40dB, -60dB respectively. The Bode plot below shows what happens if the dominant pole compensation technique is added across the op-amp output, where fd is the dominant pole frequency.

2. Miller compensation

Another effective compensation technique is the miller compensation technique and it is an in-loop compensation technique where a simple capacitor is used with or without load isolation resistor (Nulling resistor). That means a capacitor is connected in the feedback loop to compensate the op-amp frequency response.

The miller compensation circuit is shown below. In this technique, a capacitor is connected to the feedback with a resistor across the output.



Video Content / Details of website for further learning (if any):

https://www.youtube.com/watch?v=uyOfonR_rEw

Important Books/Journals for further learning including the page nos.:

Linear Integrated Circuits Sixth Edition Ganesh Babu T.R,Suseela B,SCITECH Publication
"Understanding Single-Ended, Pseudo-Differential and Fully-Differential ADC Inputs". Maxim Application Note 1108. Archived from the original on 2007-06-26. Retrieved November 10, 2007.

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LECTURE HANDOUTS

MDE

II / IV

Course Name with Code : 19MDC04 – LOGIC CIRCUITS FOR CLINICAL ENGINEERS

Course Faculty : Mrs.M.Birunda

Unit : II - Characteristics of OP Amp and Applications

Date of Lecture:

Topic of Lecture: Applications: Closed Loop Op Amp Configuration

Introduction :

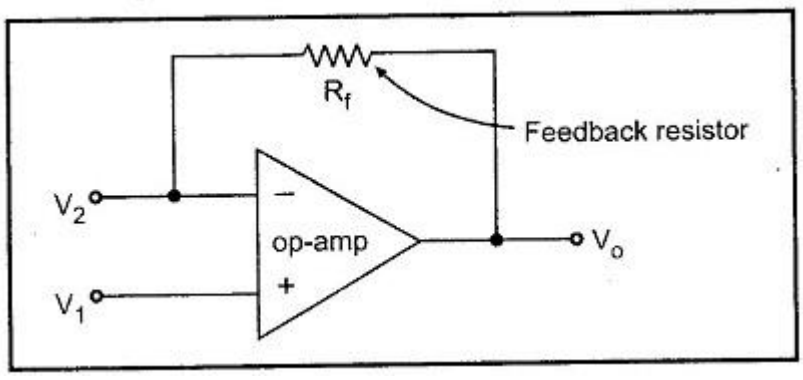
In this configuration, the input voltage signal, (VIN) is applied directly to the non-inverting (+) input terminal which means that the output gain of the amplifier becomes "Positive" in value in contrast to the "Inverting Amplifier" circuit whose output gain is negative in value. The result of this is that the output signal is "in-phase" with the input signal.

Prerequisite knowledge for Complete understanding and learning of Topic:

Operational Amplifier

Closed Loop Op Amp Configuration:

- The op-amp can be effectively utilized in linear applications by providing a feedback from the output to the input, either directly or through another network.
- If the signal feedback is out- of-phase by 1800 with respect to the input, then the feedback is referred to as negative feedback or degenerative feedback.
- Conversely, if the feedback signal is in phase with that at the input, then the feedback is referred to as positive feedback or regenerative feedback



Video Content / Details of website for further learning (if any):

https://www.youtube.com/watch?v=uyOfonR_rEw

Important Books/Journals for further learning including the page nos.:

- Linear Integrated Circuits Sixth Edition Ganesh Babu T.R, Suseela B, SCITECH Publication

- Programmable OP-AMP Configurations Mayuresh Sardar, Dept. of Electronics and Tele Communication Engineering, Vishwakarma Institute of Information Technology, International Research Journal of Engineering and Technology (IRJET), Volume: 03 Issue: 10 | Oct -2016

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LECTURE HANDOUTS

L 13

MDE

II / IV

Course Name with Code : 19MDC04 – LOGIC CIRCUITS FOR CLINICAL ENGINEERS

Course Faculty : Mrs.M.Birunda

Unit : II - Characteristics of OP Amp and Applications

Date of Lecture:

Topic of Lecture: Inverting and Non inverting Amplifiers, Inverters

Introduction :

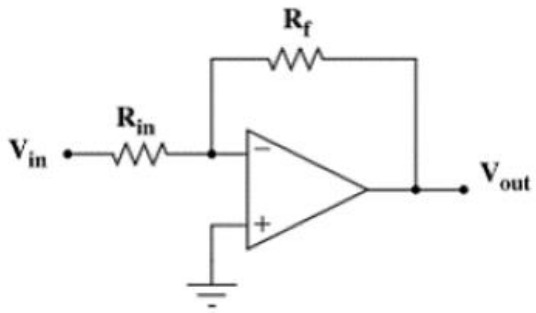
In this configuration, the input voltage signal, (VIN) is applied directly to the non-inverting (+) input terminal which means that the output gain of the amplifier becomes "Positive" in value in contrast to the "Inverting Amplifier" circuit whose output gain is negative in value. The result of this is that the output signal is "in-phase" with the input signal.

Prerequisite knowledge for Complete understanding and learning of Topic:

Operational Amplifier

Inverting Amplifier:

The output voltage V0 is feedback to the inverting input terminal through Rf – R1 network where Rf is the feedback resistor. Input signal is applied to the inverting input through R1and non-inverting input terminal is grounded.



Analysis:

For simplicity assume an ideal op-amp for analysis. As Vd = 0, node'a' is at ground potential an the current i1 through R1 is

$$i1 = Vi / R1$$

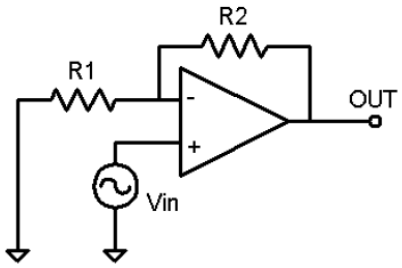
Since op-amp draws no current all the current flowing through R1must flow through Rf. Therefore Output voltage ,

$$V0 = -i1Rf = -ViRf / R1$$

$$\text{Gain ACL} = V0/Vi = -Rf/R1$$

Negative sign indicates a phase shift of 1800 between Vi and V0. R1 should be kept fairly large to avoid loading effect.

Non-inverting Amplifier:



Here the signal is applied to the positive input terminal and feedback is given; the circuit amplifies without inverting the input signal hence it is called non-inverting amplifier.
The voltage at node 'a' is Vi.

$$Vi = (V0/R1+Rf).R1$$
$$V0/Vi = (Ri+Rf)/R1 = 1+Rf/R1$$
$$\text{i.e. } ACL = 1+Rf/R1$$

The gain can be adjusted to unity or more by proper seletion of resistors Rf and R1.
Comparing with inverting amplifier the input resistance Ri is extremely large.

Inverter

An inverter can be defined as it is a compact and rectangular shaped electrical equipment used to convert direct current (DC) voltage to alternating current (AC) voltage in common appliances. Direct current is used in many of the small electrical equipment such as solar power systems, power batteries, power-sources, fuel cells because these are simply produced direct current.

These devices are standalone devices for some applications like solar power. There are different types of inverters available in the market based on the switching waveform shape. An inverter uses DC power sources to provide an AC voltage to giving the supply to the electronic as well as electrical equipment.

Working of Inverter

The working of an inverter is, it converts DC to AC, and these devices never generate any kind of power because the power is generated by the DC source. In some situations like when the DC voltage is low then we cannot use the low DC voltage in a home appliance. So due to this reason, an inverter can be used whenever we utilize solar power panel.

Video Content / Details of website for further learning (if any):
https://www.youtube.com/watch?v=uyOfonR_rEw

Important Books/Journals for further learning including the page nos.:
Linear Integrated Circuits Sixth Edition Ganesh Babu T.R,Suseela B,SCITECH Publication
Programmable OP-AMP Configurations Mayuresh Sardar, Dept. of Electronics and Tele Communication Engineering, Vishwakarma Institute of Information Technology, International Research Journal of Engineering and Technology (IRJET), Volume: 03 Issue: 10 | Oct -2016

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MDE | **II / IV**

Course Name with Code : 19MDC04 – LOGIC CIRCUITS FOR CLINICAL ENGINEERS

Course Faculty : Mrs.M.Birunda

Unit : II - Characteristics of OP Amp and Applications

Date of Lecture:

Topic of Lecture: Voltage Follower, Summing Amplifier, Averaging Circuits - Subtractor

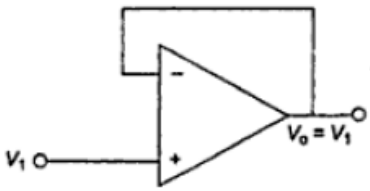
Introduction :

An op-amp based adder produces an output equal to the sum of the input voltages applied at its inverting terminal. It is also called as a summing amplifier, since the output is an amplified one. In the above circuit, the non-inverting input terminal of the op-amp is connected to ground.

Prerequisite knowledge for Complete understanding and learning of Topic:

Operational Amplifier, Differential Amplifier

Voltage follower:



The output voltage follows the input voltage exactly hence the circuit is called a voltage follower. Voltage follower is obtained from the non-inverting amplifier if Rf = 0 and R1 = ∞.

V0 = Vi

Voltage follower is used as buffer for impedance matching. i.e. to connect a high impedance source to a low impedance load.

Summing Amplifier Circuit:

Figure shows an Summing Amplifier Circuit in inverting configuration with three inputs Va, Vb, Vc. Depending on the relation between Ra, Rb, Rc and RF, the circuit can be used as a Summing amplifier, Scaling amplifer or Average ampli-fier.

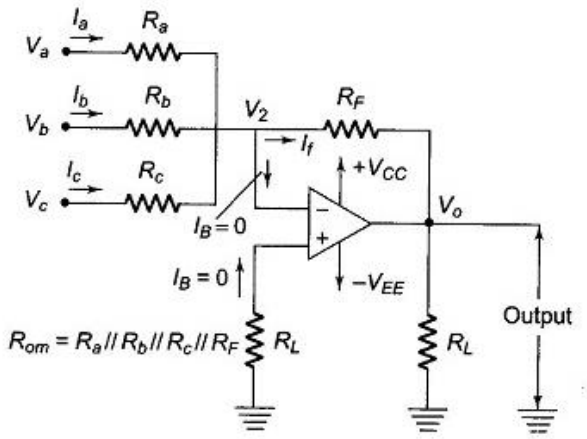


Fig. Summing Amplifier (3 Input Inverting Configuration)

Using Kirchoff's circuit equation, we have la + lb+ lc= IB + If. But IB ≡ 0 and V1 ≡ V2 ≡ 0

Therefore

$$I_a + I_b + I_c = I_f$$

$$\frac{V_a}{R_a} + \frac{V_b}{R_b} + \frac{V_c}{R_c} = -\frac{V_o}{R_F}$$

$$R_a = R_b = R_c$$

$$V_o = -\frac{R_F}{R_a}(V_a + V_b + V_c)$$

In this circuit Ra = Rb = Rc = RF. Therefore Vo = — (Va + Vb + Vc). (14.7) Hence the output voltage is the negative sum of all the input voltages. If each input voltages is amplified by a different factor, i.e. weighted differently at the output, the circuit is called a scaling or weighted amplifier. The condition can be obtained by making Ra, Rb, and Rc, different in value. The output voltage of the scaling amplifier is then

$$V_o = -\left(\frac{R_F}{R_a}V_a + \frac{R_F}{R_b}V_b + \frac{R_F}{R_c}V_c\right)$$

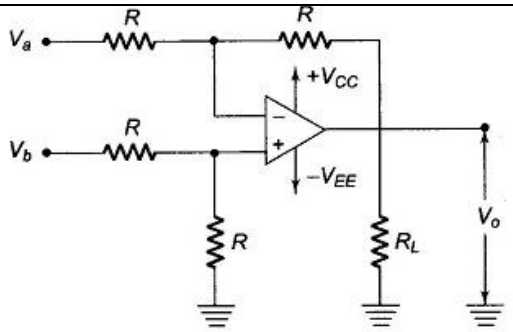
where $R_F/R_a \neq R_F/R_b \neq R_F/R_c$.

In this amplifier, the output voltage is the average value of the input voltages. This modification can be obtained by making Ra = Rb = Rc. = R. Also, the gain by which input is amplified must be equal to 1 over the number of inputs, i.e. RF/R = 1/n where n is the number of inputs. Therefore the output voltage is given by Vo = Va + Vb + Vc. Therefore the output voltage for three inputs is RF/R = 1/3. The output volt-age is given by

$$V_o = -\frac{V_a + V_b + V_c}{3}$$

Subtractor

A subtractor circuit using a basic differential amplifier is as shown in Fig.



Subtractor Using OpAmp

By selecting the appropriate values for the external resistance, the input signal can be scaled (attenuated) to the desired value. If this is done, the circuit is referred to as a scaling amplifier.

As in Fig., all values of the external resistance are equal, and the gain of the amplifier is unity.

Therefore, the output voltage of differential amplifier with unity gain is

$$V_o = -\frac{R}{R}[V_a - V_b]$$

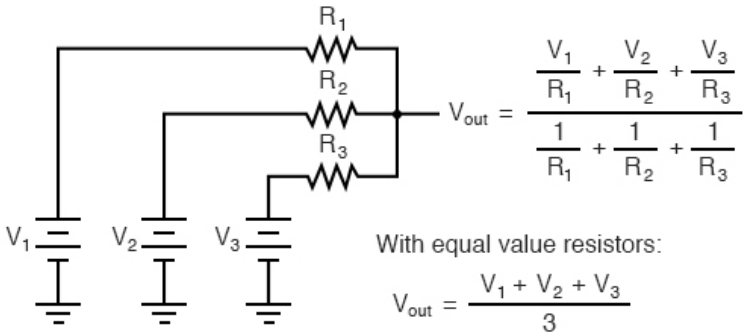
$$V_o = -[V_a - V_b]$$

Hence the circuit is called a subtractor.

Averaging Amplifier

An Averaging Amplifier is a variation of a Summing Amplifier. The input resistors must all be the same –in this case they are all set to 100 kΩ. The feedback resistor is selected so that its value of the value of RF divided by the number of inputs. So RF = 100 kΩ/4 = 25 kΩ

"Passive Averager" Circuit



Video Content / Details of website for further learning (if any):

https://www.youtube.com/watch?v=3RRSR6SByz4

Important Books/Journals for further learning including the page nos.:

Linear Integrated Circuits Sixth Edition Ganesh Babu T.R,Suseela B,SCITECH Publication

Paul Horowitz and Winfield Hill, The Art of Electronics. 2nd ed. Cambridge University Press, Cambridge, 1989 ISBN 0-521-37095-7

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MDE

II / IV

Course Name with Code : 19MDC04 – LOGIC CIRCUITS FOR CLINICAL ENGINEERS

Course Faculty : Mrs.M.Birunda

Unit : II - Characteristics of OP Amp and Applications

Date of Lecture:

Topic of Lecture: Differential Amplifier, Multiplier, Differentiator

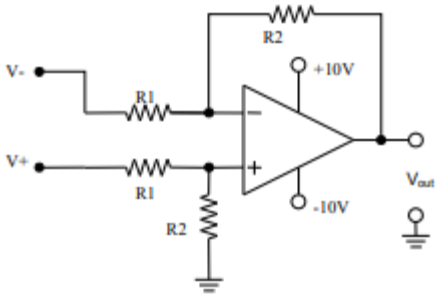
Introduction :

A differential amplifier is a type of electronic amplifier that amplifies the difference between two input voltages but suppresses any voltage common to the two inputs. Differentiator or Differentiation amplifier is a circuit which performs mathematical operation of differentiation. i.e., the output waveform is the derivative of the input waveform.

Prerequisite knowledge for Complete understanding and learning of Topic:

Operational Amplifier, Differential Amplifier

Differential Amplifier



Applying KCL,

$$\frac{V_2 - V_X}{R_1} = \frac{V_X - 0}{R_2}$$

$$\therefore \frac{V_2}{R_1} = \frac{V_X}{R_1} + \frac{V_X}{R_2}$$

$$\frac{V_2}{R_1} = V_X\left[\frac{1}{R_1} + \frac{1}{R_2}\right]$$

$$V_X = V_Y$$

$$V_X = \frac{V_2}{R_1\left[\frac{1}{R_1} + \frac{1}{R_2}\right]} = \frac{V_2}{\left(1 + \frac{R_1}{R_2}\right)}$$

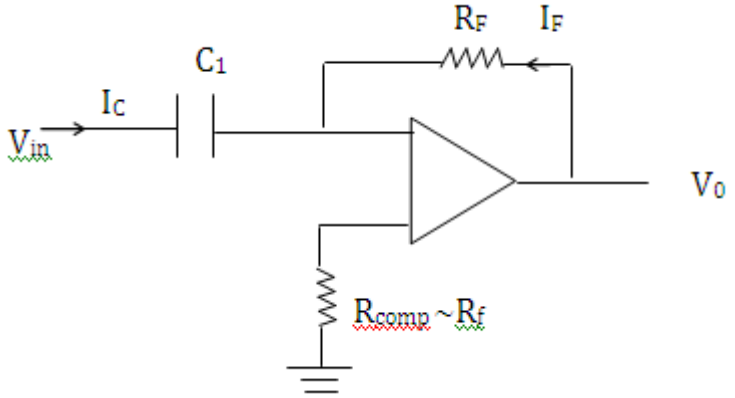
Similarly Vy

$$V_1 = V_Y\left[1+\frac{R_1}{R_2}\right] - V_0\frac{R_1}{R_2}$$

$$V_1 = \frac{V_2}{1+\frac{R_1}{R_2}}\left[1+\frac{R_1}{R_2}\right] - V_0\frac{R_1}{R_2}$$

$$V_0 = \frac{R_2}{R_1}[V_2 - V_1]$$

Ideal Differentiator



The node A is at virtual ground i.e., VA= 0

The current through capacitor is $I_C = C_1\left[\frac{d}{dt}(v_{iA} - V_A)\right] = C_1.\frac{d.Vin}{dt}$ -------- (1)

The circuit iF though RF is given by

$$I_F = \frac{V_0 - V_A}{R_F} = \frac{V_0}{R_F}$$ ---------- (2) since $V_A = 0$

At node A, by KCL (i.e) equations (1) + (2)

$$I_C + I_F = 0$$

$$\Rightarrow C_1\frac{d.V_{in}}{dt} + \frac{V_0}{R_F} = 0$$

$$C_1\frac{d.V_{in}}{dt} = -\frac{V_0}{R_F}$$

$\Rightarrow$ $\boxed{V_0 = -R_F.C_1.\frac{d.V_{in}}{dt}}$ ---------- (A)

Thus the outputvoltage,V0 is (-RFC1) times the derivative of input voltage Vin. The minus indicates phase shift of 180^o between i/p signals.

Writing equation (A) in frequency domain, we get

$$V_0(s) = -R_F C_1.S.V_{IN}(S)$$

Now gain 'A' of the differentiator is

$$|A| = \left|\frac{V_0(s)}{V_{in}(s)}\right| = |-SR_F.C_1| = |-j\omega.R_F.C_1| = \omega.R_F.C_1$$

(s = jω , ω = 2πf)

$$\therefore |A| = 2\pi f.R_F C_1 = \frac{f}{fa}$$

Where

$$\boxed{fa = \frac{1}{2\pi R_F C_1}}$$

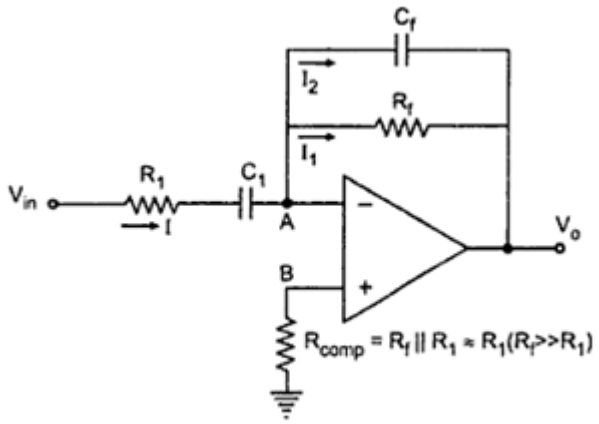
At f=fa, $|A| = 1$, i.e 0 dB and gain increases at a rate of +20dB/decade.

Demerits

The i/p impedance (1/ωC1) decreases with increase in frequency, thereby making the circuit sensitive to high frequency noise.

Also, at high frequencies, the circuit becomes unstable and enters into oscillation.

Practical Differentiator



Practical differentiator circuit

Both stability and high frequency noise problems can be corrected by adding two components, R1 & CF as shown in above circuit. The transfer function of this circuit is

$$\frac{V_0(s)}{V_{in}(s)} = \frac{-Z_f}{Z_i} = \frac{-SR_F C_1}{(1+SR_1C_1)(1+SR_F C_F)}$$

For R1C1 = RFCF,

$$|A| = \left|\frac{V_0(s)}{V_{in}(s)}\right| = \frac{-sR_F C_1}{(1+sR_1C_1)^2} = \frac{-sR_F.C_1}{\left(1+j\frac{f}{fb}\right)^2}$$

where

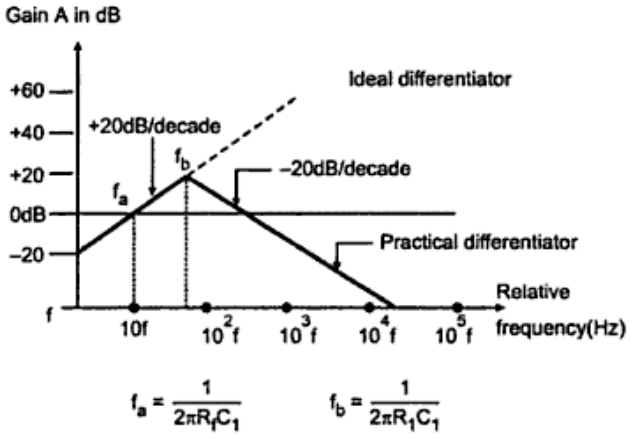
$$f_b = \frac{1}{2\pi R_1 C_1} = \frac{1}{2\pi R_F C_F}$$

Frequency response

fa is the frequency at which gain is 0 dB.

fb is the gain limiting frequency

fC is the unity gain bandwidth of Op-Amp.



Frequency response of the practical differentiator

From fa to fb gain increases at rate of +20db/decade.

After fb the gain decreases at -20dB/decade.

This change in gain is caused by R1C1 & RFCF combinations.

The value of fb should be selected such that

$$f_a < f_b < f_c$$

For good differentiation, the time period T of input signal is

$$T \geq RFC1.$$

APPLICATIONS:

In wave shaping circuits to detect high frequency components in input signal.
As Rate of change detector in FM Modulator.

Video Content / Details of website for further learning (if any):

https://www.youtube.com/watch?v=-KxxD68sra0

Important Books/Journals for further learning including the page nos.:

Linear Integrated Circuits Sixth Edition Ganesh Babu T.R,Suseela B,SCITECH Publication
Paul Horowitz and Winfield Hill, The Art of Electronics. 2nd ed. Cambridge University Press, Cambridge, 1989 ISBN 0-521-37095-7
A novel differential differentiator, M.A. Al-Alaoui, IEEE Transactions on Instrumentation and Measurement.

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LECTURE HANDOUTS

L 16

MDE

II / IV

Course Name with Code : 19MDC04 – LOGIC CIRCUITS FOR CLINICAL ENGINEERS

Course Faculty : Mrs.M.Birunda

Unit : II - Characteristics of OP Amp and Applications

Date of Lecture:

Topic of Lecture: Integrator

Introduction :

A circuit in which the output voltage wave is the integral of the input voltage waveform is the **Integrator** or **Integration Amplifier.**

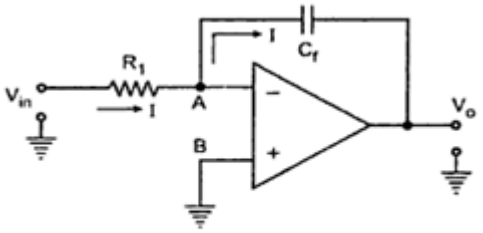
Replacing the feedback resistor Rf of the amplifier in the inverting mode by a capacitor.

Prerequisite knowledge for Complete understanding and learning of Topic:

Integrator

Integrator

A circuit in which the output voltage wave is the integral of the input voltage waveform is the **Integrator** or **Integration Amplifier.**



Op-amp Integrator

Ideal Integrator

The nodal equation at node A is,

$$\frac{V_{in}-V_A}{R_1}+C_F\frac{d(V_0-V_A)}{dt}=0$$

Since node A is at virtual ground, $V_A = 0$

$$\Rightarrow \frac{V_{in}}{R_1}+C_F\frac{dV_0}{dt}=0$$

$$\Rightarrow \frac{dV_0}{dt}=-\frac{1}{R_1C_F}V_{in}$$

Integrating on both sides we get,

$$V_0=-\frac{1}{R_1C_F}\int_0^t V_{in}dt+C \qquad \text{---------- (A)}$$

Where, C is the integration constant. Thus the output voltage is directly proportional to negative integral of input voltage and inversely proportional to time constant R_1C_F.

In Op-amp integrator the effective input capacitance by Millers theorem is $C_f(1-A_v)$. Where, $A_V \rightarrow$ gain of the Op - Amp

Gain A_V is infinite for ideal Op-Amp, so effective time of Op-amp becomes large which results in perfect integration.

The equation (A) written in phasor notation,

$$V_0(s) = -\frac{1}{sR_1C_F}.V_{IN}(s)$$

In steady state, s = jω

$$\rightarrow |A| = \left|\frac{V_0(s)}{V_{in}(s)}\right| = \left|\frac{-1}{SR_1C_F}\right| = \left|\frac{1}{-j\omega R_1C_F}\right|$$

$$\Rightarrow |A| = \frac{1}{\omega R_1C_F}$$

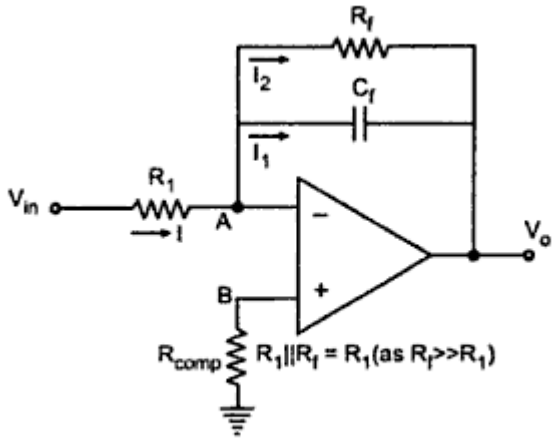
$$\boxed{\therefore |A| = \frac{f_b}{f}} \quad \text{where,} \quad f_b = \frac{1}{2\pi R_1C_F}$$

Where $f_{b\ is}$ the frequency where gain is 0dB.

Errors in ideal integrator

- At low frequencies (ω≅~0), the gain becomes infinite (saturates).
- Input offset voltage gets amplified and appears as error voltage which causes saturation.
- It is difficult to pull integrator out of saturation; hence perfect integration is not possible.
- Limited bandwidth.

Practical integrator



Practical integrator circuit

The demerits of ideal circuit are overcome by practical integrator circuit, in which feedback resistor R_F is connected across C_F. It reduces the low frequency gain of the Op-Amp. It is also called **Lossy Integrator.**

Nodal equation at node A gives,

$$\frac{V_{in}(s)}{R_1} + sC_FV_0(S) + \frac{V_0(s)}{R_F} = 0$$

$$\Rightarrow V_0(s) = -\left(\frac{1}{sR_1C_F + \frac{R_1}{R_F}}\right).V_{in}(s)$$

$$\Rightarrow \frac{V_0(s)}{V_{in}(s)} = -\frac{-R_F/R_1}{1+sR_FC_F}$$

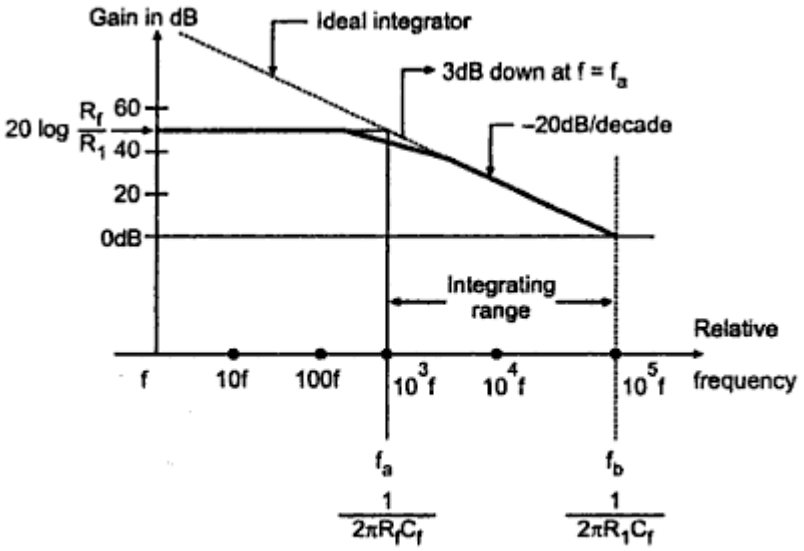
Put s = jω ,

$$\Rightarrow |A| = \left|\frac{V_0(j\omega)}{V_{in}(j\omega)}\right| = \left|\frac{-R_F/R_1}{1+j\omega R_F C_F}\right| = \left|\frac{-R_F/R_1}{1+j2\pi f R_F C_F}\right|$$

$$\therefore |A| = \frac{-R_F/R_1}{\left|1+j\frac{f}{fa}\right|}$$

Where,

$f_a = \frac{1}{2\pi R_F C_F}$, is the break frequency at which gain is (0.707) R_F/R_1



Frequency response of the practical integrator

- The value of f_a is selected such that $f_a < f_b$
- f_b, the input frequency should be 10 times. f_a. i.e $f_b = 10\ f_a$.
- For perfect integration, time period T of input signal should be, $T \geq R_F C_F$.

Applications:

1. Analog computers, ADC's
2. Wave shaping circuits.
3. Ramp generators.

Video Content / Details of website for further learning (if any):
https://www.youtube.com/watch?v=vOOjcrbY0LQ

Important Books/Journals for further learning including the page nos.:
Linear Integrated Circuits Sixth Edition Ganesh Babu T.R,Suseela B,SCITECH Publication
Wideband Differentiator and Integrator With Ideal Phase Response,Jayalaxmi Devate ; S. Y. Kulkarni ; K. R. Pai, IEEE Transactions on Instrumentation and Measurement.

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L 17

LECTURE HANDOUTS

MDE

II / IV

Course Name with Code : 19MDC04 – LOGIC CIRCUITS FOR CLINICAL ENGINEERS

Course Faculty : Mrs.M.Birunda

Unit : II - Characteristics of OP Amp and Applications

Date of Lecture:

Topic of Lecture: Instrumentation Amplifier

Introduction :

A differential amplifier is a type of electronic amplifier that amplifies the difference between two input voltages but suppresses any voltage common to the two inputs.

Prerequisite knowledge for Complete understanding and learning of Topic:

Operational Amplifier, Differential Amplifier

Instrumentation Amplifier

1. It constructed using three Op-Amps as shown in Fig
2. Op-Amps A1 and A2 are connected basically, in noninverting amplifier configuration.
3. The only change is that instead of grounding inverting terminals of both Op-Amps as in noninverting configuration), they are connected to resistor RG
4. Effectively, the inverting terminals of Op-Amp A1 is fed a voltage Vl through RG and the inverting terminal of Op-Amp A2 is fed by a voltage V2 through RG. This is obvious by virtual ground concept.

Derivation for Output Voltage

As per the superposition theorem, the output of A1 (Vo′)and A2 (Vo′′) is given below

$$V_o' = \left(1 + \frac{R_2}{R_G}\right) V_1 - \frac{R_2}{R_G} V_2$$

$$V_o'' = \left(1 + \frac{R_2}{R_G}\right) V_2 - \frac{R_2}{R_G} V_1$$

The output of two op-amps (A1 and A2) are applied to the input of differential amplifier. Therefore, the final output of the instrumentation amplifier is written as follows

$$\text{Output } V_o = \frac{R_f}{R_1}(V_o'' - V_o')$$

$$V_o = \frac{R_f}{R_1}\left(\left(\left(1+\frac{R_2}{R_G}\right)V_2 - \frac{R_2}{R_G}V_1\right) - \left(1+\frac{R_2}{R_G}\right)V_1 + \frac{R_2}{R_G}V_2\right)$$

$$= \frac{R_f}{R_1}\left(\left(\left(1+\frac{R_2}{R_G}\right)(V_2 - V_1) + \frac{R_2}{R_G}(V_2 - V_1)\right)\right)$$

$$= \frac{R_f}{R_1}(V_2 - V_1)\left(\left(1+\frac{R_2}{R_G}\right) + \frac{R_2}{R_G}\right)$$

Video Content / Details of website for further learning (if any):
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LECTURE HANDOUTS

MDE

II / IV

Course Name with Code : 19MDC04 – LOGIC CIRCUITS FOR CLINICAL ENGINEERS

Course Faculty : Mrs.M.Birunda

Unit : II - Characteristics of OP Amp and Applications

Date of Lecture:

Topic of Lecture: Precision rectifier, V/I & I/V Converter

Introduction :

The precision rectifier, also known as a super diode, is a configuration obtained with an operational amplifier in order to have a circuit behave like an ideal diode and rectifier. It is very useful for high-precision signal processing.

The circuits in instrumentation for analog representation of certain physical quantities (weight, pressure, motion etc), DC current is preferred.

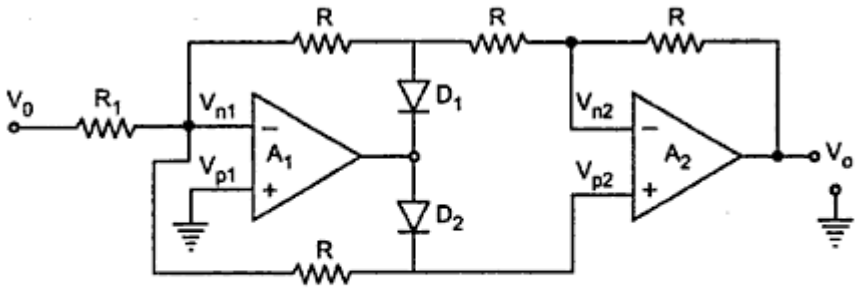
This is because DC current signals will be constant throughout the circuit in series from the source to the load.

The current sensing instruments also have the advantage of less noise. So, sometimes it is essential to create current which is corresponding or proportional to a definite voltage. For this purpose Voltage to Current Converters are used.

Prerequisite knowledge for Complete understanding and learning of Topic:

Precision rectifier, Voltage to current convertor, current to voltage convertor

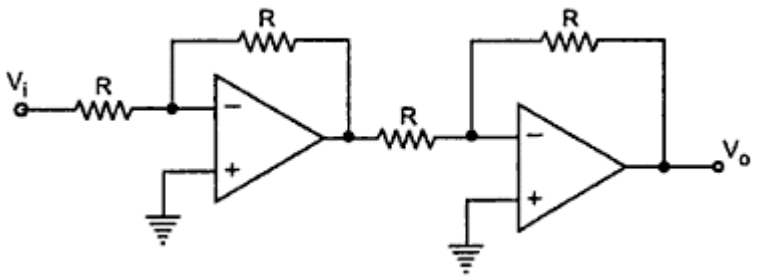
Precision rectifier



Full wave rectifier

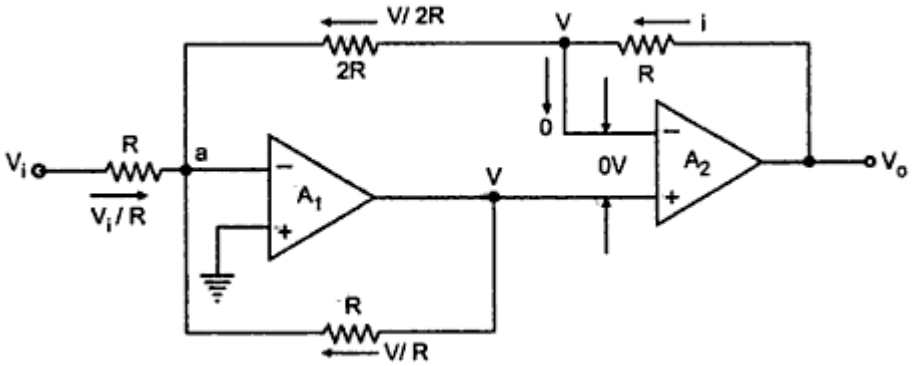
- Full Wave rectifier accepts a.c input signal, inverts either positive or negative half and delivers both the inverted and non-inverted halves at the output.
- For positive inputs ($V_i > 0$), diode D_1 is ON and D_2 is OFF. Both the Op-amps $A_1$and A_2 acts as inverters. So the output is $V_0 = V_i$.

Equivalent ckt. For $V_i > 0$.



- For negative inputs i.e (V_i < 0V), diode D_1 is OFF and D_2 is ON.

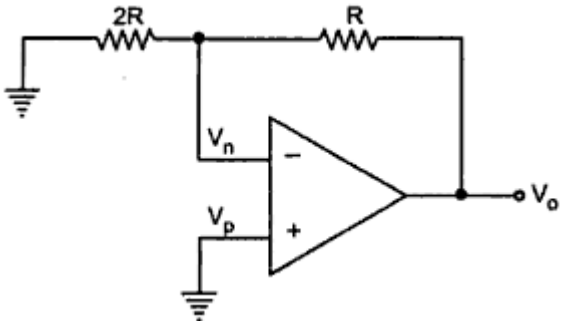
Equivalent ckt. For V_i < 0.



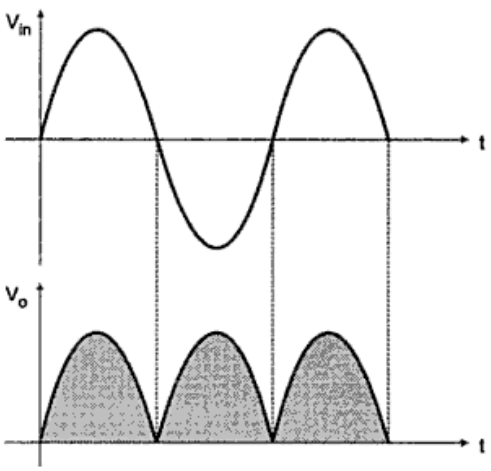
- Let the output voltage of A_2 be V. Since differential input of A_2 is zero, input to (-) terminal is also V.

  KCL at node 'a' gives

  Equivalent circuit is a non-inverting amplifier as shown below



Input and Output Waveforms:



Input and output waveforms for full wave rectifier

$$\frac{V_i}{R}+\frac{v}{R}+\frac{V}{2R}=0 \qquad \text{---------- (1)}$$

$$\Rightarrow \frac{2v_i+2v+v}{2R}=0$$

$$\Rightarrow 2v_i=-3V$$

$$\therefore v=\frac{-2}{3}v_i \qquad \text{---------- (2)}$$

- Hence output voltage, V_0 is given as,

$$v_0=\left(1+\frac{R}{2R}\right)\left(\frac{-2}{3}v_i\right)=-v_i$$

$$\Rightarrow \boxed{v_0=-v_i} \qquad \text{---------- (A)}$$

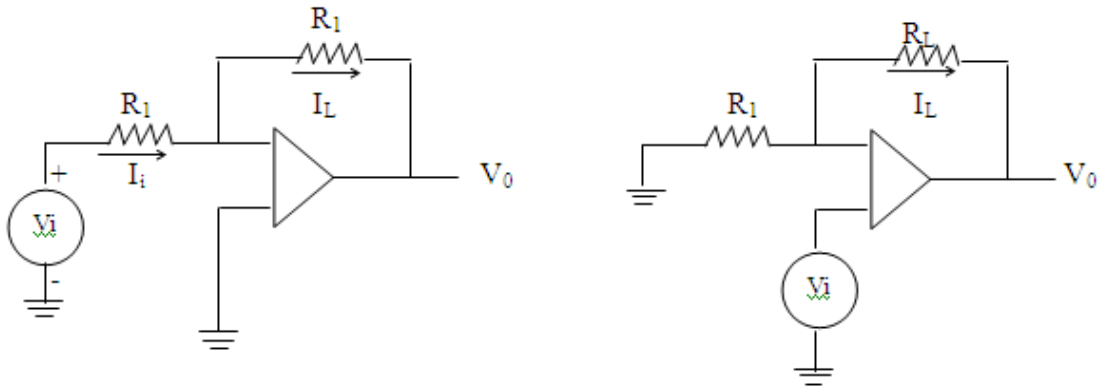
- So for negative input, the output is positive.

V to I Converter

- The voltage to current converter is a circuit the output load current is proportional to the input voltage.
- According to connection of load, there are two types,

  i. Floating load. ii. Grounded load.

Floating Load V-I Converter



- As the input current to an Op-Amp is zero,

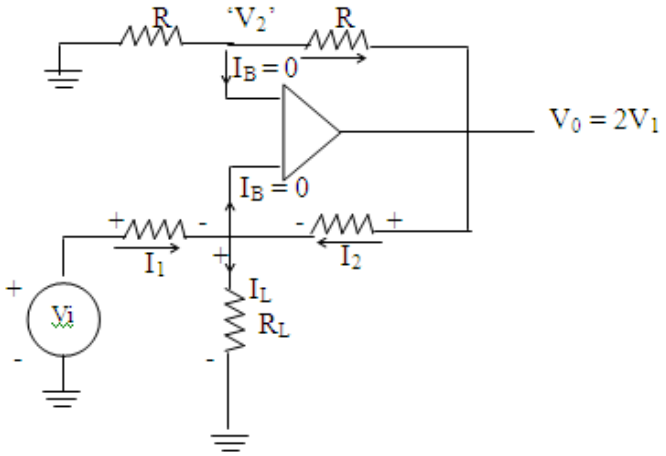
$$I_L=I_i=\frac{V_i}{R_1}$$

$$\Rightarrow \boxed{I_L \alpha\, V_i}$$

- Thus the load current is proportional to input voltage and the circuit acts as a voltage to current converter.
- If the load is a capacitor, it charges and discharges at a constant rate. Such converters are used to generate Saw tooth or triangular waveforms.
- The proportionality constant is generally $1/R_1$. Hence the circuit is called Transconductance amplifier. It is also called voltage controlled current source. (VCCS).

- The load current, $I_L = V_i/R_1$ is same for all types of loads. Load can be linear (e.g Resistor), or non-linear (e.g LED) or it can have time dependent.
- No matter what the load is, the Op-amp will draw the current I_i whose magnitude depends only Vi and R.

Grounded Load V – I Converter:



- When one end of the load is grounded, it is called grounded V-I converter. The circuit is also called as HOWLAND CURRENT CONVERTER.
- Applying KCL at node, V_1

$$I_1 + I_2 = I_L$$

$$\Rightarrow \frac{V_i - V_1}{R} + \frac{V_0 - V_1}{R} = I_L$$

$$\Rightarrow V_i + V_0 - 2V_1 = I_L.R$$

$$\therefore V_i = \frac{V_i + V_0 - I_L.R}{2} \qquad \text{---------- (1)}$$

The gain of an Op-Amp in non- inverting mode is given as,

$$A_{CL} = 1 + \frac{R_F}{R_1} \qquad \text{---------- (2)}$$

For this circuit, $R_f = R_1 = R$,

$$\therefore A_{CL} = 1 + \frac{R}{R} = 2$$

$$\therefore A_{CL} = \frac{V_0}{V_1} = 2$$

$$\Rightarrow V_0 = 2V_1 \qquad \text{---------- (3)}$$

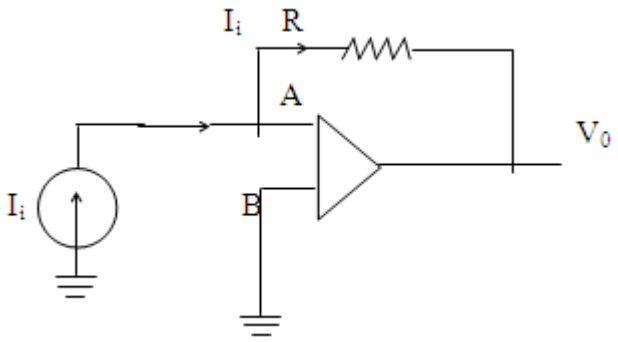
$$= V_1 + V_0 - I_L.R \qquad \text{From equation (1)}$$

$$\Rightarrow V_i = I_L R \qquad \text{---------- (A)}$$

$$\boxed{I_L \alpha V_i} \qquad \text{---------- (B)}$$

- Hence the load current depends on input voltage V_i and resistor R.

I to V Converter



- The circuit in which the output voltage is proportional to input current is called current to voltage converter. Consider, input current I_i and output voltage V_0, then

$$V_0 = A.I_i \qquad (1)$$

Where, A $\rightarrow$ Gain of the circuit.

- As we measure gain in ohms it is appropriate to denote gain by R. Hence I-V converter is also called as Transresistance amplifier.
- Node B is grounded. Hence node A is at virtual ground.

$$\therefore V_A = 0$$

$$\Rightarrow I_i = \frac{V_A - V_0}{R} = \frac{-V_0}{R}$$

$$\Rightarrow V_0 - R.I_i$$

$$\Rightarrow \boxed{V_0 \alpha R.I_i}$$

- Here the output voltage (V_0) is proportional to input current (I_i), therefore the circuit is a current to voltage converter.
- The circuit is also called as current controlled voltage source [CCVS].
- It the resistance in the circuit is replaced with impedance Z, the circuit is called Trans impedance Amplifier.

Video Content / Details of website for further learning (if any):
https://www.youtube.com/watch?v=5HweBajP-5g

Important Books/Journals for further learning including the page nos.:
Linear Integrated Circuits Sixth Edition Ganesh Babu T.R,Suseela B,SCITECH Publication
New precision rectifier circuits with high accuracy and wide bandwidth,S. J. G. Gift ,Pages 601-617 | Received 16 Sep 2003, Accepted 30 Mar 2005, Published online: 19 Aug 2006

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L 19

LECTURE HANDOUTS

MDE

II / IV

Course Name with Code : 19MDC04 – LOGIC CIRCUITS FOR CLINICAL ENGINEERS

Course Faculty : Mrs.M.Birunda

Unit : III – Comparator and Waveform Generators

Date of Lecture:

Topic of Lecture: Comparators, open loop Op Amp configuration

Introduction :

A **comparator** is an electronic circuit, which compares the two inputs that are applied to it and produces an output. The output value of the comparator indicates which of the inputs is greater or lesser. Please note that comparator falls under non-linear applications of ICs.

Prerequisite knowledge for Complete understanding and learning of Topic:

Operation of Op Amp, Basic Analog electronics and Electronic Devices, and Circuit theory

Comparators, open loop Op Amp configuration:

A **comparator** is an electronic circuit, which compares the two inputs that are applied to it and produces an output. The output value of the comparator indicates which of the inputs is greater or lesser. Please note that comparator falls under non-linear applications of ICs.

An op-amp consists of two input terminals and hence an op-amp based comparator compares the two inputs that are applied to it and produces the result of comparison as the output. This chapter discusses about **op-amp based comparators**.

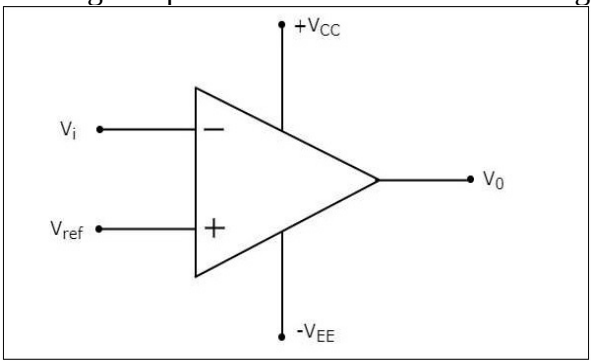
Types of Comparators

Comparators are of two types : **Inverting** and **Non-inverting**. This section discusses about these two types in detail.

Inverting Comparator

An **inverting comparator** is an op-amp based comparator for which a reference voltage is applied to its non-inverting terminal and the input voltage is applied to its inverting terminal. This comparator is called as **inverting** comparator because the input voltage, which has to be compared is applied to the inverting terminal of op-amp.

The **circuit diagram** of an inverting comparator is shown in the following figure.



The **operation** of an inverting comparator is very simple. It produces one of the two values, +Vsat+Vsat and −Vsat−Vsat at the output based on the values of its input voltage ViVi and

the reference voltage VrefVref.

- The output value of an inverting comparator will be −Vsat−Vsat, for which the input ViVi voltage is greater than the reference voltage VrefVref.
- The output value of an inverting comparator will be +Vsat+Vsat, for which the input ViVi is less than the reference voltage VrefVref.

Video Content / Details of website for further learning (if any):
https://www.youtube.com/watch?v=fWN17g-JGro

Important Books/Journals for further learning including the page nos.:

Linear Integrated Circuits By D. Roy Choudhury, Shail B. Jain T1

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L 20

LECTURE HANDOUTS

MDE

II / IV

Course Name with Code : 19MDC04 – LOGIC CIRCUITS FOR CLINICAL ENGINEERS

Course Faculty : Mrs.M.Birunda

Unit : III – Comparator and Waveform Generators

Date of Lecture:

Topic of Lecture: Inverting, Non-inverting Comparators

Introduction :

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Prerequisite knowledge for Complete understanding and learning of Topic:

Operation of Op Amp, Basic Analog electronics and Electronic Devices, and Circuit theory

Inverting, Non-inverting Comparators

Types of Comparators

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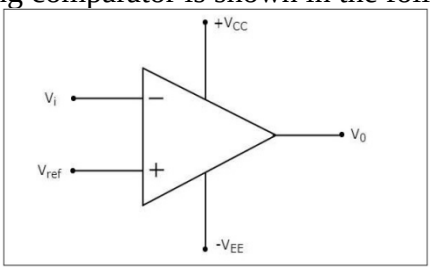
The **circuit diagram** of an inverting comparator is shown in the following figure.



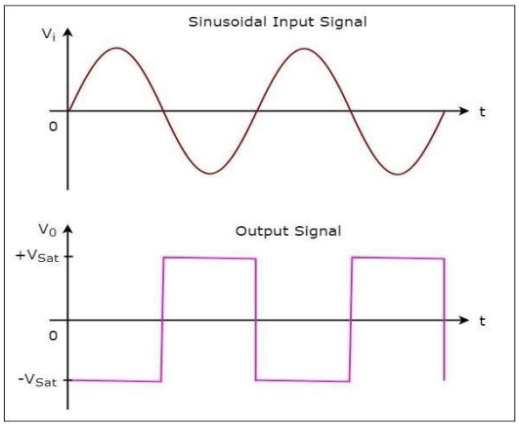
The **operation** of an inverting comparator is very simple. It produces one of the two values, +Vsat+Vsat and −Vsat−Vsat at the output based on the values of its input voltage ViVi and the reference voltage VrefVref.

- The output value of an inverting comparator will be −Vsat−Vsat, for which the input ViVi voltage is greater than the reference voltage VrefVref.
- The output value of an inverting comparator will be +Vsat+Vsat, for which the input ViVi is less than the reference voltage VrefVref.

The **operation** of the inverting comparator shown above is discussed below −

- During the **positive half cycle** of the sinusoidal input signal, the voltage present at the inverting terminal of op-amp is greater than zero volts. Hence, the output value of the inverting comparator will be equal to −Vsat−Vsat during positive half cycle of the sinusoidal input signal.
- Similarly, during the **negative half cycle** of the sinusoidal input signal, the voltage present at the inverting terminal of the op-amp is less than zero volts. Hence, the output value of the inverting comparator will be equal to +Vsat+Vsat during negative half cycle of the sinusoidal input signal.

The following figure shows the **input and output waveforms** of an inverting comparator, when the reference voltage is zero volts.

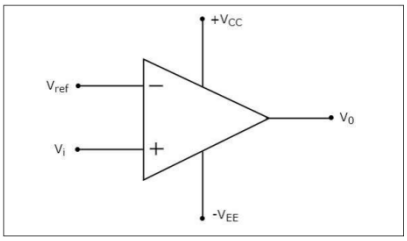


In the figure shown above, we can observe that the output transitions either from −Vsat−Vsat to +Vsat+Vsat or from +Vsat+Vsat to −Vsat−Vsat whenever the sinusoidal input signal is crossing zero volts. In other words, output changes its value when the input is crossing zero volts. Hence, the above circuit is also called as **inverting zero crossing detector.**

Non-Inverting Comparator

A non-inverting comparator is an op-amp based comparator for which a reference voltage is applied to its inverting terminal and the input voltage is applied to its non-inverting terminal. This op-amp based comparator is called as **non-inverting** comparator because the input voltage, which has to be compared is applied to the non-inverting terminal of the op-amp.

The **circuit diagram** of a non-inverting comparator is shown in the following figure



The **operation** of a non-inverting comparator is very simple. It produces one of the two values, +Vsat+Vsat and −Vsat−Vsat at the output based on the values of input voltage VtVt and the reference voltage +Vref+Vref.

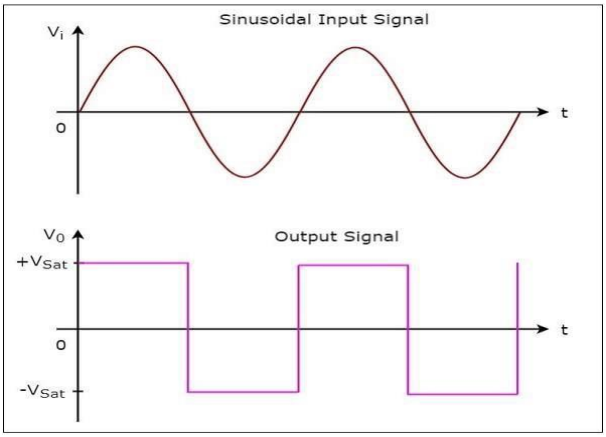
- The output value of a non-inverting comparator will be +Vsat+Vsat, for which the input voltage ViVi is greater than the reference voltage +Vref+Vref.
- The output value of a non-inverting comparator will bee −Vsat−Vsat, for which the input voltage ViVi is less than the reference voltage +Vref+Vref.

The **operation** of a non-inverting comparator is explained below −

- During the **positive half cycle** of the sinusoidal input signal, the voltage present at the non-inverting terminal of op-amp is greater than zero volts. Hence, the output value of a non-inverting comparator will be equal to +Vsat+Vsat during the positive half cycle of the sinusoidal input signal.
- Similarly, during the **negative half cycle** of the sinusoidal input signal, the voltage present at the non-inverting terminal of op-amp is less than zero volts. Hence, the output value of non-

inverting comparator will be equal to −Vsat−Vsat during the negative half cycle of the sinusoidal input signal.

The following figure shows the **input and output waveforms** of a non-inverting comparator, when the reference voltage is zero volts.



From the figure shown above, we can observe that the output transitions either from +Vsat+Vsat to −Vsat−Vsat or from −Vsat−Vsat to +Vsat+Vsat whenever the sinusoidal input signal crosses zero volts. That means, the output changes its value when the input is crossing zero volts. Hence, the above circuit is also called as **non-inverting zero crossing detector**.

Video Content / Details of website for further learning (if any):
https://www.youtube.com/watch?v=cfO8PDgsrN8

Important Books/Journals for further learning including the page nos.:
Linear Integrated Circuits By D. Roy Choudhury, Shail B. Jain T1

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LECTURE HANDOUTS

L 21

MDE

II / IV

Course Name with Code : 19MDC04 – LOGIC CIRCUITS FOR CLINICAL ENGINEERS

Course Faculty : Mrs.M.Birunda

Unit : III – Comparator and Waveform Generators

Date of Lecture:

Topic of Lecture: Applications of comparator

Introduction :

A **comparator** is an electronic circuit, which compares the two inputs that are applied to it and produces an output. The output value of the comparator indicates which of the inputs is greater or lesser. Please note that comparator falls under non-linear applications of ICs.

Prerequisite knowledge for Complete understanding and learning of Topic:

Operation of Op Amp, Basic Analog electronics and Electronic Devices, and Circuit theory

Applications of comparator:

Zero Crossing Detector

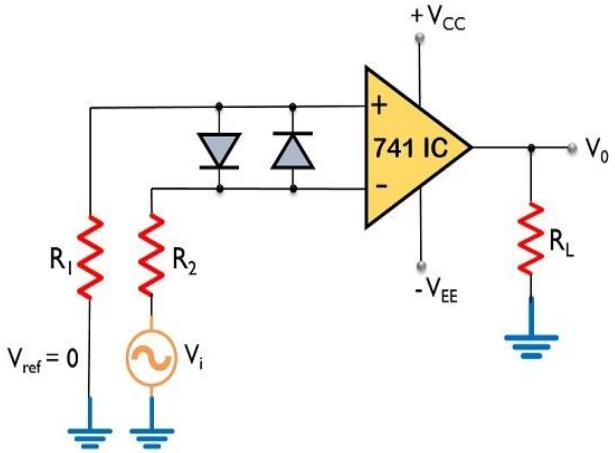
Definition: An op-amp detector that has the ability to detect the change from positive to negative or negative to a positive level of a sinusoidal waveform is known as a zero crossing detector. More specifically, we can say that it detects the zero crossing of the applied ac signal.

It is basically a voltage comparator whose output changes when the input signal crosses the zero of the reference voltage level. Thus it is named so.

It is also known to be a **square wave generator** as the applied input signal is converted into a square wave by the zero crossing detector.

Circuit Diagram of Zero Crossing Detector

The figure below represents the circuit of a zero crossing detector using inverting op-amp:



Here, the input signal V_i is provided to the inverting terminal of the op-amp while the non-inverting

terminal is grounded by making use of two resistors R_1 and R_2.
As we can see that analog input signal is provided at the inverting terminal of the op-amp. Thus, the waveform of the signal at the output will hold reverse polarity. This we will discuss under working of the detector.

Working of Zero Crossing Detector

As we have already discussed that it detects the point where the input signal crosses zero of the reference voltage level. For every crossing, the saturation level of the output signal changes from one to another.
As we have already mentioned that the reference level is set at 0 and applied at the non-inverting terminal of the op-amp. The sine wave applied at the inverting terminal of the op-amp is compared with the reference level each time the phase of the wave changes either from positive to negative or negative to positive.
Firstly, when positive half of the sinusoidal signal appears at the input. Then the op-amp comparator compares the reference voltage level with the peak level of the applied signal

$$V_0 = V_{ref} - V_i$$

And we know the reference level is 0, thus

$$V_0 = 0 - (+ V_{sat})$$

So, we will have

$$V_0 = - V_{sat}$$

Secondly, in case of the negative half of the sinusoidal signal, the op-amp comparator again compares the reference voltage level with the peak of the applied signal.
As this time the circuit is dealing with negative half of the signal, thus the peak will have a negative polarity.
Again

$$V_0 = V_{ref} - V_i$$

Thus,

$$V_0 = 0 - (- V_{sat})$$

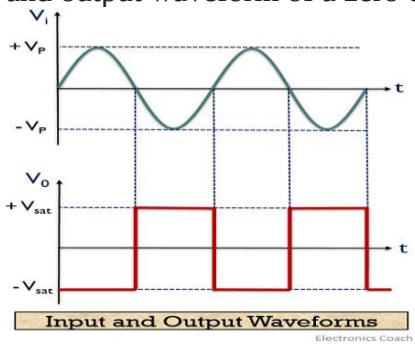
So, we get

$$V_0 = + V_{sat}$$

In this way, the zero crossing detector detects the change in the level of the applied signal.

Input and Output Waveform

From the beginning, we are mentioning that a zero crossing detector is also known to be a square wave generator. As the output of the window comparator is nothing but a square wave.
Let us now have a look at the input and output waveform of a zero crossing detector:



Applications of Zero Crossing Detector

Zero crossing detectors widely find applications in electronics circuits mainly for switching purpose and in phase locked loop. Also, these are used in frequency counters and in phase meters.
It can also be used as phase meters, as it can be used to measure the phase angle between two voltage applied at its terminals.

Window Comparator

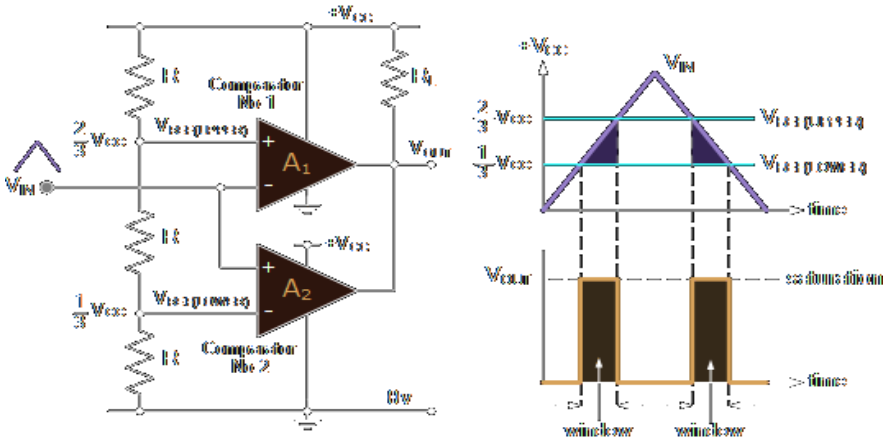
A **Window Comparator** is basically the inverting and the non-inverting comparators above combined into a single comparator stage. The window comparator detects input voltage levels that are within a specific band or *window* of voltages, instead of indicating whether a voltage is greater or less

than some preset or fixed voltage reference point.

This time, instead of having just one reference voltage value, a window comparator will have two reference voltages implemented by a pair of voltage comparators. One which triggers an op-amp comparator on detection of some upper voltage threshold, $V_{REF(UPPER)}$ and one which triggers an op-amp comparator on detection of a lower voltage threshold level, $V_{REF(LOWER)}$. Then the voltage levels between these two upper and lower reference voltages is called the "window", hence its name.

Using our idea above of a voltage divider network, if we now use three equal value resistors so that R1 = R2 = R3 = R we can create a very simple window comparator circuit as shown. Also as the resistive values are all equal, the voltage drops across each resistor will also be equal at one-third the supply voltage, 1/3Vcc. Then in this simple example, we can set the upper reference voltage to 2/3Vcc and the lower reference voltage to 1/3Vcc. Consider the window comparator circuit below.

Window Comparator Circuit



When V_{IN} is below the lower voltage level, $V_{REF(LOWER)}$ which equates to 1/3Vcc, the output will be LOW. When V_{IN} exceeds this 1/3Vcc lower voltage level, the first op-amp comparator detects this and switches the output HIGH to Vcc.

As V_{IN} continues to increase it passes the upper voltage level, $V_{REF(UPPER)}$ at 2/3Vcc and the second op-amp comparator detects this and switches the output back LOW. Then the difference between $V_{REF(UPPER)}$ and $V_{REF(LOWER)}$ (which is 2/3Vccc – 1/3Vcc in this example) creates the switching window for the positive going signal.

Lets now assume that V_{IN} is at its maximum value and equal to Vcc. As V_{IN} decreases it passes the upper voltage level $V_{REF(UPPER)}$ of the second op-amp comparator which switches the output HIGH. As V_{IN} continues to decrease it passes the lower voltage level, $V_{REF(LOWER)}$ of the first op-amp comparator once again switching the output LOW.

Then the difference between $V_{REF(UPPER)}$ and $V_{REF(LOWER)}$ creates the window for the negative going signal. So we can see that as V_{IN} passes above or passes below the upper and lower reference levels set by the two op-amp comparators, the output signal V_{OUT} will be HIGH or LOW.

Video Content / Details of website for further learning (if any):

https://www.youtube.com/watch?v=k9zQjEaKtfk&t=9s

Important Books/Journals for further learning including the page nos.:

Linear Integrated Circuits By D. Roy Choudhury, Shail B. Jain T1

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LECTURE HANDOUTS

L 22

MDE

II / IV

Course Name with Code : 19MDC04 – LOGIC CIRCUITS FOR CLINICAL ENGINEERS

Course Faculty : Mrs.M.Birunda

Unit : III – Comparator and Waveform Generators

Date of Lecture:

Topic of Lecture: Regenerative Comparator (Schmitt Trigger)

Introduction :

A Schmitt trigger circuit is also called a regenerative comparator circuit. The circuit is designed with a positive feedback and hence will have a regenerative action which will make the output switch levels.

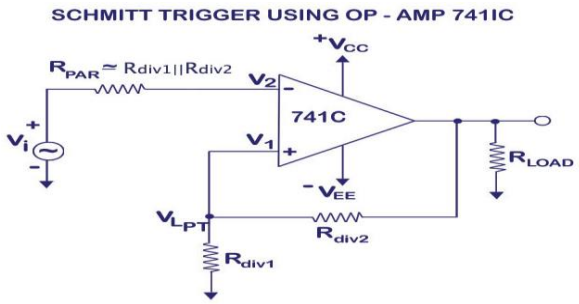
Prerequisite knowledge for Complete understanding and learning of Topic:

Operation of Op Amp, Basic Analog electronics and Electronic Devices, and Circuit theory

Schmitt Trigger or Regenerative Comparator Circuit

A Schmitt trigger circuit is also called a regenerative comparator circuit. The circuit is designed with a positive feedback and hence will have a regenerative action which will make the output switch levels. Also, the use of positive voltage feedback instead of a negative feedback, aids the feedback voltage to the input voltage, instead of opposing it. The use of a regenerative circuit is to remove the difficulties in a **zero-crossing detector circuit** due to low frequency signals and input noise voltages.

Shown below is the circuit diagram of a Schmitt trigger. It is basically an inverting comparator circuit with a positive feedback. The purpose of the Schmitt trigger is to convert any regular or irregular shaped input waveform into a square wave output voltage or pulse. Thus, it can also be called a squaring circuit.

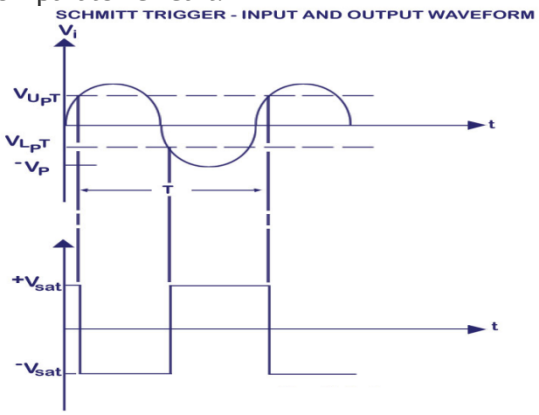


Schmitt Trigger Circuit Using Op-Amp uA741 IC

As shown in the circuit diagram, a voltage divider with resistors Rdiv1 and Rdiv2 is set in the positive feedback of the 741 IC op-amp. The same values of Rdiv1 and Rdiv2 are used to get the resistance value Rpar = Rdiv1||Rdiv2 which is connected in series with the input voltage. Rpar is used to minimize the offset problems. The voltage across R1 is fedback to the non-inverting input. The input voltage Vi triggers or changes the state of output Vout every time it exceeds its voltage levels above a certain threshold value called Upper Threshold Voltage (Vupt) and Lower Threshold Voltage (Vlpt).

Let us assume that the inverting input voltage has a slight positive value. This will cause a negative

value in the output. This negative voltage is fedback to the non-inverting terminal (+) of the op-amp through the voltage divider. Thus, the value of the negative voltage that is fedback to the positive terminal becomes higher. The value of the negative voltage becomes again higher until the circuit is driven into negative saturation (-Vsat). Now, let us assume that the inverting input voltage has a slight negative value. This will cause a positive value in the output. This positive voltage is fedback to the non-inverting terminal (+) of the op-amp through the voltage divider. Thus, the value of the positive voltage that is fedback to the positive terminal becomes higher. The value of the positive voltage becomes again higher until the circuit is driven into positive saturation (+Vsat). This is why the circuit is also named a regenerative comparator circuit.



Schmitt Trigger Input and Output Waveform

When Vout = +Vsat, the voltage across Rdiv1 is called Upper Threshold Voltage (Vupt). The input voltage, Vin must be slightly more positive than Vupt inorder to cause the output Vo to switch from +Vsat to -Vsat. When the input voltage is less than Vupt, the output voltage Vout is at +Vsat.

Upper Threshold Voltage, Vupt = +Vsat (Rdiv1/[Rdiv1+Rdiv2])

When Vout = -Vsat, the voltage across Rdiv1 is called Lower Threshold Voltage (Vlpt). The input voltage, Vin must be slightly more negaitive than Vlpt inorder to cause the output Vo to switch from -Vsat to +Vsat. When the input voltage is less than Vlpt, the output voltage Vout is at -Vsat.

Lower Threshold Voltage, Vlpt = -Vsat (Rdiv1/[Rdiv1+Rdiv2])

If the value of Vupt and Vlpt are higher than the input noise voltage, the positive feedback will eliminate the false output transitions. With the help of positive feedback and its regenerative behaviour, the output voltage will switch fast between the positive and negative saturation voltages.

Hysteresis Characteristics

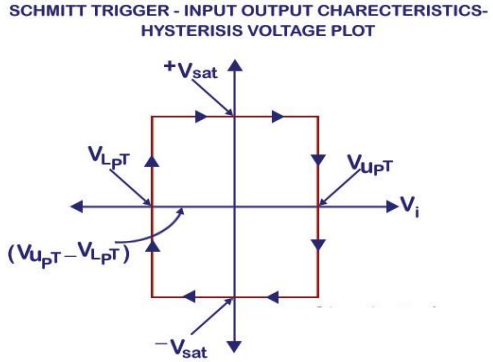
Since a comparator circuit with a positive feedback is used, a dead band condition hysteresis can occur in the output. When the input of the comparator has a value higher than Vupt, its output switches from +Vsat to -Vsat and reverts back to its original state, +Vsat, when the input value goes below Vlpt. This is shown in the figure below. The hysteresis voltage can be calculated as the difference between the upper and lower threshold voltages.

Vhysteresis = Vupt – Vlpt

Subsituting the values of Vupt and Vlpt from the above equations:

Vhysteresis = +Vsat (Rdiv1/Rdiv1+Rdiv2) – {-Vsat (Rdiv1/Rdiv1+Rdiv2)}

Vhysteresis = (Rdiv1/Rdiv1+Rdiv2) {+Vsat – (-Vsat)}



Schmitt-Trigger-Hysteresis Characteristics

Applications of Schmitt Trigger

Schmitt trigger is mostly used to convert a very slowly varying input voltage into an output having abruptly varying waveform occurring precisely at certain predetermined value of input voltage. Schmitt trigger may be used for all applications for which a general comparator is used. Any type of input

voltage can be converted into its corresponding square signal wave. The only condition is that the input signal must have large enough excursion to carry the input voltage beyond the limits of the hysteresis range. The amplitude of the square wave is independent of the peak-to-peak value of the input waveform.

Video Content / Details of website for further learning (if any):
https://www.youtube.com/watch?v=RcKq3MQvUeQ

Important Books/Journals for further learning including the page nos.:

Linear Integrated Circuits By D. Roy Choudhury, Shail B. Jain T1

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LECTURE HANDOUTS | **L 23**

MDE | **II / IV**

Course Name with Code : 19MDC04 – LOGIC CIRCUITS FOR CLINICAL ENGINEERS

Course Faculty : Mrs.M.Birunda

Unit : III – Comparator and Waveform Generators

Date of Lecture:

Topic of Lecture: Multivibrators, Astable multivibrator

Introduction :

A *multivibrator* circuit oscillates between a "HIGH" state and a "LOW" state producing a continuous output. Astable multivibrators generally have an even 50% duty cycle, that is that 50% of the cycle time the output is "HIGH" and the remaining 50% of the cycle time the output is "OFF".

Prerequisite knowledge for Complete understanding and learning of Topic:

Operation of Op Amp, Basic Analog electronics and Electronic Devices, and Circuit theory

Multivibrators

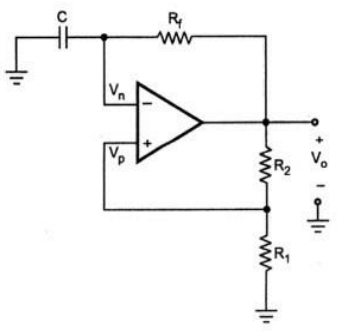
A *multivibrator* circuit oscillates between a "HIGH" state and a "LOW" state producing a continuous output. Astable multivibrators generally have an even 50% duty cycle, that is that 50% of the cycle time the output is "HIGH" and the remaining 50% of the cycle time the output is "OFF". In other words, the duty cycle for an astable timing pulse is 1:1.

There are basically three types of clock pulse generation circuits:

- Astable – A *free-running multivibrator* that has **NO** stable states but switches continuously between two states this action produces a train of square wave pulses at a fixed frequency.
- Monostable – A *one-shot multivibrator* that has only **ONE** stable state and is triggered externally with it returning back to its first stable state.
- Bistable – A *flip-flop* that has **TWO** stable states that produces a single pulse either positive or negative in value.

Astable Multivibrators

The **astable multivibrator** is also called as **a free running multivibrator.** It has **two** quasi-stable states i.e. no stable state such. **No external signal** is required to produce the changes in state. The component values used to decide the time for which circuit remains in each state. Usually, as the astable multivibrator oscillates between two states, is used to produce **a square wave.**



The circuit looks like a Schmitt trigger except that the input voltage is replaced by a capacitor. As

shown in fig. 6.15 the comparator and positive feedback resistors R_1 and R_2 form an inverting Schmitt trigger.

When V_0 is at V_{sat} , the feedback voltage is called the upper threshold voltage V_{UT} and is given as

$$V_{UT} = R_1 \frac{V_{sat}}{R_1 + R_2}$$

When V_0 is at $-V_{sat}$, the feedback voltage is called the lower threshold voltage V_{LT} and is given as

$$V_{LT} = -\frac{R_1 V_{sat}}{R_1 + R_2}$$

Circuit operation

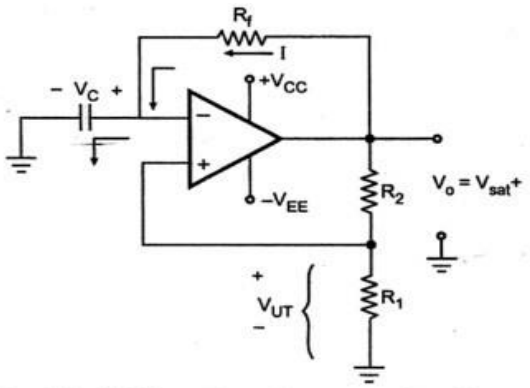


Fig. 6.16 (a) When $V_o = +V_{sat}$, capacitor charges towards V_{UT}

(i). When power is turned ON, V_0 automatically swings either V_{sat} or to $-V_{sat}$ since these are the only stable states allowed by Schmitt trigger. Assume it swings to $+V_{sat}$.

(ii). Now capacitor starts charging towards $+V_{sat}$ through the feedback path provided by the resistor R_f to the inverting input. As long as the capacitor voltage V_C is less than V_{UT}, the output voltage remains at V_{sat}

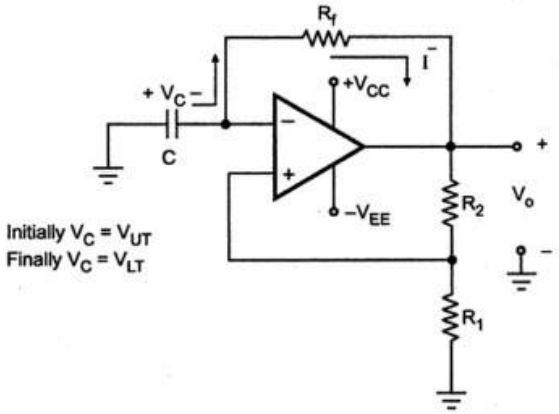


Fig. 6.16 (b) When $V_o = -V_{sat}$, capacitor charges towards V_{LT}

(iii). As soon as V_C charges to a value slightly greater than V_{UT} , the input goes positive with respect to the input. This switches the output voltage from $+V_{sat}$ to $-V_{sat}$

(iv). As V_0 switches to $-V_{sat}$, capacitor starts discharging via . The current I discharges capacitor to 0 V and recharges capacitor to V_{LT} When V_C becomes slightly more negative than the feedback voltage $V_{LT,}$ output voltage switches back to $+V_{sat}$.

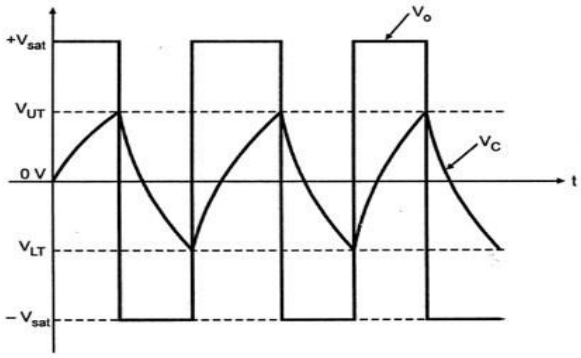


Fig. 6.16 (c) Waveforms

- **Frequency of Oscillation:** The frequency of oscillation is determined by the time it takes the capacitor to charge from V_{LT} to V_{UT} and vice versa.

Voltage across Capacitor at time t is given by the eq

$$V_C(t) = V_{CO}e^{-\frac{t}{RC}} + V_0\left(1 - e^{-\frac{t}{RC}}\right)$$

At time $t = T_C$

$$V_0 = -V_{sat}$$

$$V_C(T_C) = +\beta V_{sat}$$

$$V_C(t) = \left(V_{CO} - V_0\right)e^{-\frac{t}{RC}} + V_0$$

$$+\beta V_{sat} = \left(-\beta V_{sat} + V_{sat}\right)e^{-\frac{T_C}{RC}} + V_{sat}$$

$$T_C = RCln\left(\frac{1+\beta}{1-\beta}\right)$$

$$\beta = \frac{R_2}{R_1 + R_2}$$

$$T_C = T_d$$

Total time period (T)

$$T = T_C + T_d$$

$$T = 2RCln\left(\frac{1+\beta}{1-\beta}\right)$$

Video Content / Details of website for further learning (if any):
https://www.youtube.com/watch?v=T7T3At9N9dk

Important Books/Journals for further learning including the page nos.:
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LECTURE HANDOUTS

MDE

II / IV

Course Name with Code : 19MDC04 – LOGIC CIRCUITS FOR CLINICAL ENGINEERS

Course Faculty : Mrs.M.Birunda

Unit : III – Comparator and Waveform Generators

Date of Lecture:

Topic of Lecture: Monostable Multivibrator

Introduction :

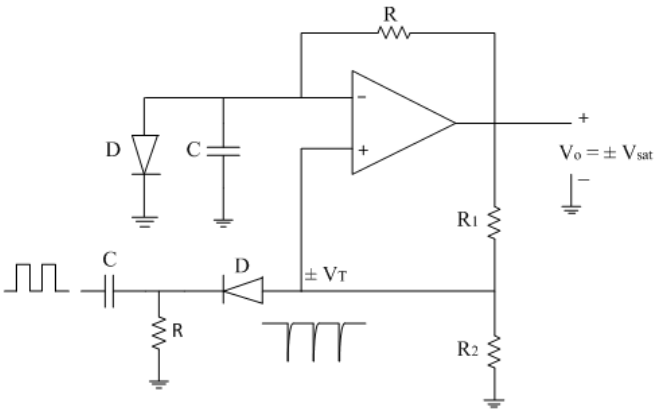
A *multivibrator* circuit oscillates between a "HIGH" state and a "LOW" state producing a continuous output. Astable multivibrators generally have an even 50% duty cycle, that is that 50% of the cycle time the output is "HIGH" and the remaining 50% of the cycle time the output is "OFF".

Prerequisite knowledge for Complete understanding and learning of Topic:

Operation of Op Amp, Basic Analog electronics and Electronic Devices, and Circuit theory

Monostable multivibrator

In this multivibrator one state is permanent stable state while the other state is temporary state. The permanent stable state is either HIGH or LOW. Assume the permanent state is HIGH. Apply a triggering pulse to change output state to LOW. But this state is a temporary state. So it will remain in LOW state for some time and after some time without applying any triggering pulse output goes back to permanent stable state i.e. HIGH.
Thus only one triggering pulse is required to come back to the permanent stable state so frequency of output is equal to frequency of input triggering pulse. Thus called as single shot or mono-shot multivibrator. The following circuit diagram shows monostable multivibrator using op-amp.

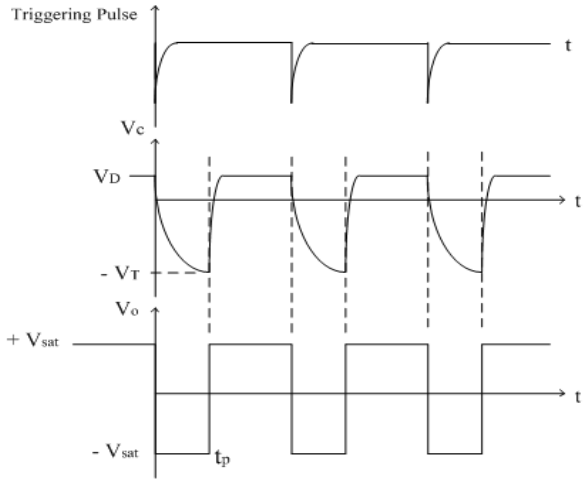


The triggering pulses are obtained by differentiating a square wave. The pulse has large amplitude and small width. In most of the circuits we require only one type of pulses either positive or negative. So one type of pulses should be eliminated. This is done with the help of diode when it is forward biased. Let us assume, for above circuit the stable state is +Vsat. so diode D is forward biased and voltage

across is 0.7V. Thus voltage across capacitor (i.e. voltage at inverting terminal) is 0.7V. Select values of R1 and R2 such that voltage an non-inverting terminal is greater than 0.7V so output is +Vsat. Voltage across capacitor is always 0.7V because of diode. In forward biased condition resistance of diode is very small so capacitor is almost short so no charging takes place. If output want to be –Vsat, then voltage at inverting terminal should be greater than non-inverting terminal. So apply a negative triggering pulse at non-inverting terminal to change the output state.

Working:

A negative triggering pulse is applied at t = 0. Initially drop across capacitor C is 0.7V and output is +Vsat. When pulse is applied at t = 0, output state changes to -Vsat. The diode D is reversed biased so capacitor starts charging through resistance R towards-Vsat. When output is –Vsat, triggering point VT is also negative, so when capacitor charges upto –VT, output changes state to +Vsat. The capacitor then discharges through diode forward resistance (rf). The diode is almost shorted so discharging time constant is very small. The triggering pulses are applied only when output is in permanent state or the triggering pulse can be applied at that time when the output is just come back to original permanent state. The time constant RC determines the pulse width (tp) of the output pulse, which is a rectangular shape. So monostablemultivibrator is also called as rectangular pulse generator. The related waveforms are shown in figure below,



Video Content / Details of website for further learning (if any):

https://www.youtube.com/watch?v=pUibCkUB364&t=65s

Important Books/Journals for further learning including the page nos.:

Linear Integrated Circuits By D. Roy Choudhury, Shail B. Jain T1

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LECTURE HANDOUTS

MDE

II / IV

Course Name with Code : 19MDC04 – LOGIC CIRCUITS FOR CLINICAL ENGINEERS

Course Faculty : Mrs.M.Birunda

Unit : III – Comparator and Waveform Generators

Date of Lecture:

Topic of Lecture: Principles of sine wave oscillator

Introduction :

The oscillators that produce an output having a sine waveform are called **sinusoidal** or **harmonic oscillators**. Such oscillators can provide output at frequencies ranging from 20 Hz to 1 GHz.

Prerequisite knowledge for Complete understanding and learning of Topic:

Operation of Op Amp, Basic Analog electronics and Electronic Devices, and Circuit theory

Detailed content of the Lecture:

Principles of sine wave oscillator

The oscillators that produce an output having a sine waveform are called **sinusoidal** or **harmonic oscillators**. Such oscillators can provide output at frequencies ranging from 20 Hz to 1 GHz.

Sinusoidal Oscillators - Basic Concepts

An amplifier with positive feedback produces its output to be in phase with the input and increases the strength of the signal. Positive feedback is also called as **degenerative feedback** or **direct feedback**. This kind of feedback makes a feedback amplifier, an oscillator.

The use of positive feedback results in a feedback amplifier having closed-loop gain greater than the open-loop gain. It results in **instability** and operates as an oscillatory circuit. An oscillatory circuit provides a constantly varying amplified output signal of any desired frequency.

An Oscillator circuit is a complete set of all the parts of circuit which helps to produce the oscillations. These oscillations should sustain and should be Undamped as just discussed before. Let us try to analyze a practical Oscillator circuit to have a better understanding on how an Oscillator circuit works.

Frequency Stability of an Oscillator

The frequency stability of an oscillator is a measure of its ability to maintain a constant frequency, over a long time interval. When operated over a longer period of time, the oscillator frequency may have a drift from the previously set value either by increasing or by decreasing.

The change in oscillator frequency may arise due to the following factors −

- Operating point of the active device such as BJT or FET used should lie in the linear region of the amplifier. Its deviation will affect the oscillator frequency.
- The temperature dependency of the performance of circuit components affect the oscillator frequency.
- The changes in d.c. supply voltage applied to the active device, shift the oscillator frequency. This can be avoided if a regulated power supply is used.
- A change in output load may cause a change in the Q-factor of the tank circuit, thereby causing a change in oscillator output frequency.

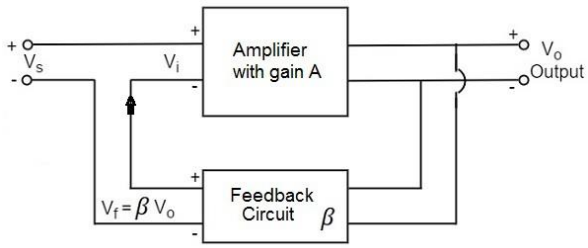
- The presence of inter element capacitances and stray capacitances affect the oscillator output frequency and thus frequency stability.

The Barkhausen Criterion

With the knowledge we have till now, we understood that a practical oscillator circuit consists of a tank circuit, a transistor amplifier circuit and a feedback circuit. so, let us now try to brush up the concept of feedback amplifiers, to derive the gain of the feedback amplifiers.

Principle of Feedback Amplifier

A feedback amplifier generally consists of two parts. They are the **amplifier** and the **feedback circuit**. The feedback circuit usually consists of resistors. The concept of feedback amplifier can be understood from the following figure below.



From the above figure, the gain of the amplifier is represented as A. The gain of the amplifier is the ratio of output voltage Vo to the input voltage V_i. The feedback network extracts a voltage $V_f = \beta V_o$ from the output V_o of the amplifier.

This voltage is added for positive feedback and subtracted for negative feedback, from the signal voltage V_s.

So, for a positive feedback,

$$V_i = V_s + V_f = V_s + \beta V_o$$

The quantity $\beta = V_f/V_o$ is called as feedback ratio or feedback fraction.

The output V_o must be equal to the input voltage $(V_s + \beta V_o)$ multiplied by the gain A of the amplifier. Hence,

$$(Vs+\beta Vo)A=Vo(Vs+\beta Vo)A=Vo$$

Or

$$AVs+A\beta Vo=VoAVs+A\beta Vo=Vo$$

Or

$$AVs=Vo(1-A\beta)AVs=Vo(1-A\beta)$$

Therefore

$$VoVs=A1-A\beta VoVs=A1-A\beta$$

Let A_f be the overall gain (gain with the feedback) of the amplifier. This is defined as the ratio of output voltage V_o to the applied signal voltage V_s, i.e.,

$$Af=OutputVoltageInputSignalVoltage=VoVsAf=OutputVoltageInputSignalVoltage=VoVs$$

Rrom the above two equations, we can understand that, the equation of gain of the feedback amplifier with positive feedback is given by

$$Af=A1-A\beta Af=A1-A\beta$$

Where **Aβ** is the **feedback factor** or the **loop gain**.

If $A\beta = 1$, $A_f = \infty$. Thus the gain becomes infinity, i.e., there is output without any input. In another words, the amplifier works as an Oscillator.

The condition $A\beta = 1$ is called as **Barkhausen Criterion of oscillations**. This is a very important factor to be always kept in mind, in the concept of Oscillators.

Video Content / Details of website for further learning (if any):

https://www.youtube.com/watch?v=XVS8Puf4tiw

Important Books/Journals for further learning including the page nos.:

Linear Integrated Circuits By D. Roy Choudhury, Shail B. Jain T1

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LECTURE HANDOUTS | **L 26**

MDE | **II / IV**

Course Name with Code : 19MDC04 – LOGIC CIRCUITS FOR CLINICAL ENGINEERS

Course Faculty : Mrs.M.Birunda

Unit : III – Comparator and Waveform Generators

Date of Lecture:

Topic of Lecture: RC phase shift oscillator

Introduction :

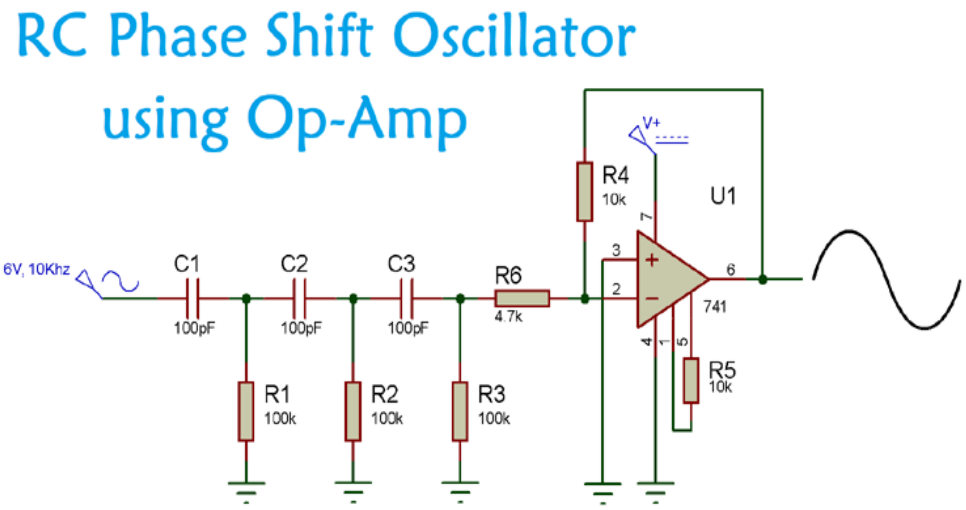
The oscillators that produce an output having a sine waveform are called **sinusoidal** or **harmonic oscillators**. Such oscillators can provide output at frequencies ranging from 20 Hz to 1 GHz. ***RC phase-shift oscillators*** use resistor-capacitor (RC) network to provide the phase-shift required by the feedback signal. They have excellent frequency stability and can yield a pure sine wave for a wide range of loads.

Prerequisite knowledge for Complete understanding and learning of Topic:

Operation of Op Amp, Basic Analog electronics and Electronic Devices, and Circuit theory

RC phase shift oscillator

A **Phase Shift Oscillator** is an **electronic oscillator circuit** which produces sine wave output. It can either be designed by using transistor or by using an Op-amp as inverting amplifier. Generally, these phase shift oscillators are used as audio oscillators. In RC phase shift oscillator, 180 degree phase shift is generated by the RC network and another 180 degree is generated by the Op-amp, so the resulting wave is inverted by 360 degree.



When we use op-amp for RC phase shift oscillator, it functions as an inverting amplifier. Initially, the input wave has been into the RC network, due to which we get 180 degree of phase shift. And, this output of RC is fed into the inverting terminal of the op-amp.

Now, as we know that the op-amp will produce a 180 degree of phase shift when functions as an inverting amplifier. So, we get a 360-degree of phase shift in the output sine wave. This RC phase shift oscillator using op-amp provides a constant frequency even under the varying load conditions.

Here, the feedback network is offering a phase shift of 180 degree. We are getting 60 degree from each of the RC network. And, the remaining 180 degree phase shift is generated by the op-amp in the inverting configuration.

For calculating the **frequency of oscillation** use the below formula:

$F = 1 / 2\pi RC\sqrt{2N}$

Where, N is the number of RC stages formed by the resistors R and the capacitors C.

The disadvantage of RC phase shift oscillator using op-amp is that it can't be used for high frequency applications. Because whenever the frequency is too high the capacitor's reactance is very low and it act as a short circuit.

Apart from generating the sine wave output they are also used to provide significant control over the phase shifting process. Other usages of phase shift oscillators are:

1. In audio oscillators
2. Sine Wave Inverter
3. Voice Synthesis
4. GPS units
5. Musical Instruments.

Video Content / Details of website for further learning (if any):
https://www.youtube.com/watch?v=i9754WMGOio

Important Books/Journals for further learning including the page nos.:
Linear Integrated Circuits By D. Roy Choudhury, Shail B. Jain T1

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LECTURE HANDOUTS

MDE

II / IV

Course Name with Code : 19MDC04 – LOGIC CIRCUITS FOR CLINICAL ENGINEERS

Course Faculty : Mrs.M.Birunda

Unit : III – Comparator and Waveform Generators

Date of Lecture:

Topic of Lecture: Wein bridge oscillator

Introduction :

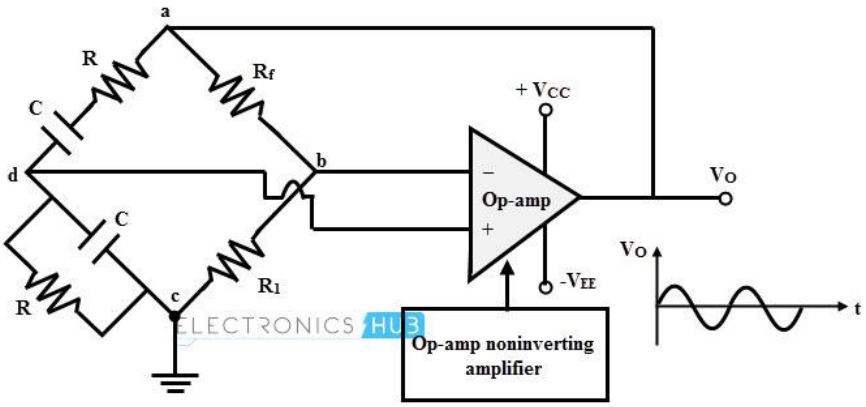
The oscillators that produce an output having a sine waveform are called **sinusoidal** or **harmonic oscillators**. Such oscillators can provide output at frequencies ranging from 20 Hz to 1 GHz. A Wien bridge oscillator produces sine waves which uses RC network as the frequency determining portion of the circuit.

Prerequisite knowledge for Complete understanding and learning of Topic:

Operation of Op Amp, Basic Analog electronics and Electronic Devices, and Circuit theory

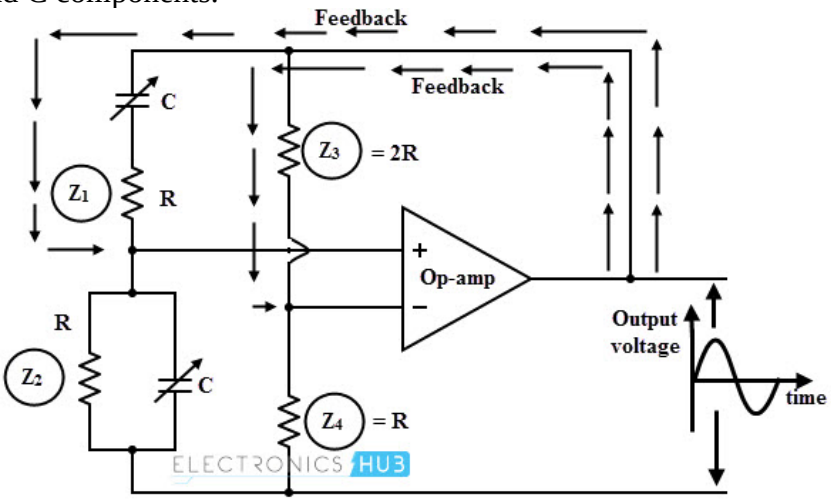
Wien Bridge Oscillator Using Op-amp

The figure below shows a widely used type of Wien bridge oscillator. The operational amplifier is used in a non inverting configuration and feedback form a voltage divider network. The resistances R1 and Rf forms the part of the feedback path which determines or facilitates to adjust the amplifier gain.
The output of op-amp is connected as input to the bridge at points a and c while the output of the bridge at points b and d are connected to the input of op-amp.



A portion of the amplifier output is feedback through the voltage divider network (a series combination of resistor and capacitor) to the positive or non-inverting terminal of the amplifier.
Also, second portion of the amplifier is feedback to the inverting or negative terminal of the amplifier through the impedance of magnitude 2R.
If the feedback network elements are chosen properly, the phase shift of the signal input to the amplifier is zero at certain frequency. Since the amplifier is non-inverting which introduce zero phase shift plus the feedback network zero phase shift, the total phase shift becomes zero around the loop hence the required condition of oscillations.

Therefore the Wien bridge oscillator works as a sine wave generator whose frequency of oscillations is determined by R and C components.



The gain of the operational amplifier is expressed as

$$A = 1 + (Rf / R1)$$

As we discussed above that the gain of non-inverting amplifier must be of minimum 3 to satisfy Barkhausen criterion.

Therefore, $1 + (Rf / R1) \geq 3$

$$\rightarrow (Rf / R1) \geq 2$$

Therefore the ratio of resistances Rf to R1 must be equal to or greater than 2. The frequency of oscillations is given by

$$f = 1 / 2\pi RC$$

Video Content / Details of website for further learning (if any):

https://www.youtube.com/watch?v=gbUXbaxvX94

Important Books/Journals for further learning including the page nos.:

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LECTURE HANDOUTS

MDE

II / IV

Course Name with Code : 19MDC04 – LOGIC CIRCUITS FOR CLINICAL ENGINEERS

Course Faculty : Mrs.M.Birunda

Unit : IV – Phase Locked Loops and Data Converters

Date of Lecture:

Topic of Lecture: Block diagram of PLL- Principles, Types

Introduction :

A phase-locked loop (PLL) is an electronic circuit with a voltage or voltage-driven oscillator that constantly adjusts to match the frequency of an input signal. PLLs are used to generate, stabilize, modulate, demodulate, filter or recover a signal from a "noisy" communications channel where data has been interrupted.

Prerequisite knowledge for Complete understanding and learning of Topic:

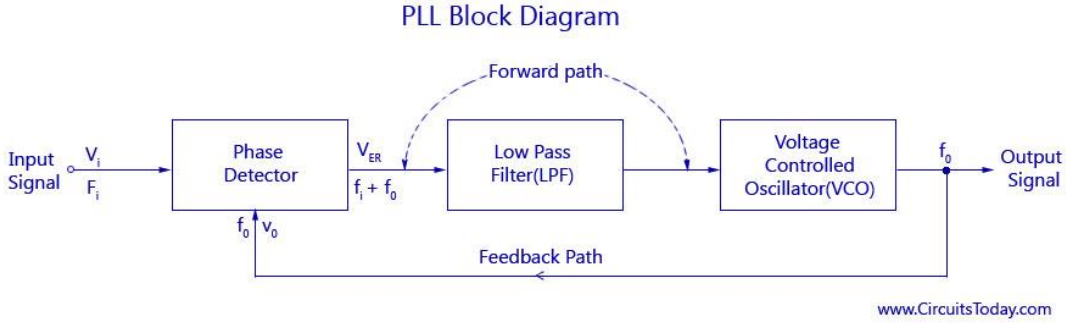
Working of Op amp, Electronic Devices, Analog Electronics, Circuit Theory, Communication Theory

PLL

The concept of Phase Locked Loops (PLL) first emerged in the early 1930's.But the technology was not developed as it now, the cost factor for developing this technology was very high. Since the advancement in the field of integrated circuits, PLL has become one of the main building blocks in the electronics technology. In present, the PLL is available as a single IC in the SE/NE560 series (560, 561, 562, 564, 565 and 567) to further reduce the buying cost ,the discrete IC's are used to construct a PLL.

PLL Block Diagram

The block diagram of a basic PLL is shown in the figure below. It is basically a flip flop consisting of a phase detector, a low pass filter (LPF),and a Voltage Controlled Oscillator (VCO).



The input signal Vi with an input frequency fi is passed through a phase detector. A phase detector basically a comparator which compares the input frequency fiwith the feedback frequency fo .The phase detector provides an output error voltage Ver (=fi+fo),which is a DC voltage. This DC voltage is then passed on to an LPF. The LPF removes the high frequency noise and produces a steady DC level, Vf (=Fi-Fo). Vf also represents the dynamic characteristics of the PLL.

The DC level is then passed on to a VCO. The output frequency of the VCO (fo) is directly

proportional to the input signal. Both the input frequency and output frequency are compared and adjusted through feedback loops until the output frequency equals the input frequency. Thus the PLL works in these stages – free-running, capture and phase lock.

As the name suggests, the free running stage refer to the stage when there is no input voltage applied. As soon as the input frequency is applied the VCO starts to change and begin producing an output frequency for comparison this stage is called the capture stage. The frequency comparison stops as soon as the output frequency is adjusted to become equal to the input frequency. This stage is called the phase locked state.

2. Low Pass Filter (LPF)

A Low Pass Filter (LPF) is used in Phase Locked Loops (PLL) to get rid of the high frequency components in the output of the phase detector. It also removes the high frequency noise. All these features make the LPF a critical part in PLL and helps control the dynamic characteristics of the whole circuit. The dynamic characteristics include capture and lock ranges, bandwidth, and transient response. The lock range is the tracking range where the range of frequencies of the PLL system follows the changes in the input frequency. The capture range is the range in which the Phase Locker Loops attains the Phase Lock.

When the filter bandwidth is reduced, the response time increases .But this reduces the capture range. But it also helps in reducing noise and in maintaining the locked loop through momentary losses of signal. Two types of passive filter are used for the LPF circuit in a PLL. An amplifier is used also with LPF to obtain gain. The active filter used in PLL is shown below.

3. Voltage Controlled Oscillator (VCO)

The main function of the VCO is to generate an output frequency that is directly proportional to the input voltage. The connection diagram of a SE/NE 566 VCO is shown in the figure below. The macimum frequency of the VCO is 500 KHz.

This VCO provides simultaneous square wave and triangular wave outputs as a function of the input voltage. The frequency of oscillation is determined by the resistor R and capacitor C along with the voltage Vc applied to the control terminal.

Video Content / Details of website for further learning (if any):

https://www.youtube.com/watch?v=CM8n3wzNOvc

Important Books/Journals for further learning including the page nos.:

Linear Integrated Circuits 4th Edition by D. Roy Choudhury and Shail B. Jain T1

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LECTURE HANDOUTS

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II / IV

Course Name with Code : 19MDC04 – LOGIC CIRCUITS FOR CLINICAL ENGINEERS

Course Faculty : Mrs.M.Birunda

Unit : IV – Phase Locked Loops and Data Converters

Date of Lecture:

Topic of Lecture: Phase Detector, Voltage controlled oscillator

Introduction :

A phase-locked loop (PLL) is an electronic circuit with a voltage or voltage-driven oscillator that constantly adjusts to match the frequency of an input signal. PLLs are used to generate, stabilize, modulate, demodulate, filter or recover a signal from a "noisy" communications channel where data has been interrupted.

Prerequisite knowledge for Complete understanding and learning of Topic:

Working of Op amp, Electronic Devices, Analog Electronics, Circuit Theory, Communication Theory

Phase Detector, Voltage controlled oscillator

Now let us study in detail about the various parts of a PLL – The phase detector, Low Pass Filter and Voltage Controlled Oscillator.

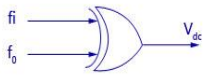
1. Phase Detector

This comparator circuit compares the input frequency and the VCO output frequency and produces a dc voltage that is proportional to the phase difference between the two frequencies. The phase detector used in PLL may be of analog or digital type. Even though most of the monolithic PLL integrated circuits use analog phase detectors, the majority of discrete phase detectors are of the digital type. One of the most commonly used analog phase detector is the double balanced mixer circuit. Some of the common digital type phase detectors are

1.1 Exclusive OR Phase Detector

An exclusive OR phase detector is shown in the figure below.

Exclusive - OR Phase Detector



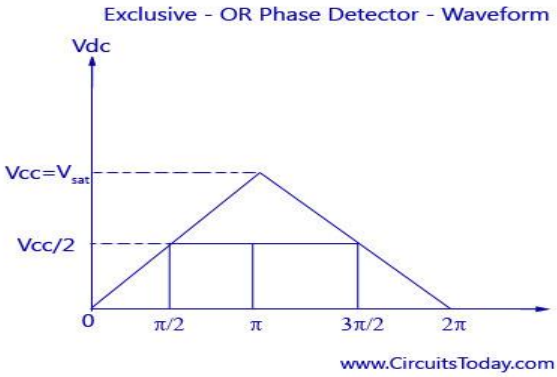
fi	f_0	Output
Low	Low	Low
Low	High	High
High	Low	High
High	High	Low

www.CircuitsToday.com

Exclusive-OR Phase Detector

It is obtained as a CMOS IC of type 4070. Both the frequencies are provided as an input to the EX OR phase detector. Obeying the EX-OR concept the output becomes HIGH only if either of the inputs fi or fo becomes HIGH. All other conditions will produce a LOW output. Let us consider a waveform where the input frequency leads the output frequency by θ degrees. That is, fi and fo has a phase difference of θ degrees. The dc output voltage of the comparator will be a function of the phase difference between its two inputs.

The figure shows the graph of DC output voltage as a function of the phase difference between fi and fo. The output DC voltage is maximum when the phase detector is 180°.This type of phase detector is used when both fi and fo are square waves.



Exclusive-OR Phase Detector-Waveform

1.2 Edge Triggered Phase Detector

Edge triggered phase detector is used when fi and fo are pulse waveforms with less than 50% duty cycles. The figure of such a phase detector using an R-S Flip Flop is shown below. Two NOR Gate (CD4001) are cross-coupled to form an R-S Flip Flop. The output of the phase detector changes it's logic state by triggering of the R-S Flip Flop. That is, the output of the phase detector changes its logic state on the positive edge of the input fi and fo. The advantage of such a detector can be understood from the graph below. It is clear that the DC output voltage is linear over 360°.

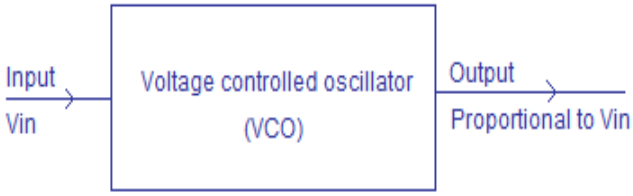
Monolithic Phase Detectors

The monolithic type phase detector uses a CMOS type 4044 IC ,Which is highly advantages as the harmonic sensitivity and duty cycle problems are neglected and the circuit will be respond only to the transition in the input signals. This is the most preferred phase detector in the critical applications as the phase error and the output error voltage are independent of variations in the amplitude and duty cycles of the input waveforms.

Voltage Controlled Oscillator

Voltage controlled oscillator is a type of oscillator where the frequency of the output oscillations can be varied by varying the amplitude of an input voltage signal. Voltage controlled oscillators are commonly used in frequency (FM), pulse (PM) modulators and phase locked loops (PLL).

Another application of the voltage controlled oscillator is the variable frequency signal generator itself. The block diagram of a typical voltage controlled oscillator is shown below.



Voltage controlled oscillators can be broadly classified into a linear voltage controlled oscillators and relaxation type voltage controlled oscillators. Linear voltage controlled oscillators are generally used to produce a sine wave. In such oscillators, an LC tank circuit is used for producing oscillations. An active element like a transistor is used for amplifying the output of the LC tank circuit, compensating the energy lost in the tank circuit and for establishing the necessary feedback conditions. Here a varactor (varicap) diode is used in place of the capacitor in the tank circuit. A varactor diode is a type of semiconductor diode whose capacitance across the junction can be varied by varying the voltage across the junction. Thus by varying the voltage across the varicap diode in the tank circuit, the output frequency of the VCO can be varied.

Relaxation-type voltage controlled oscillators are used to produce a sawtooth or triangular waveform. This is achieved by the gradual charging and sudden discharge of a capacitor connected appropriately

to an active element (UJT, PUT etc) or a monolithic IC (LM566 etc). Nowadays relaxation type VCOs are generally realized using monolithic ICs.
Video Content / Details of website for further learning (if any): https://www.youtube.com/watch?v=EeYL6lJsNT8 **https://www.youtube.com/watch?v=35jWSQXku74**
Important Books/Journals for further learning including the page nos.: **Linear Integrated Circuits 4th Edition by D. Roy Choudhury and Shail B. Jain T1**

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LECTURE HANDOUTS

MDE

II / IV

Course Name with Code : 19MDC04 – LOGIC CIRCUITS FOR CLINICAL ENGINEERS

Course Faculty : Mrs.M.Birunda

Unit : IV – Phase Locked Loops and Data Converters

Date of Lecture:

Topic of Lecture: IC 566 and IC 565 Internal block diagram

Introduction :

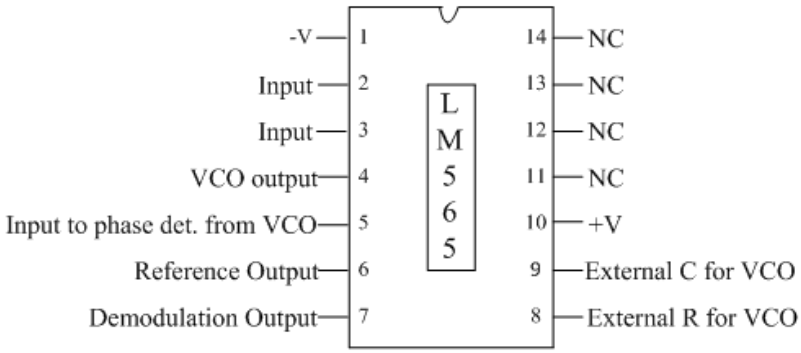
A phase-locked loop (PLL) is an electronic circuit with a voltage or voltage-driven oscillator that constantly adjusts to match the frequency of an input signal. PLLs are used to generate, stabilize, modulate, demodulate, filter or recover a signal from a "noisy" communications channel where data has been interrupted.

Prerequisite knowledge for Complete understanding and learning of Topic:

Working of Op amp, Electronic Devices, Analog Electronics, Circuit Theory, Communication Theory

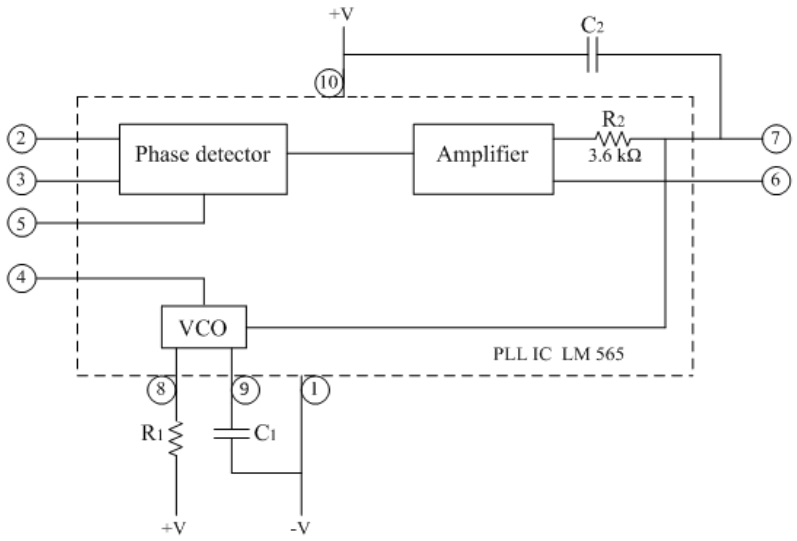
PLL IC 565

The PLL IC 565 is usable over the frequency range 0.1 Hz to 500 kHz. It has highly stable centre frequency and is able to achieve a very linear FM detection. The output of VCO is capable of producing TTL compatible square wave. The dual supply is in the range of ±6V to ±12V. The IC can also be operated from single supply in the range 12V to 24V. The following figure shows the pin-out and the internal block schematic of PLL IC LM 565.



It is a 14 pin IC, operated from a dual power supply +V (at pin no. 10) and –V (at pin no. 1).
Pin no 2 & 3 -> Signal input for phase detector.
Pin no 4 ->VCO output is available
Pin no 4 & 5 are shorted externally so that VCO output is applied for phase detection. In some applications PLL loop is broken and some circuit is to be connected between pin no 4 and 5.
Pin no 6-> reference dc voltage is available.

Pin no 7 -> demodulated output.If input signal between pin no 2 and 3 is FM signal then at pin no 7 we get FM demodulation output.
Pin no 8 and 9 -> external R1 and C1 for VCO (determines free running frequency of VCO)
Internal resistance R2 and external capacitor C2 forms a LPF. The value of internal resistance R2 is 3.6kΩ.

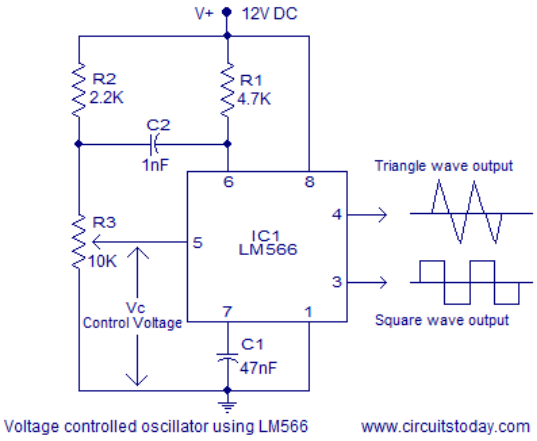


Features of IC 565:
1) Extreme stability of center frequency typically 200ppm.
2) Wide range of operating voltage ±6V to ±12V.
3) Very high linearity of demodulated output typically 0.2%
4) Centre frequency of VCO is programmable by means of resistor, capacitor or voltage.
5) TTL compatible square wave output.
6) Highly linear triangular wave output available at pin no.9
7) Loop can be broken between pin no.4 and 5 and external circuit can be added.
8) Frequency adjustable over the range 1:10 with single capacitor.

Voltage controlled oscillator using LM566 IC

LM566 is a **monolithic voltage controlled oscillator** from National Semiconductors. It can be used to generates square and triangle waveforms simultaneously. The frequency of the output waveform can be adjusted using an external control voltage. The output frequency can be also programmed using a set of external resistor and capacitor.
Typical applications of LM566 IC are signal generators, FM modulators, FSK modulators, tone generators etc. The LM566 IC can be operated from a single supply or dual supply. While using a single supply, the supply voltage range is from 10V to 24V. The IC has a very linear modulation characteristic and has excellent thermal stability. The circuit diagram of a voltage controlled oscillator using LM566 is shown in the figure below.

Circuit Diagram



Components
Resistor – 4.7k ohm – 1 nos

Resistor – 2.2k ohm – 1 nos
Resistor – 10k ohm – 1 nos
IC – LM566 – 1 nos
Capacitor – 47nF – 1 nos
Capacitor – 1nF – 1 nos

Working

Resistor R1 and capacitor C1 form the timing components. Capacitor C2 is used to prevent the parasitic oscillations during VCO switching. Resistor R3 is used to provide the control voltage Vc. Triangle and square wave outputs are obtained from pins 4 and 3 respectively. The output frequency of the VCO can be obtained using the following equation:

Fout = $2.4(V^+-V5)/(R1C1V^+)$. Where Fout is the output frequency, R1 and C1 are the timing components and V^+ is the supply voltage.

Video Content / Details of website for further learning (if any):

https://www.youtube.com/watch?v=j_cJ7DV_T_M

Important Books/Journals for further learning including the page nos.:

Linear Integrated Circuits 4th Edition by D. Roy Choudhury and Shail B. Jain T1

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L 31

LECTURE HANDOUTS

MDE

II / IV

Course Name with Code : 19MDC04 – LOGIC CIRCUITS FOR CLINICAL ENGINEERS

Course Faculty : Mrs.M.Birunda

Unit : IV - Phase Locked Loops and Data Converters

Date of Lecture:

Topic of Lecture: PLL applications

Introduction :

A phase-locked loop (PLL) is an electronic circuit with a voltage or voltage-driven oscillator that constantly adjusts to match the frequency of an input signal. PLLs are used to generate, stabilize, modulate, demodulate, filter or recover a signal from a "noisy" communications channel where data has been interrupted.

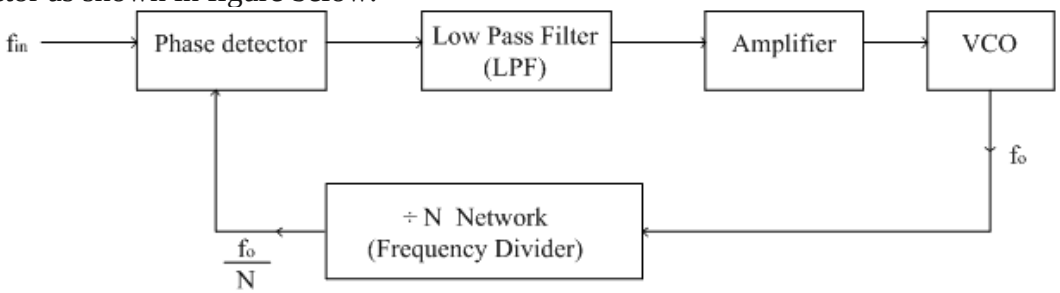
Prerequisite knowledge for Complete understanding and learning of Topic:

Working of Op amp, Electronic Devices, Analog Electronics, Circuit Theory, Communication Theory

PLL applications

1. Frequency Multiplier:

In this application, the loop is broken and a frequency divider network is inserted between VCO and phase detector as shown in figure below.



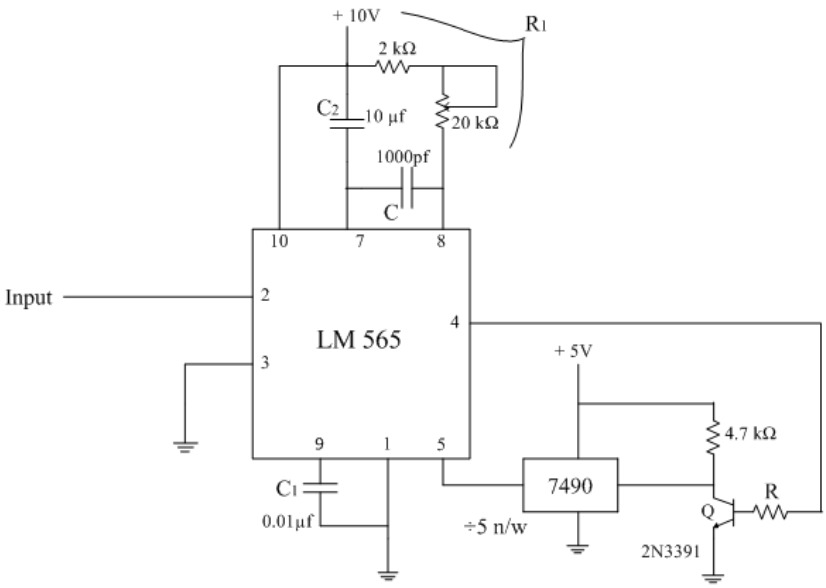
Since the output of frequency divider is locked to input frequency fin, the VCO is actually running at a multiple of the input frequency. The desired amount of multiplication can be obtained by selecting a proper ÷N network.

∴Input to phase detector, fin=fo/N

∴fo=Nfin

First adjust the fin range and then adjust the free running frequency fo of the VCO by means of R1 and C1.

Consider the following example shown below. Between pin no.4 and 5 the loop is broken i.e. ÷N network is inserted. In this case we have connected IC 7490 as ÷5 network. The output of VCO at pin no. 4 is not sufficient to drive IC so a transistor is used in-between to increase the drive. Transistor is in CE configuration so there is current gain at collector to drive IC. After ÷5 network, the frequency is applied to phase detector.



VCO frequency can be varied with the help of R1 (consists of 20kΩ pot and 2kΩ resistor) and C1.

$$f(Omin)=0.3/(R_{1\_max}\ C_1)=0.3/(22k\Omega\times0.01\mu f)=1.3636kHz$$

$$f(Omax)=0.3/(R_{1\_min}\ C_1)=0.3/(2k\Omega\times0.01\mu f)=15kHz$$

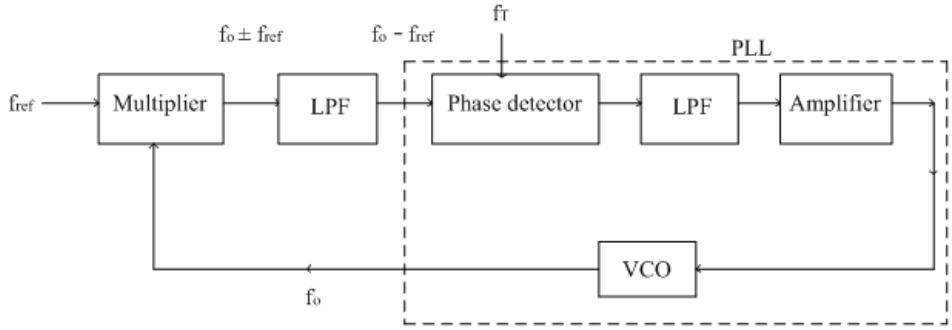
Thus the output frequency can be varied from 1.3636 kHz to 15 kHz with a single capacitor. The input waveform can be square wave (pin no.3) or sine wave (pin no. 2). A small capacitor, typically 1000pf is connected between pin no. 7 and 8 to eliminate possible oscillations. Also capacitor C2 should be large enough to stabilize the VCO frequency.

2. Frequency Translator (frequency Synthesizer):

In some applications we want to shift the input frequency (fin) by a small amount and not by multiple numbers. This shift is called as frequency translation (fT). It is useful in communication systems. While transmission, a carrier frequency is used which is highly stable. We can generate carrier frequency from oscillator. For this purpose a quartz crystal oscillator is required.As crystal oscillators have some temperature coefficient, we get some thermal drift in frequency. To avoidthis frequency change due to temperature, we have to keep temperature constant. This method is very costly.

If we want to use many carrier frequencies then it is impossible to use separate crystal for each carrier frequency. So by using PLL we can generate different carrier frequencies shifted by small amount from reference frequency.

A stable frequency generated by crystal is called reference frequency and numbers of other frequencies are generated from PLL. Since the PLL IC is available in low cost, the system is not costly. The following figure shows the block diagram of frequency translator.



Externally multiplier (or mixer) and LPF are added. Multiplier is basically a non-linear circuit. Input for multipliers are fref and VCO frequency fo.

Let fref is 1 MHz and we want to shift it to a value 1.2 MHz So there is a frequency translation of 0.2 MHz.

At the output of multiplier, we have number of frequency components including addition and difference frequencies i.e. (fo ± fref). This frequency is passed through LPF. The output of LPF is the difference signal i.e. (fo-fref).

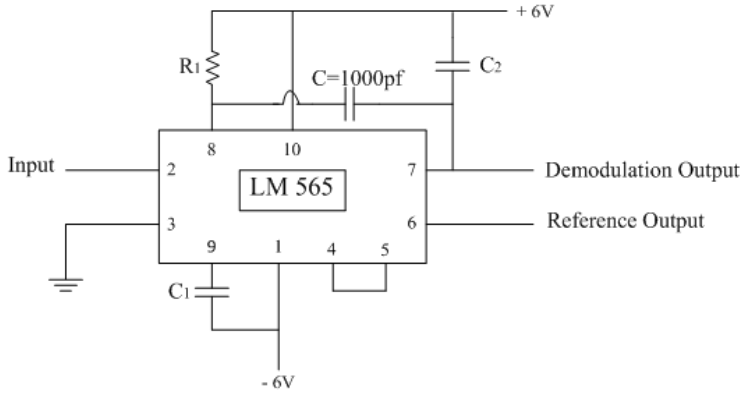
The external frequency (translation frequency) is selected such that it is equal to translation required. In the above example fT = 0.2 MHz.

Thus to achieve the locked condition, the two input frequencies for phase detector must be equal.

$\therefore fo\text{-}fref=fT$

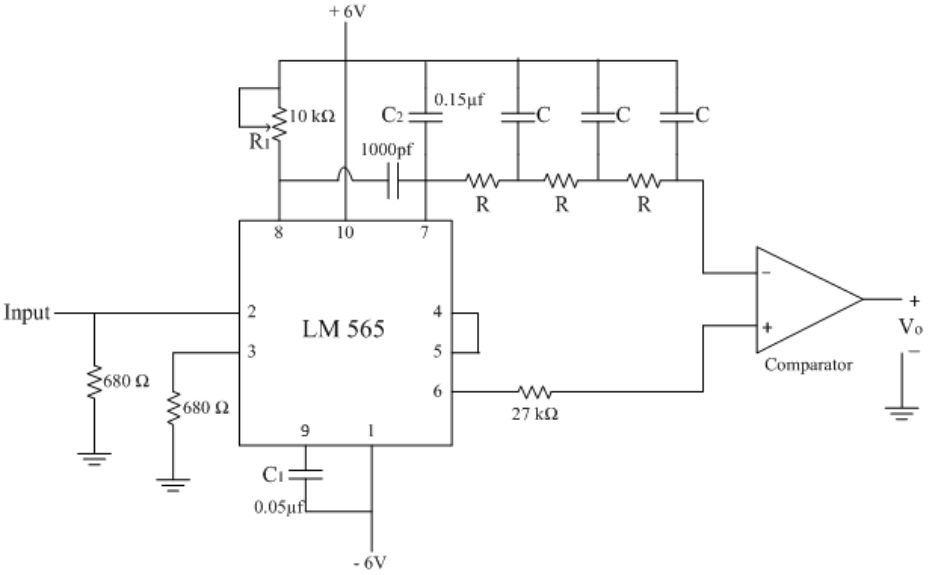
∴fo=fT+fref
∴fo=fT+fref
∴fo=(0.2+1)MHz
∴fo=1.2 MHz
Thus the reference frequency is shifted from 1 MHz to 1.2 MHz and when the locked condition is achieved, this output frequency is highly stable i.e. translated frequency is also stable. Thus by using PLL, from a single reference frequency we can generate number of stable frequencies by this method of translation.
The instrumentation which generates number of frequencies from single reference frequency is called frequency synthesizer.

3. FM Detector:
There is shift in carrier frequency about the mean value according to modulating signal at FM transmitter. The deviation or shift in carrier frequency from centre value is converted to low voltage or high voltage, is demodulation.
Assume the loop is in locked condition, so VCO frequency and input frequency is same. FM signal is applied as input to phase detector. Phase detector produce error voltage proportional to frequency shift. This signal is passed through LPF and amplifier to give controlled voltage. Thus controlled voltage is proportional to change in frequency. As input frequency is shifted up or down, VCO voltage also varies accordingly.
FM input is applied to pin no. 2 which is input to phase detector internally. Pin no. 4 and 5 are shorted externally to complete the loop. Initially loop is locked onto carrier frequency. As carrier frequency changes we get demodulated output at pin no.7. R1 and C1 connected externally, determine the oscillator frequency. An external capacitor of 1000pf is connected for stability of internal circuit. Range of R1 is from 2kΩ to 20kΩ (typically=4kΩ). Direct coupling can be used at input if the dc resistance as seen from pin no. 2 and pin no. 3 are equal and if there is no dc voltage difference these two pins. If resistance is connected between pin no.6 and pin no.7, the gain of output stage can be reduced. The lock range is thus decreased with little change in VCO free running frequency



4. FSK Demodulator:
Two frequencies are used instead of two voltage levels while transmitting signal called FSK modulation. At receiver from these two frequencies we can detect the two voltage levels called FSK demodulation.
In computer peripherals and radio communication binary data or code is transmitted by means of a carrier frequency which is shifted between two predetermined frequencies. The frequencies corresponding to logic 1 and logic 0 states are commonly called as mark and space frequencies. Several standards are used to set the mark and space frequencies. For e.g.when transmitting teletypewriter information using a modem system 1070/1270 Hz pair represents the original signal and the other pair 2025/2225Hz is used as answering unit.
The difference between FSK signals of 1070 and 1270 Hz is 200 Hz and between 2025 and 2225 Hz is also 200 Hz. This is called as frequency shift. Generally binary data is transmitted at the rate of 150 Hz. At receiver end we have to generate two different voltage levels (high & low). The following figure shows the PLL IC 565 as FSK demodulator.
Pin no.4 and pin no.5 shorted externally to get VCO output to phase detector. At pin no.7 the demodulated output is available. This demodulated output is further passed through a 3 identical sections of ladder RC LPF. At the output of 3 LPF sections we get almost a dc voltage. The following

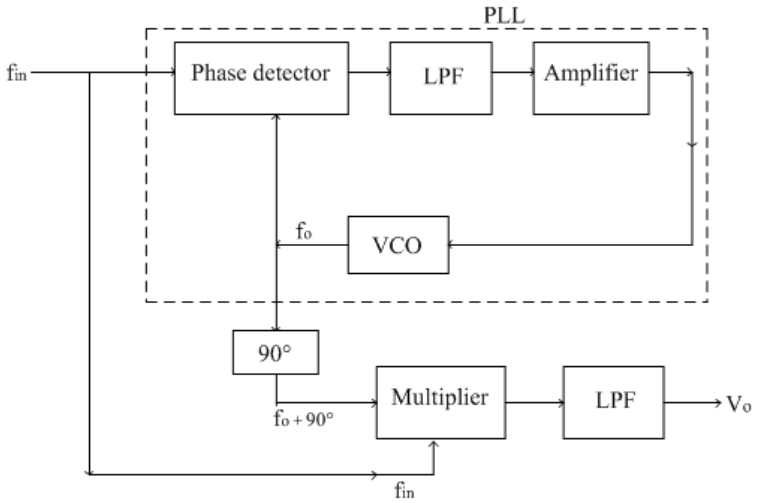
figure shows the PLL IC 565 as FSK demodulator.



This dc voltage is applied to inverting terminal of open loop comparator. At pin no.6 reference dc voltage is present, this is second input to comparator i.e. this is the triggering point for comparator. At pin no.6 we may use RC LPF to get pure dc output. Corresponding to 1070 Hz frequency, we get one signal VC1 at output of 3 RC LPF sections which is connected to comparator. When input frequency is shifted to 1270 Hz, we have another voltage Vc2. The triggering voltage of the comparator is adjusted such that it lies between Vc1 and Vc2. When Vc1 is received at output which is less than VT, then output of comparator is +Vsat. When Vc2 is received at output is more than VT, output of comparator changes to –Vsat. Thus the corresponding two frequencies are converted into two voltage levels +Vsatand –Vsat (high & low) at output; which is nothing but FSK demodulation.

5. AM Detector:

The PLL can be used as an AM detector for demodulating the amplitude modulated signals.
The following figure shows AM detection using PLL.



The equation of AM signal is, E[1+m cos⁡ωm t]cosωc t
where m→Modulation index (0 to 1)
ωm=2πfm→Modulating frequency
ωc=2πfc→Carrier frequency
Amplitude of VCO is constant =Ecos⁡ωc t
These are the two inputs to the multiplier block. The output is the product of the two inputs as calculated below.
=E[1+m cos⁡ωmt]cosωc t [E cos⁡ωc t]
=E^2 [1+m cosωm t] cos^2 ωc t
=E^2 [1+m cos⁡ωm t][(1+cos⁡2ωc t)/2]
Where cos2ωc t〗 →Second harmonics of carrier frequency
When this output signal is passed through LPF, second harmonic is removed.

Video Content / Details of website for further learning (if any): https://www.youtube.com/watch?v=30DaodObd9Q
Important Books/Journals for further learning including the page nos.: **Linear Integrated Circuits 4th Edition by D. Roy Choudhury and Shail B. Jain T1**

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LECTURE HANDOUTS

MDE

II / IV

Course Name with Code : 19MDC04 – LOGIC CIRCUITS FOR CLINICAL ENGINEERS

Course Faculty : Mrs.M.Birunda

Unit : IV - Phase Locked Loops and Data Converters

Date of Lecture:

Topic of Lecture: Data Converters- Sample and hold circuits

Introduction :

Data Conversion is the process of changing or converting one form of data in to another form. In processing and communication there are only two types of data forms i.e analog and digital data. The converter which converts the digital data in to analog data is called analog to digital to analog converter (ADC) and in the same the converter which converts digital to analog is called as DAC.

Prerequisite knowledge for Complete understanding and learning of Topic:

Working of Op amp, Electronic Devices, Analog Electronics, Circuit Theory, Communication Theory

Data Converters- Sample and hold circuits

All the real world quantities are analog in nature. We can represent these quantities electrically as analog signals. An **analog signal** is a time varying signal that has any number of values (variations) for a given time slot.

In contrast to this, a **digital signal** varies suddenly from one level to another level and will have only finite number of values (variations) for a given time slot.

This chapter discusses about the types of data converters and their specifications.

Types of Data Converters

The electronic circuits, which can be operated with analog signals are called as analog circuits. Similarly, the electronic circuits, which can be operated with digital signals are called as digital circuits. A data converter is an electronic circuit that converts data of one form to another.

There are two **types of data converters** −

- Analog to Digital Converter
- Digital to Analog Converter

If we want to connect the output of an analog circuit as an input of a digital circuit, then we have to place an interfacing circuit between them. This interfacing circuit that converts the analog signal into digital signal is called as **Analog to Digital Converter**.

Similarly, if we want to connect the output of a digital circuit as an input of an analog circuit, then

we have to place an interfacing circuit between them. This interfacing circuit that converts the digital signal into an analog signal is called as **Digital to Analog Converter**.

Note that some Analog to Digital Converters may require Digital to Analog Converter as an internal block for their operation.

Specifications

The following are the **specifications** that are related to data conversions −

- Resolution
- Conversion Time

Resolution

Resolution is the **minimum amount of change** needed in an analog input voltage for it to be represented in binary (digital) output. It depends on the number of bits that are used in the digital output.

Mathematically, resolution can be represented as

$$Resolution=12NResolution=12N$$

where, 'N' is the number of bits that are present in the digital output.

From the above formula, we can observe that there exists an **inverse relationship** between the resolution and number of bits. Therefore, resolution decreases as the number of bits increases and vice-versa.

Resolution can also be defined as the ratio of maximum analog input voltage that can be represented in binary and the equivalent binary number.

Mathematically, resolution can be represented as

$$Resolution=VFS2N−1Resolution=VFS2N−1$$

where,

VFSVFS is the full scale input voltage or maximum analog input voltage,

'N' is the number of bits that are present in the digital output.

Conversion Time

The amount of time required for a data converter in order to convert the data (information) of one form into its equivalent data in other form is called as **conversion time**. Since we have two types of data converters, there are two types of conversion times as follows

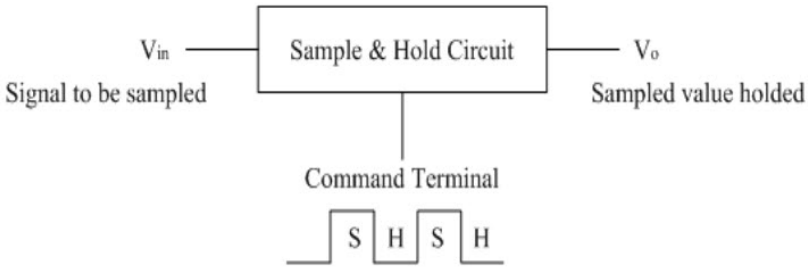
- Analog to Digital Conversion time
- Digital to Analog Conversion time

The amount of time required for an Analog to Digital Converter (ADC) to convert the analog input voltage into its equivalent binary (digital) output is called as **Analog to Digital conversion time**. It depends on the number of bits that are used in the digital output.

The amount of time required for a Digital to Analog Converter (DAC) to convert the binary (digital) input into its equivalent analog output voltage is called as **Digital to Analog conversion time**. It depends on the number of bits that are present in the binary (digital) input.

Sample and Hold Circuit:
A Sample and Hold Circuit, sometimes represented as S/H Circuit or S & H Circuit, is usually used with an Analog to Digital Converter to sample the input analog signal and hold the sampled signal. In the S/H Circuit, the analog signal is sampled for a short interval of time, usually in the range of 10µS to 1µS. After this, the sampled value is hold until the arrival of next input signal to be sampled. The duration for holding the sample will be usually between few milliseconds to few seconds.

The following image shows a simple block diagram of a typical Sample and Hold Circuit.



Need for Sample and Hold Circuits

If the input analog voltage of an ADC changes more than ±1/2 LSB, then there is a severe chance that the output digital value is an error. For the ADC to produce accurate results, the input analog voltage should be held constant for the duration of the conversion.

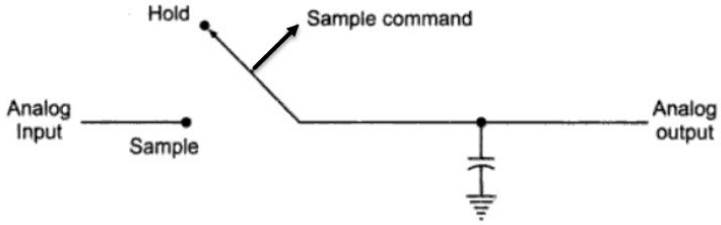
As the name suggests, a S/H Circuit samples the input analog signal based on a sampling command and holds the output value at its output until the next sampling command is arrived.

Simple Sample and Hold Circuit

Let us understand the operating principle of a S/H Circuit with the help of a simplified circuit diagram. This sample and hold circuit consist of two basic components:

- Analog Switch
- Holding Capacitor

The following image shows the basic S/H Circuit.



This circuit tracks the input analog signal until the sample command is changed to hold command. After the hold command, the capacitor holds the analog voltage during the analog to digital conversion.

Analog Switch

Any FET like **JFET** or **MOSFET** can be used as an Analog Switch. In this discussion, we will concentrate on JFET. The Gate-Source voltage V_{GS} is responsible for switching the JFET.

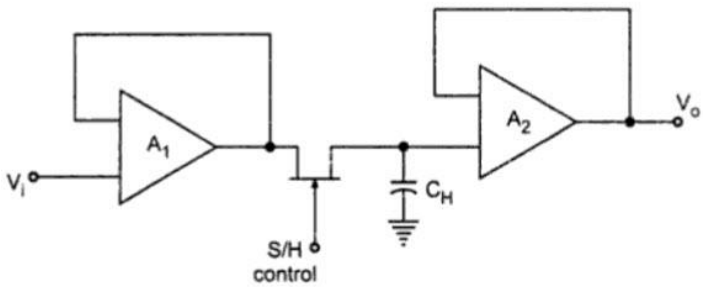
When V_{GS} is equal to 0V, the JFET acts as a closed switch as it operates in its Ohmic region. When V_{GS} is a large negative voltage (i.e. more negative than $V_{GS(OFF)}$), the JFET acts as an open switch as it is cut-off. The switch can be either a Shunt Switch or a Series Switch, depending on its position with respect to input and output.

Types of Sample and Hold Circuits

Let us now see a few different types of Sample and Hold circuits. Note that all the below mentioned circuits use JFET as the switch. During the sampling period, the JFET is turned ON and the charging in the holding capacitor rises to the level of the input analog voltage.

At the end of the sampling period, the JFET is turned OFF and the holding capacitor is isolated from the input signal. This makes sure that the output voltage is held constant at the value of the input voltage irrespective of minor changes in the input value. To compensate for the low drop-out voltage across the holding capacitor, two buffers (voltage followers) are used, one at the input and one at the output.

Keeping this in mind, let us take a look at the first S/H Circuit. The following image shows an open-loop type S/H Circuit.



As there is no feedback, this circuit is relatively faster than the coming circuits (which all are in

closed-loop configuration). But the feedback in the closed-loop architectures provide higher accuracy figures. The acquisition time (discussed in the next section) must be as low as possible. It is dependent on three factors:

- The RC time constant, where R is the ON Resistance of the JFET (r_{on}) and C is the holding capacitor C_H.
- Maximum output current
- Slew-rate of the Op-Amp

A slightly improved circuit than the first one is presented in the next circuit. In this configuration, the ON Resistance of the JFET is brought into the feedback loop and hence, the acquisition time is dependent on the other two factors.The next circuit is further improved when compared to the previous circuit by providing voltage gain. The voltage gain of the circuit can be calculated using the input resistor R_1 and the feedback resistor R_F as follows:

$$A = 1 + (R_F / R_1)$$

The final circuit offers additional advantages than the previous circuit. The important one is that the position of the holding capacitor is changed and as a result, the voltage at non-inverting terminal of A2 is equal to the voltage across the capacitor divided by the open-loop gain of A2.
This ensure a faster charging time of the holding capacitor and subsequently a shorter acquisition time.

Performance Parameters

The performance of an S/H Circuit can be characterized by parameters that are commonly used for an amplifier like Input Offset Voltage, Gain Error, Non-linearity and so on. But there are a few characteristics that are specific to the S/H Circuits.
These characteristics are helpful in analyzing its performance during the transition from sampling mode to hold mode (and vice versa) and also during hold mode operations. Let us understand these characteristics with the help of the following image.

Acquisition Time (t_{ac})

The time required for the charge in the holding capacitor to rise up to a level that is close to the input voltage during the sampling is called acquisition time. It is affected by three factors:

- The RC Time Constant
- The Slew-Rate of the Op-Amp
- The maximum output current of the Op-Amp

Aperture Time (t_{ap})

The time delay between the initiation of V_O tracking the V_i and the initiation of the hold command is called the Aperture Time. This delay is usually due to the propagation delays through the driver and the switch circuits.
For a precise timing operation, the hold command must be initiated in advance by an amount of aperture time.

Aperture Uncertainty (Δt_{ap})

The Aperture time will not be the same for all the sample and will vary from sample to sample. This uncertainty is called Aperture Uncertainty. This will severely affect the advancing of the hold command.

Hold Mode Settling Time (t_s)

The hold mode settling time is the time taken by the output V_O to settle within the specified error band (usually 1%, 0.1% or 0.01%) after the application of hold command.

Hold Step

During the switching from sample mode to hold mode, there might an unwanted transfer of charge between the switch and the holding capacitor (mainly due to the parasitic capacitances). This will affect the capacitor voltage as well as the output voltage. This change in the output voltage from the desired voltage is called Hold Step.

Feedthrough

Again, the parasitic capacitances in the switch may cause AC coupling between V_O and V_i in hold mode. As a result, the output voltage may vary with changes in the input voltage and this is referred to as feedthrough.

Droop

Voltage Droop is a phenomenon where the voltage across the holding capacitor drops down due to leakage currents.

Advantages

- The main and important advantage of a typical SH Circuit is to aid an Analog to Digital Conversion process by holding the sampled analog input voltage.
- In multichannel ADCs, where synchronization between different channels is important, an SH circuit can help by sampling analog signals from all the channels at the same time.
- In multiplexed circuits, the crosstalk can be reduced with an SH circuit.

Applications of Sample and Hold Circuit

Some of the important applications are mentioned below:

- Analog to Digital Converter Circuits (ADC)
- Digital Interface Circuits
- Operational Amplifiers
- Analog De-multiplexers
- Data distribution systems
- Storage of outputs of multiplexers
- Pulse Modulation Systems

Video Content / Details of website for further learning (if any):

https://www.youtube.com/watch?v=6saRcQycX6I

Important Books/Journals for further learning including the page nos.:

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LECTURE HANDOUTS

MDE

II / IV

Course Name with Code : 19MDC04 – LOGIC CIRCUITS FOR CLINICAL ENGINEERS

Course Faculty : Mrs.M.Birunda

Unit : IV - Phase Locked Loops and Data Converters

Date of Lecture:

Topic of Lecture: D/A Techniques: Binary weighted resistors, R-2R ladder DAC

Introduction :

Data Conversion is the process of changing or converting one form of data in to another form. In processing and communication there are only two types of data forms i.e analog and digital data. The converter which converts the digital data in to analog data is called analog to digital to analog converter (ADC) and in the same the converter which converts digital to analog is called as DAC.

Prerequisite knowledge for Complete understanding and learning of Topic:

Working of Op amp, Electronic Devices, Analog Electronics, Circuit Theory, Communication Theory

DAC – Binary weighted resistor DAC

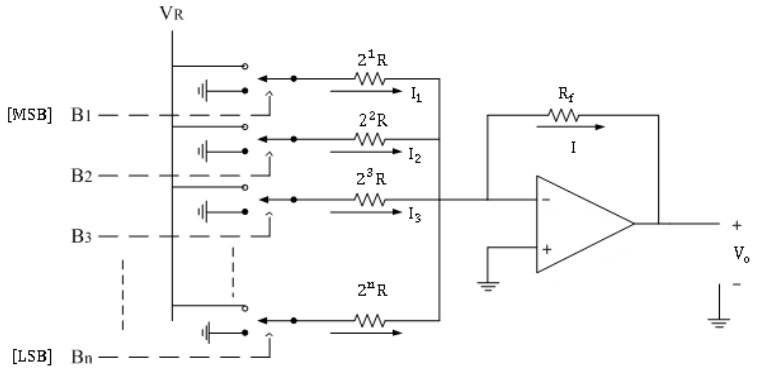
The converter which converters the digital form of data in to analog form is called digital to analog converter. In this the digital data in the form of 1's and 0's are used to control the switches which are placed in a analog circuit with reference voltage, based on this switch condition (ON/OFF) and position (MSB or LSB) the output analog amplitude is calculated.

Types of Digital to Analog Converters

1. Binary Weighted Resistor DAC or R-2^nR DAC
2. R-2R Ladder DAC

Binary Weighted Resistor DAC

In the weighted resistor type DAC, each digital level is converted into an equivalent analog voltage or current. The following figure shows the circuit diagram of the binary weighted resistor type DAC.



It consists of parallel binary weighted resistor bank and a feedback resistor Rf. The switch positions decides the binary word (i.e. B1 B2B3…Bn).
In the circuit op-amp is used as current to voltage converter.

Analysis:

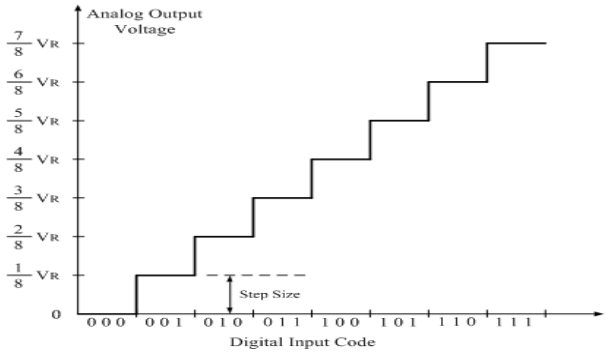
Let us analyze the circuit using normal analysis concepts used in op-amp. When the switches are closed the respective currents are flowing through resistors as shown in the circuit diagram above. Since input current to the op-amp is zero, the addition current flows through feedback resistor.
∴I=I1+I2+I3+ ……+In
The inverting terminal of op-amp is virtually at ground potential. If the reference voltage is positive i.e. + VR, then the output voltage is positive.
Similarly for other six combinations of digital input, the analog output voltage Vo is calculated as follows

$$\therefore V_o = -IR_f$$
$$\therefore V_o = -[I_1 + I_2 + I_3 + \ldots\ldots\ldots + I_n]R_f$$
$$\therefore V_o = -\left[B_1 \frac{V_R}{2^1 R} + B_2 \frac{V_R}{2^2 R} + B_3 \frac{V_R}{2^3 R} + \ldots\ldots + B_n \frac{V_R}{2^n R}\right] R_f$$
$$V_o = -\frac{R_f}{R} V_R [B_1 . 2^{-1} + B_2 . 2^{-2} + B_3 . 2^{-3} + \ldots\ldots + B_n . 2^{-n}]$$
$$If R_f = R$$
$$\therefore V_o = -V_R [B_1 . 2^{-1} + B_2 . 2^{-2} + B_3 . 2^{-3} + \ldots\ldots + B_n . 2^{-n}]$$

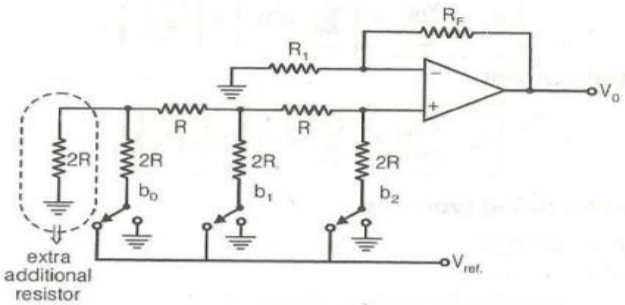
If the reference voltage is positive i.e. + VR, then the output voltage is positive. Similarly for other six combinations of digital input, the analog output voltage Vo is calculated as follows

Sr. No.	Digital Input B_1	B_2	B_3	Analog Output, V_o (V) (When V_R is Positive)	Analog Output, V_o (V) (When V_R is negative)
01	0	0	0	0	0
02	0	0	1	$-\frac{V_R}{8}$	$+\frac{V_R}{8}$
03	0	1	0	$-\frac{2V_R}{8}$	$+\frac{2V_R}{8}$
04	0	1	1	$-\frac{3V_R}{8}$	$+\frac{3V_R}{8}$
05	1	0	0	$-\frac{4V_R}{8}$	$+\frac{4V_R}{8}$
06	1	0	1	$-\frac{5V_R}{8}$	$+\frac{5V_R}{8}$
07	1	1	0	$-\frac{6V_R}{8}$	$+\frac{6V_R}{8}$

The following figure shows the staircase output voltage waveform obtained for R-2R ladder DAC (when VR is positive).



Disadvantages:
1) When number of binary input increases, it is not easy to maintain the resistance ratio.
2) Very wide ranges of different values of resistors are required. For high accuracy of conversion, the values of resistances must be accurate.
3) Different current flows through resistors, so their wattage ratings are also different.
4) Accuracy and stability of conversion depends primarily on the absolute accuracy of the resistors and tracking of each other with temperature.
eg. For 10 digit converter
small resistance value = 10 kΩ and
large resistance value = 5.12 MΩ
It is very difficult and expensive to obtain stable precise resistances of such value.
5) Since 'R' is very large, op-amp bias currents gives a drop which offsets output.
6) Resistances of switches may be comparable with smallest resistor.



R-2R non-inverting Ladder DAC

DAC Output Voltage:-

$$V_0 = \frac{V_{ref.}}{2^N}\left[\sum_{i=0}^{N-1} 2^i b_i\right] \times \left[1 + \frac{R_F}{R_1}\right]$$

R-2R Ladder DAC Non-Inverting Type ...Equation-1

Video Content / Details of website for further learning (if any):
https://www.youtube.com/watch?v=Pc1aFloxSMw
https://www.youtube.com/watch?v=jDn1eXijQdY

Important Books/Journals for further learning including the page nos.:
Linear Integrated Circuits 4th Edition by D. Roy Choudhury and Shail B. Jain T1

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LECTURE HANDOUTS

L 34

MDE

II / IV

Course Name with Code : 19MDC04 – LOGIC CIRCUITS FOR CLINICAL ENGINEERS

Course Faculty : Mrs.M.Birunda

Unit : IV - Phase Locked Loops and Data Converters

Date of Lecture:

Topic of Lecture: Inverted R-2R ladder DAC, A/D Converter: Flash type

Introduction :

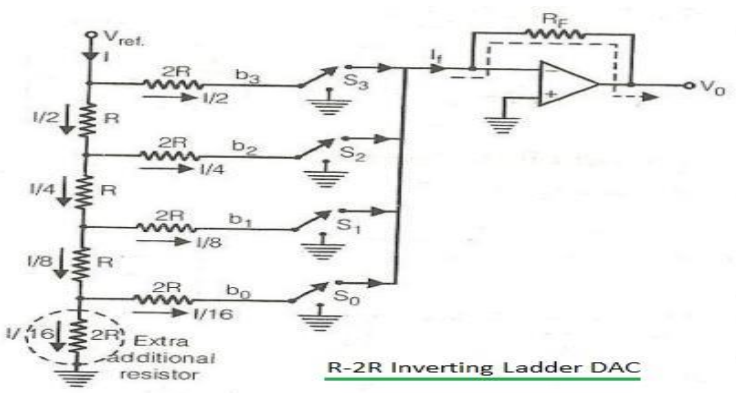
Data Conversion is the process of changing or converting one form of data in to another form. In processing and communication there are only two types of data forms i.e analog and digital data. The converter which converts the digital data in to analog data is called analog to digital to analog converter (ADC) and in the same the converter which converts digital to analog is called as DAC.

Prerequisite knowledge for Complete understanding and learning of Topic:

Working of Op amp, Electronic Devices, Analog Electronics, Circuit Theory, Communication Theory

Inverted R-2R ladder or current mode DAC

As the name implies, Current mode DACs operates based on the ladder currents. The ladder is formed by resistance R in the series path and resistance 2R in the shunt path. Thus the current is divided into i1 , i2, i3 ……in. in each arm. The currents are either diverted to the ground bus (io) or to the Virtual-ground bus (io).



R-2R Inverting Ladder DAC

$$V_0 = \frac{V_{ref.}}{2^N} \times \left[\sum_{i=0}^{N-1} 2^i b_i\right] \times \left(\frac{-R_F}{R}\right)$$

R-2R Ladder DAC Inverting Type Equation-2

Advantages:
• Only two resistor values are used in R-2R ladder type.
• It does not need as precision resistors as Binary weighted DACs.
• It is cheap and easy to manufacture.

Disadvantages:
• It has slower conversion rate.
For N bit DAC:
• Number of different levels = 2^N
• Number of Steps = $2^N - 1$
Resolution or step size of DAC = Analog output/Number of steps = Va/($2^N - 1$)
% Resolution = (Step Size/Full scale output) x 100 %

Analog to Digital Converter

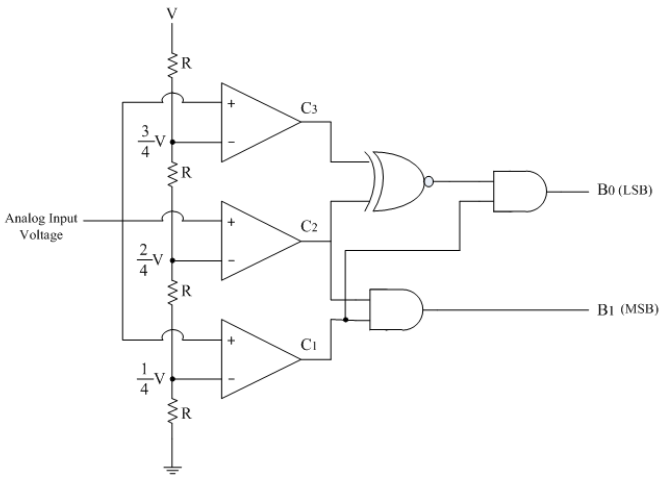
The data converter which converts the data from analog values to digital values is called Analog to Digital converter in shot it is called ADC. In ADC the input signal value is sampled at a particular time interval and compared with the analog value produced by the combination of counter and DAC. If the output of the comparator is zero then the value of the counter will be the output digital value. These are very important converters as the environmental analog signals has too be converted in to digital for processing with the digital computer.

Types of Analog to Digital Converters:

1. Simultaneous or Flash A/D Converters
2. Counter-Type A/D Converter
3. Tracking-Type A/D Converter
4. Successive Approximation Type A/D Converter
5. Single-, Dual- and Multislope A/D Converters
6. Sigma-Delta A/D Converter

Flash Type ADC

Flash Type ADC is based on the principle of comparing analog input voltage with a set of reference voltages.
To convert the analog input voltage into a digital signal of n-bit output, (2^n – 1) comparators are required.
The following figure shows 2- bit flash type ADC



The three op-amps are used as comparators. The non-inverting inputs of all the three comparators are connected to the analog input voltage. The inverting terminals are connected to a set of reference voltages (V/4), (2V/4) and (3V/4) respectively which are obtained using a resistive divider network and power supply +V.
The output of the comparator is in positive saturation(i.e. logic 1), when voltage at non-inverting terminal is greater than voltage at inverting terminal and is in negative saturation otherwise.
The following table shows the comparator outputs for different ranges of analog input voltages and their corresponding digital outputs.

Analog Input Conditions	Comparator Outputs			Digital output	
	C_1	C_2	C_3	B_1	B_0
$0 \leq V_{in} \leq \frac{V}{4}$	0	0	0	0	0
$\frac{V}{4} \leq V_{in} \leq \frac{2V}{4}$	1	0	0	0	1
$\frac{2V}{4} \leq V_{in} \leq \frac{3V}{4}$	1	1	0	1	0
$\frac{3V}{4} \leq V_{in} \leq V$	1	1	1	1	1

Consider first condition, where analog input voltage VA is less than (V/4). In this case, the voltage at the non-inverting terminals of all the three comparators is less than the respective voltages at inverting terminals and hence the comparator outputs are C1C2C3 = 000. This comparator outputs are applied to the further coding circuit to get the digital outputs as B1B0 = 00 Similarly the digital outputs are calculated for other three conditions also.

Advantages:

1)It is the fastest type of ADC because the conversion is performed simultaneously through a set of comparators, hence referred as flash type ADC. Typical conversion time is 100ns or less.
2)The construction is simple and easier to design.

Disadvantages:

1)It is not suitable for higher number of bits.
2)To convert the analog input voltage into a digital signal of n-bit output, $(2^n - 1)$ comparators are required. The number of comparators required doubles for each added bit.

Video Content / Details of website for further learning (if any):

https://www.youtube.com/watch?v=q6WVxBs82IQ
https://www.youtube.com/watch?v=A9NinZYWyo8

Important Books/Journals for further learning including the page nos.:

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LECTURE HANDOUTS

L 35

MDE

II / IV

Course Name with Code : 19MDC04 – LOGIC CIRCUITS FOR CLINICAL ENGINEERS

Course Faculty : Mrs.M.Birunda

Unit : IV - Phase Locked Loops and Data Converters

Date of Lecture:

Topic of Lecture: Counter – Successive approximation converter

Introduction :

Data Conversion is the process of changing or converting one form of data in to another form. In processing and communication there are only two types of data forms i.e analog and digital data. The converter which converts the digital data in to analog data is called analog to digital to analog converter (ADC) and in the same the converter which converts digital to analog is called as DAC.

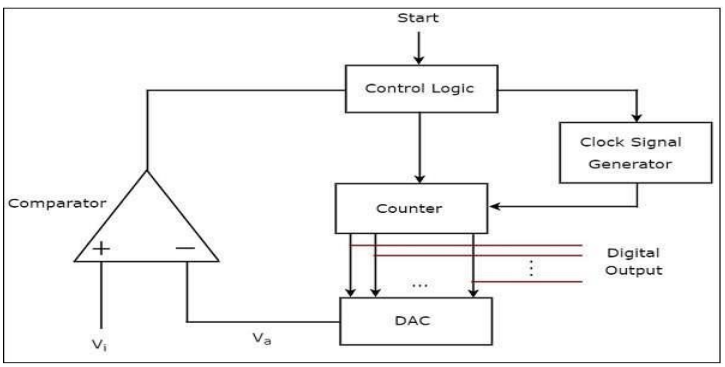
Prerequisite knowledge for Complete understanding and learning of Topic:

Working of Op amp, Electronic Devices, Analog Electronics, Circuit Theory, Communication Theory

Counter Type ADC (Analog to Digital Converter)

A **counter type ADC** produces a digital output, which is approximately equal to the analog input by using counter operation internally.

The **block diagram** of a counter type ADC is shown in the following figure −



The counter type ADC mainly consists of 5 blocks: Clock signal generator, Counter, DAC, Comparator and Control logic.

The **working** of a counter type ADC is as follows −

- The **control logic** resets the counter and enables the clock signal generator in order to send the clock pulses to the counter, when it received the start commanding signal.

- The **counter** gets incremented by one for every clock pulse and its value will be in binary (digital) format. This output of the counter is applied as an input of DAC.
- **DAC** converts the received binary (digital) input, which is the output of counter, into an analog output. Comparator compares this analog value,VaVa with the external analog input value ViVi.
- The **output of comparator** will be **'1'** as long as Vi is greater than. The operations mentioned in above two steps will be continued as long as the control logic receives '1' from the output of comparator.
- The **output of comparator** will be **'0'** when ViVi is less than or equal to VaVa. So, the control logic receives '0' from the output of comparator. Then, the control logic disables the clock signal generator so that it doesn't send any clock pulse to the counter.
- At this instant, the output of the counter will be displayed as the **digital output**. It is almost equivalent to the corresponding external analog input value ViVi

Conversion time of Counter type ADC

Conversion time of ADC is the time taken by the ADC to convert the input sampled analog value to digital value. Here the maximum conversion of high input voltage for a N bit ADC is the clock pulses required to the counter to count its maximum count value. So

The maximum conversion of Counter type ADC is = (2^N-1) T

Where, T is the time period of clock pulse.

If N=2 bit then the T_{max} = 3T.

By observing the above conversion time of Counter type ADC it is illustrated that the sampling period of Counter type ADC should be as shown below.

Ts >= (2^N-1) T

Advantages of Counter type ADC

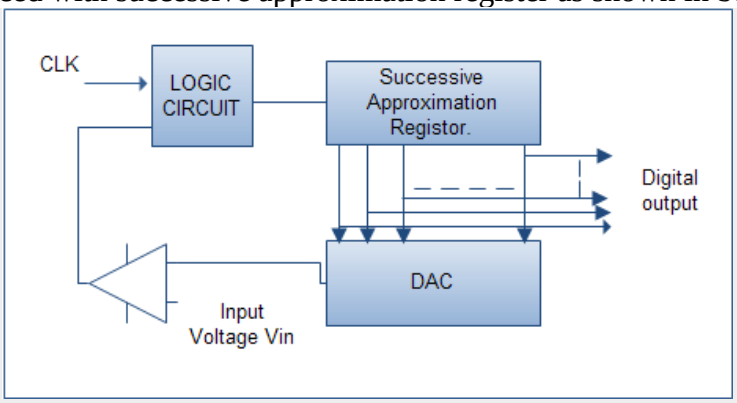
- Simple to understand and operate.
- Cost is less because of less complexity in design.

Disadvantages or limitations of Counter type of ADC

- Speed is less because every time the counter has to start from ZERO.
- There may be clash or aliasing effect if the next input is sampled before completion of one operation.

Successive Approximation ADC (Analog to Digital Converter)

Successive approximation ADC is the advanced version of Digital ramp type ADC which is designed to reduce the conversion and to increase speed of operation. In successive approximation ADC the normal counter is replaced with successive approximation register as shown in below figure.



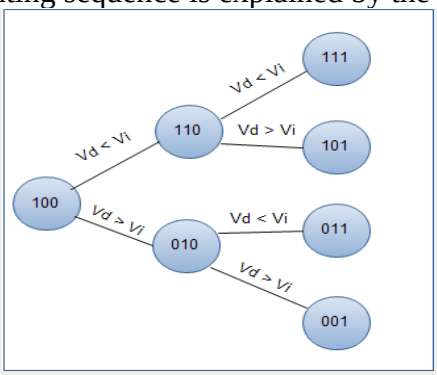
Successive Approximation ADC

The successive approximation register counts by changing the bits from MSB to LSB according to input. The detailed operation is shown below.

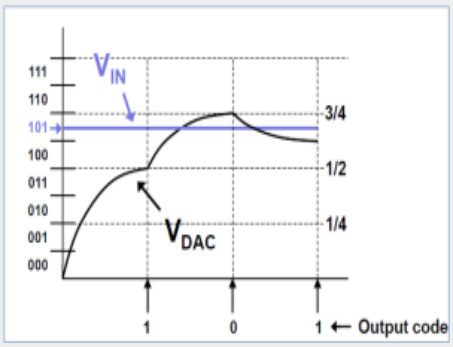
Operation of 3 bit Successive Approximation ADC

The output of SAR is converted to analog out by the DAC and this analog output is compared with the input analog sampled value in the Opamp comparator. This Opamp provides an high or low clock pulse based on the difference through the logic circuit. In very first case the 3 bit SAR enables its MSB bit as high i.e. '1' and the result will be "100". This digita output is converted to analog value and compared with input sampled voltage (V_{in}). If the deference is positive i.e. if the sampled input is high then the

SAR enables the next bit from MSB and result will be “110”. Now if the output is negative i.e. if the input sampled voltage is less than the SAR resets the last set bit and sets the next bit and resultant output in this case will be “101” which will definitely approximately equal to the input analog value. The counting sequence is explained by the following counter flow chat as shown in below.



Successive Approximation ADC Flow chat



SAR ADC input output flow voltage graph

Conversion time of Successive Approximation ADC

By observing above 3 bit example it is illustrated for a 3 bit ADC the conversion time will be 3 clock pulses. Then;

N bit Successive Approximation ADC conversion time = 3T (T- clock pulse).

Advantages of Successive Approximation ADC

- Speed is high compared to counter type ADC.
- Good ratio of speed to power.
- Compact design compared to Flash Type and it is inexpensive.

Disadvantages of Successive Approximation ADC

- Cost is high because of SAR
- Complexity in design.

Applications

The SAR ADC will used widely data acquisition techniques at the sampling rates higher than 10KH

Video Content / Details of website for further learning (if any):

Important Books/Journals for further learning including the page nos.:
Linear Integrated Circuits 4th Edition by D. Roy Choudhury and Shail B. Jain T1

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LECTURE HANDOUTS | **L 36**

MDE | **II / IV**

Course Name with Code : 19MDC04 – LOGIC CIRCUITS FOR CLINICAL ENGINEERS

Course Faculty : Mrs.M.Birunda

Unit : IV - Phase Locked Loops and Data Converters

Date of Lecture:

Topic of Lecture: Single slope and dual slope ADC

Introduction :

Data Conversion is the process of changing or converting one form of data in to another form. In processing and communication there are only two types of data forms i.e analog and digital data. The converter which converts the digital data in to analog data is called analog to digital to analog converter (ADC) and in the same the converter which converts digital to analog is called as DAC.

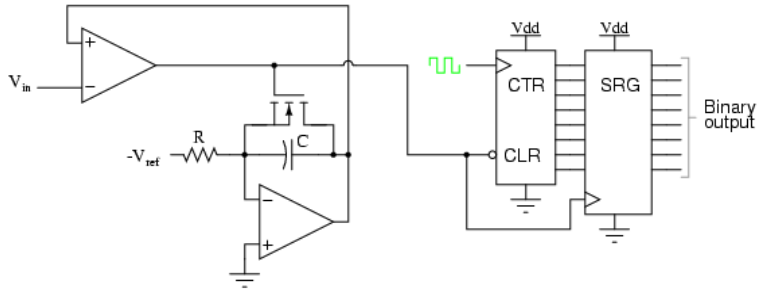
Prerequisite knowledge for Complete understanding and learning of Topic:

Basic Analog electronics and Electronic Devices, and Circuit theory,

Basic constant current source working and its necessity

Single slope ADC:

The is the basic idea behind the so-called *single-slope*, or *integrating* ADC. Instead of using a DAC with a ramped output, we use an op-amp circuit called an *integrator* to generate a sawtooth waveform which is then compared against the analog input by a comparator. The time it takes for the sawtooth waveform to exceed the input signal voltage level is measured by means of a digital counter clocked with a precise-frequency square wave (usually from a crystal oscillator). The basic schematic diagram is shown here:



The IGFET capacitor-discharging transistor scheme shown here is a bit oversimplified. In reality, a latching circuit timed with the clock signal would most likely have to be connected to the IGFET gate to ensure full discharge of the capacitor when the comparator's output goes high. The basic idea, however, is evident in this diagram. When the comparator output is low (input voltage greater than

integrator output), the integrator is allowed to charge the capacitor in a linear fashion. Meanwhile, the counter is counting up at a rate fixed by the precision clock frequency. The time it takes for the capacitor to charge up to the same voltage level as the input depends on the input signal level and the combination of $-V_{ref}$, R, and C. When the capacitor reaches that voltage level, the comparator output goes high, loading the counter's output into the shift register for a final output. The IGFET is triggered "on" by the comparator's high output, discharging the capacitor back to zero volts. When the integrator output voltage falls to zero, the comparator output switches back to a low state, clearing the counter and enabling the integrator to ramp up voltage again. This ADC circuit behaves very much like the digital ramp ADC, except that the comparator reference voltage is a smooth sawtooth waveform rather than a "stairstep:"

The single-slope ADC suffers all the disadvantages of the digital ramp ADC, with the added drawback of *calibration drift*. The accurate correspondence of this ADC's output with its input is dependent on the voltage slope of the integrator being matched to the counting rate of the counter (the clock frequency). With the digital ramp ADC, the clock frequency had no effect on conversion accuracy, only on update time. In this circuit, since the rate of integration and the rate of count are independent of each other, variation between the two is inevitable as it ages, and will result in a loss of accuracy. The only good thing to say about this circuit is that it avoids the use of a DAC, which reduces circuit complexity.

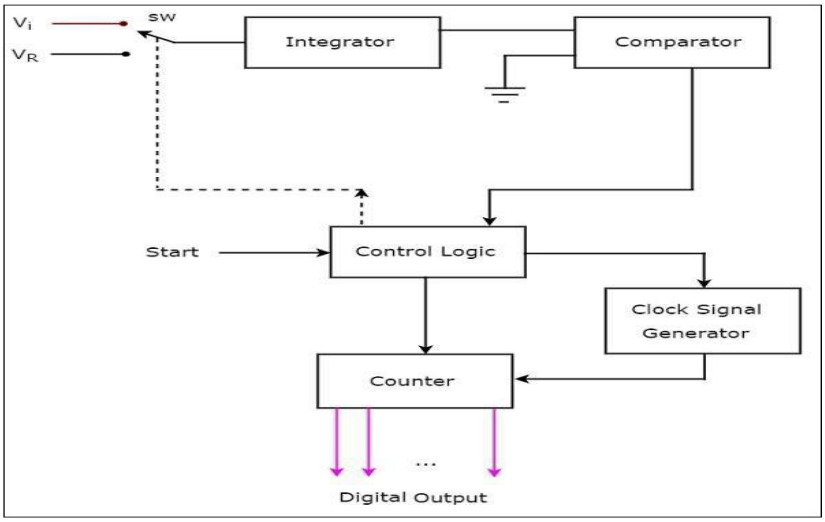
Dual slope ADC

If an ADC performs the analog to digital conversion by an indirect method, then it is called an **Indirect type ADC**. In general, first it converts the analog input into a linear function of time (or frequency) and then it will produce the digital (binary) output. Dual slope ADC is the best **example** of an Indirect type ADC. This chapter discusses about it in detail.

Dual Slope ADC

As the name suggests, a **dual slope ADC** produces an equivalent digital output for a corresponding analog input by using two (dual) slope technique.

The **block diagram** of a dual slope ADC is shown in the following figure −



The dual slope ADC mainly consists of 5 blocks: Integrator, Comparator, Clock signal generator, Control logic and Counter.

The **working** of a dual slope ADC is as follows −

- The **control logic** resets the counter and enables the clock signal generator in order to send the clock pulses to the counter, when it is received the start commanding signal.
- Control logic pushes the switch **sw** to connect to the **external analog input voltage** ViVi, when it is received the start commanding signal. This input voltage is applied to an integrator.
- The output of the **integrator** is connected to one of the two inputs of the comparator and the other input of comparator is connected to ground.

- **Comparator** compares the output of the integrator with zero volts (ground) and produces an output, which is applied to the control logic.
- The **counter** gets incremented by one for every clock pulse and its value will be in binary (digital) format. It produces an overflow signal to the control logic, when it is incremented after reaching the maximum count value. At this instant, all the bits of counter will be having zeros only.
- Now, the control logic pushes the switch **sw** to connect to the **negative reference** voltage −Vref−Vref. This negative reference voltage is applied to an integrator. It removes the charge stored in the capacitor until it becomes zero.
- At this instant, both the inputs of a comparator are having zero volts. So, comparator sends a signal to the control logic. Now, the control logic disables the clock signal generator and retains (holds) the counter value. The **counter value** is proportional to the external analog input voltage.
- At this instant, the output of the counter will be displayed as the **digital output**. It is almost equivalent to the corresponding external analog input value Vi

Video Content / Details of website for further learning (if any):
https://www.youtube.com/watch?v=K07T1dSnwxY

Important Books/Journals for further learning including the page nos.:
Linear Integrated Circuits 4th Edition by D. Roy Choudhury and Shail B. Jain T1

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LECTURE HANDOUTS

MDE

II/IV

Course Name with Code : 19MDC04 – LOGIC CIRCUITS FOR CLINICAL ENGINEERS

Course Faculty : Mrs.M.Birunda

Unit : V – Specialized IC Applications

Date of Lecture:

Topic of Lecture: Timer IC 555 Internal Architecture

Introduction : The 555 timer IC is an integrated circuit (chip) used in a variety of timer, pulse generation, and oscillator applications. The 555 can be used to provide time delays, as an oscillator, and as a flip-flop element. Derivatives provide two (556) or four (558) timing circuits in one package.

Prerequisite knowledge for Complete understanding and learning of Topic:

Operation of Op Amp, Basic Analog electronics and Electronic Devices, and Circuit theory

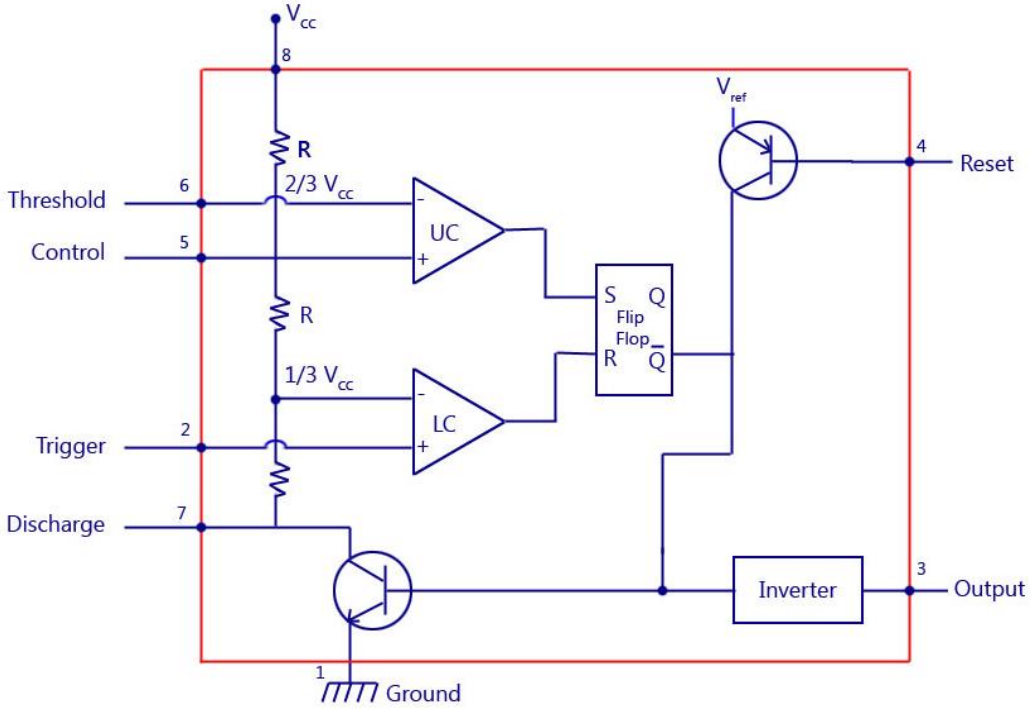
555 IC Timer Block Diagram

The block diagram of a **555 timer** is shown in the above figure. A 555 timer has two comparators, which are basically 2 op-amps), an R-S flip-flop, two transistors and a resistive network.

Resistive network consists of three equal resistors and acts as a voltage divider.
Comparator 1 compares threshold voltage with a reference voltage + 2/3 VCC volts.
Comparator 2 compares the trigger voltage with a reference voltage + 1/3 VCC volts.

Working Principle

The internal resistors act as a voltage divider network, providing (2/3)Vcc at the non-inverting terminal of the upper comparator and (1/3)Vcc at the inverting terminal of the lower comparator. In most applications, the control input is not used, so that the control voltage equals +(2/3) VCC. Upper comparator has a threshold input (pin 6) and a control input (pin 5). Output of the upper comparator is applied to set (S) input of the flip-flop. Whenever the threshold voltage exceeds the control voltage, the upper comparator will set the flip-flop and its output is high.



A high output from the flip-flop when given to the base of the discharge transistor saturates it and thus discharges the transistor that is connected externally to the discharge pin 7. The complementary signal out of the flip-flop goes to pin 3, the output. The output available at pin 3 is low. These conditions will prevail until lower comparator triggers the flip-flop. Even if the voltage at the threshold input falls below (2/3) VCC, that is upper comparator cannot cause the flip-flop to change again. It means that the upper comparator can only force the flip-flop's output high.

To change the output of flip-flop to low, the voltage at the trigger input must fall below + (1/3) Vcc. When this occurs, lower comparator triggers the flip-flop, forcing its output low. The low output from the flip-flop turns the discharge transistor off and forces the power amplifier to output a high. These conditions will continue independent of the voltage on the trigger input. Lower comparator can only cause the flip-flop to output low.

From the above discussion, it is concluded that for the having low output from the timer 555, the voltage on the threshold input must exceed the control voltage or + (2/3) VCC. This also turns the discharge transistor on. To force the output from the timer high, the voltage on the trigger input must drop below +(1/3) VCC. This turns the discharge transistor off.

A voltage may be applied to the control input to change the levels at which the switching occurs. When not in use, a 0.01 nano Farad capacitor should be connected between pin 5 and ground to prevent noise coupled onto this pin from causing false triggering.

Connecting the reset (pin 4) to a logic low will place a high on the output of flip-flop. The discharge transistor will go on and the power amplifier will output a low. This condition will continue until reset is taken high. This allows the synchronization or resetting of the circuit's operation. When not in use, reset should be tied to +VCC.

555 Timer Pin Diagram and Descriptions

There are eight pins for a 555 Timer IC namely,

1.Ground.

2.Trigger.

3.Output.

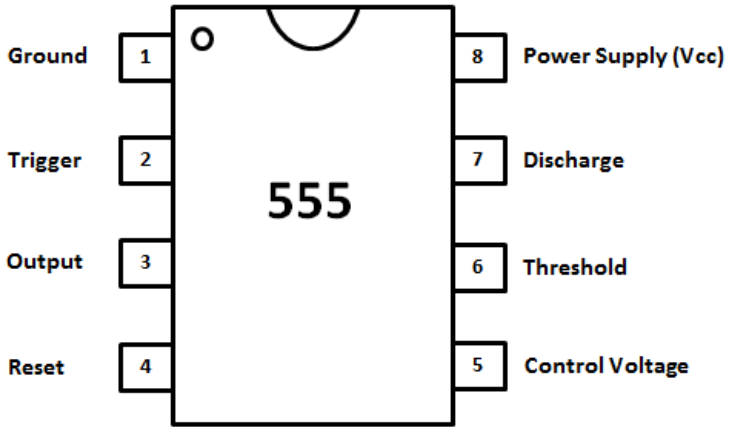
4.Reset.

5.Control

6.Threshold.

7.Discharge

8.Power or Vcc



Pin 1. Ground: This pin has no special function what so ever. It is connected to ground as usual. For the timer to function, this pin must and should be connected to ground.

Pin 8. Power or VCC: This pin also has no special function. It is connected to positive voltage. For the timer to function to work, this pin must be connected to positive voltage of range +3.6v to +15v.

Pin 4. Reset: As discussed earlier, there is a flip-flop in the timer chip. The output of flip-flop controls the chip output at pin3 directly.

Pin 3. OUTPUT: This pin also has no special function. This pin is drawn from PUSH-PULL configuration formed by transistors.

Pin 5. Conrol Pin: The control pin is connected from the negative input pin of comparator one.

Pin 2. TRIGGER: Trigger pin is dragged from the negative input of comparator two. The comparator two output is connected to SET pin of flip-flop. With the comparator two output high we get high voltage at the timer output. So we can say the trigger pin controls timer output.

Pin 6. THRESHOLD: Threshold pin voltage determines when to reset the flip-flop in the timer. The threshold pin is drawn from positive input of comparator1.

Pin 7. DISCHARGE: This pin is drawn from the open collector of transistor. Since the transistor (on which discharge pin got taken, Q1) got its base connected to Qbar.

Video Content / Details of website for further learning (if any):

Can be added as link
https://www.youtube.com/watch?v=EGmreVQ-yNM
https://www.youtube.com/watch?v=WkI7uYLRbwQ
http://www.circuitstoday.com/555-timer

Important Books/Journals for further learning including the page nos.:

Linear Integrated Circuits By D. Roy Choudhury, Shail B. Jain T1

Course Faculty

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L 38

LECTURE HANDOUTS

MDE

II/IV

Course Name with Code : 19MDC04 – LOGIC CIRCUITS FOR CLINICAL ENGINEERS

Course Faculty : Mrs.M.Birunda

Unit : V – Specialized IC Applications

Date of Lecture:

Topic of Lecture: Astable multivibrator using 555

Introduction : An astable multivibrator can be designed using different types of components, say using transistors (and associated components) alone or by using op amps (and associated components).

Prerequisite knowledge for Complete understanding and learning of Topic:
Operation of Op Amp, Basic Analog electronics and Electronic Devices, and Circuit theory

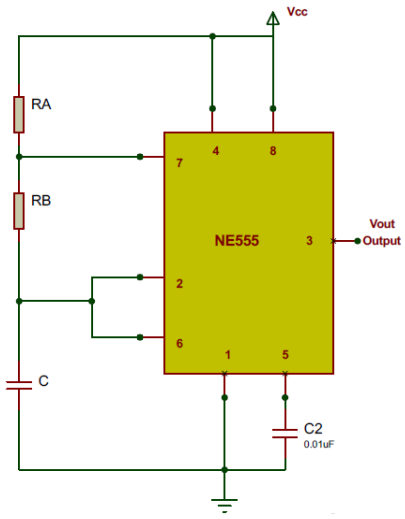
555 Timer Astable Multivibrator

An Astable Multivibrator can be designed by adding two resistors (RA and RB in circuit diagram) and a capacitor (C in circuit diagram) to the 555 Timer IC. These two resistors and the capacitor (values) are selected appropriately so as to obtain the desired 'ON' and 'OFF' timings at the output terminal (pin 3). So basically, the ON and OFF time at the output (i.e the 'HIGH' and 'LOW' state at the output terminal) is dependent on the values chosen for RA,RB and C. We will see more about this on the astable multivibrator design section given below.

The Connections

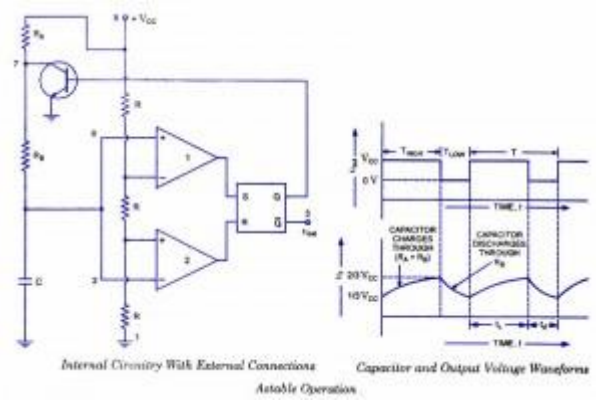
Let's see how the 555 timer astable multivibrator connections are made in the circuit diagram.

Pin 1 is grounded; pins **4 and 8** are shorted and then tied to supply **+Vcc**, Output (**Vout**) is taken from **pin 3**; pin **2 and 6** are shorted and then connected to ground through the **capacitor C to ground terminal**, pin **7** is connected to supply **+ VCC** through a **resistor RA**; and between **pin 6 and 7** a resistor **RB is connected**. At **pin 5** either a bypass capacitor (to bypass noise signals) of **0.01uF is connected** or modulation input is applied.



Astable Multivibrator Working

So far we have seen how an astable multivibrator is designed using 555 timer IC, the circuit diagram and how the pin connections are made. Now let's see the operation and working of an astable multivibrator. To explain the 555 timer astable multivibrator working, we have drawn an internal circuit diagram of 555 timer IC (consisting of two Op Amps, an SR Flip Flop and the transistor connected at the discharging terminal – pin 7) along with the necessary external connections (RA, RB and C). Wave forms from the output terminal (Vout – pin 3) is shown towards the right side of the circuit diagram. Carefully observe the circuit diagram and the output waveforms before we begin the explanation.



Internal Circuitry With External Connections — Capacitor and Output Voltage Waveforms

Astable Operation

Video Content / Details of website for further learning (if any):

Can be added as link

http://www.circuitstoday.com/555-timer-astable-multivibrator
https://www.youtube.com/watch?v=uJepMb2KP50
https://www.youtube.com/watch?v=wN6g_q3KPtw
https://www.youtube.com/watch?v=iJYm_BGqa1A

Important Books/Journals for further learning including the page s

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LECTURE HANDOUTS

MDE

II/IV

Course Name with Code : 19MDC04 – LOGIC CIRCUITS FOR CLINICAL ENGINEERS

Course Faculty : Mrs.M.Birunda

Unit : V – Specialized IC Applications

Date of Lecture:

Topic of Lecture: Monostable multivibrator using 555

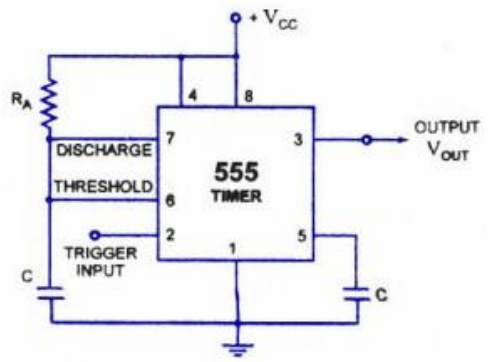
Introduction : A monostable multivibrator (MMV) often called a one-shot multivibrator, is a pulse generator circuit in which the duration of the pulse is determined by the R-C network,connected externally to the 555 timer. In such a vibrator, one state of output is stable while the other is quasi-stable (unstable).

Prerequisite knowledge for Complete understanding and learning of Topic:
Operation of Op Amp, Basic Analog electronics and Electronic Devices, and Circuit theory

Monostable Multivibrator

A Monostable Multivibrator *(MMV) often called a one-shot multivibrator,* is a pulse generator circuit in which the duration of the pulse is determined by the R-C network,connected externally to the 555 timer. In such a vibrator, one state of output is stable while the other is quasi-stable (unstable). For auto-triggering of output from quasi-stable state to stable state energy is stored by an externally connected capacitor C to a reference level.

The time taken in storage determines the pulse width. The transition of output from stable state to quasi-stable state is accomplished by external triggering. The schematic of a 555 timer in monostable mode of operation is shown in figure.

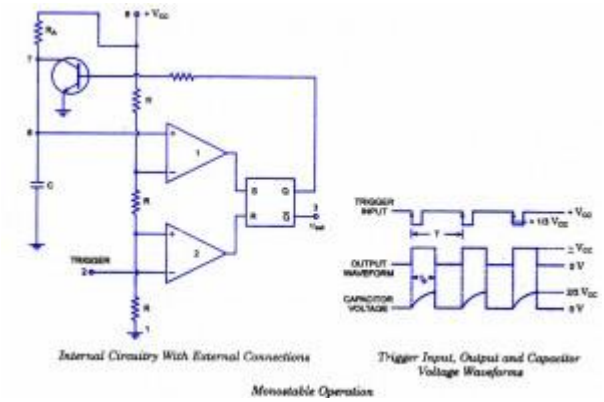


Circuit of The Timer 555 as a Monostable Multivibrator

Monostable Multivibrator PIN Description

Pin 1 is grounded. Trigger input is applied to pin 2. In quiescent condition of output this input is kept at + VCC. To obtain transition of output from stable state to quasi-stable state, a negative-going pulse of narrow width (a width smaller than expected pulse width of output waveform) and amplitude of greater than + 2/3 VCC is applied to pin 2. Output is taken from pin 3. Pin 4 is usually connected to + VCC to avoid accidental reset. Pin 5 is grounded through a 0.01 u F capacitor to avoid noise problem. Pin 6 (threshold) is shorted to pin 7. A resistor RA is connected between pins 6 and 8. At pins 7 a discharge capacitor is connected while pin 8 is connected to supply VCC.

555 IC Monostable Multivibrator Operation.



Internal Circuitry With External Connections *Trigger Input, Output and Capacitor Voltage Waveforms*

Monostable Operation

Operation Of The Circuit

Initially, when the output at pin 3 is low i.e. the circuit is in a stable state, the transistor is on and capacitor- C is shorted to ground. When a negative pulse is applied to pin 2, the trigger input falls below +1/3 VCC, the output of comparator goes high which resets the flip-flop and consequently the transistor turns off and the output at pin 3 goes high. This is the transition of the output from stable to quasi-stable state, as shown in figure. As the discharge transistor is cutoff, the capacitor C begins charging toward +VCC through resistance RA with a time constant equal to RAC. When the increasing capacitor voltage becomes slightly greater than +2/3 VCC, the output of comparator 1 goes high, which sets the flip-flop. The transistor goes to saturation, thereby discharging the capacitor C and the output of the timer goes low, as illustrated in figure.

Thus the output returns back to stable state from quasi-stable state.

The output of the Monostable Multivibrator remains low until a trigger pulse is again applied.

Video Content / Details of website for further learning (if any):

Can be added as link

http://www.circuitstoday.com/555-timer-as-monostable-multivibrator
https://www.youtube.com/watch?v=pUibCkUB364
https://www.youtube.com/watch?v=nTm-fB1OrqE

Important Books/Journals for further learning including the page s

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LECTURE HANDOUTS

MDE

II/IV

Course Name with Code : 19MDC04 – LOGIC CIRCUITS FOR CLINICAL ENGINEERS

Course Faculty : Mrs.M.Birunda

Unit : V – Specialized IC Applications

Date of Lecture:

Topic of Lecture: Applications

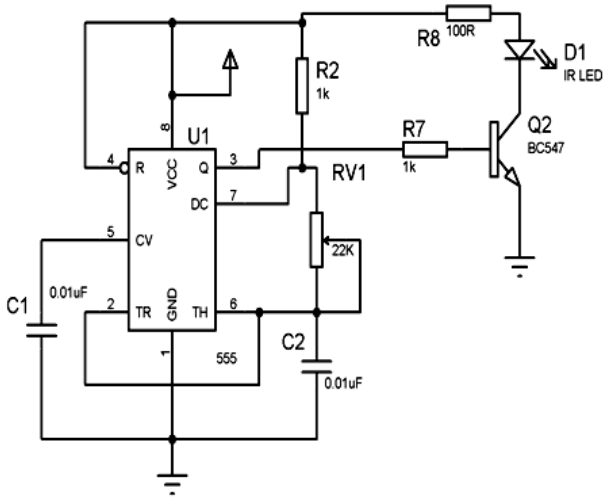
Introduction : IR Obstructer using 555 Timer, IC 555 Tester

Prerequisite knowledge for Complete understanding and learning of Topic:
Operation of Op Amp, Basic Analog electronics and Electronic Devices, and Circuit theory

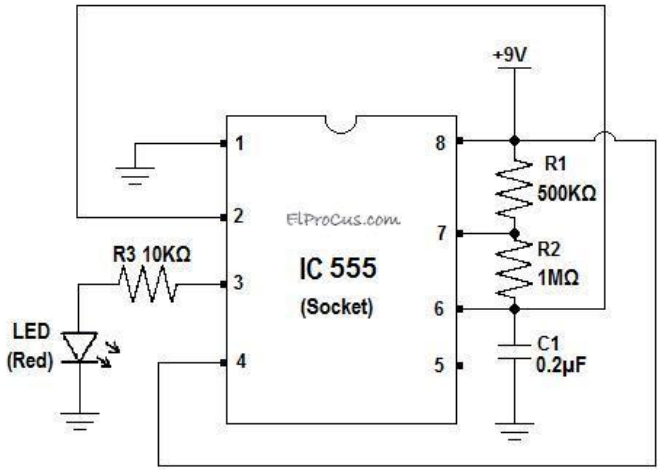
Applications of 555 Timers

1. IR Obstructer using 555 Timer

From the below circuit, here we are using 555timer where pin1 is connected to ground (GND) and pin2 is connected to pin6 which is threshold pin of timer. The pin3 is connected to base of a transistor BC547 whose emitter is connected to GND and collector is connected to power supply through IR diode / LED D1 and a Resistor. The pin4 of timer is connected to pin7 through resistor R2 of 1k again pin7 and pin5 are shorted together in between two capacitors C1 of 0.01µF, C2 of 0.01µF and a potential divider of 2.2k. The pin8 of the timer is connected to power supply. In this, the 555 timer used is in free running astable multi-vibrator mode at a frequency of 38 KHz and a duty cycle of about 60%. The said pulses drives a transistor Q2 the collector of which powers an IR diode D1 through 100Ω resistor from the power supply 6V DC. As the receiving unit of any T.V receives 38KHz pulses from its own remote, continuous stream of 38KHz pulses so generated by an external timer circuit superimposes and overrides the remote signal resulting in making the T.V remote sent pulses scrambled. Thus the T.V is not able to respond the required pulses from the T.V remote to take any action such as channel change, volume up, down etc.



2. IC 555 Tester:



The circuit is arranged as an astable multivibrator with R1 as 500 kilo ohm resistor (1/4 watt), R2 as 1 mega ohm resistor (1/4 watt) and C1 as 0.2 micro farad capacitor (ceramic bipolar). Connect this circuit with an empty 8 pin socket in place of the IC 555 so that you can easily attach the IC to be tested. Connect a power supply of 9v. You can use either a 9V adapter or else a 9V PP3 battery will work too. The resistors R1, R2 and C1 in the circuit above are used to set the frequency of operation of this circuit.

Video Content / Details of website for further learning (if any):

Can be added as link
https://www.elprocus.com/555-timer-pin-description-applications/

Important Books/Journals for further learning including the page s

Linear Integrated Circuits By D. Roy Choudhury, Shail B. Jain T1

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LECTURE HANDOUTS

MDE

II/IV

Course Name with Code : 19MDC04 – LOGIC CIRCUITS FOR CLINICAL ENGINEERS

Course Faculty : Mrs.M.Birunda

Unit : V – Specialized IC Applications

Date of Lecture:

Topic of Lecture: Voltage Regulators

Introduction : Voltage Regulator, as name suggests, is a circuit which is used to regulate the voltage. Regulated voltage is smooth supply of voltage, free from any noise or disturbance. The output from voltage regulator is independent of load current, temperature and AC line variation.

Prerequisite knowledge for Complete understanding and learning of Topic:

Operation of Op Amp, Basic Analog electronics and Electronic Devices, and Circuit theory

Voltage Regulators

Voltage regulator **minimizes the variation in voltage** to protect the device. In electrical distribution system, the voltage regulators are either in feeder lines or at substation.

Types of Voltage Regulator Circuit

Linear Voltage Regulator Circuit

- Series Voltage Regulator
- Shunt Voltage Regulator

Zener Voltage Regulator Circuit

Switching Voltage Regulator Circuit

- Buck type
- Boost type
- Buck/Boost type

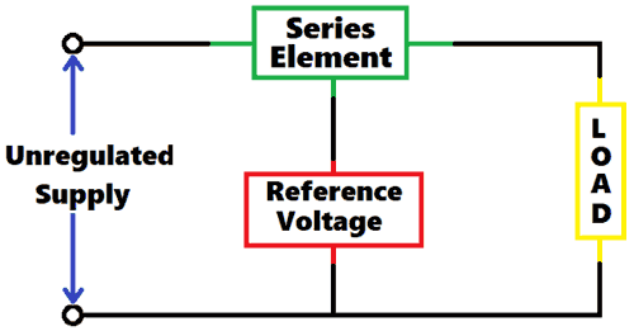
Linear Voltage Regulator Circuit

These are the most common regulators used in electronics to maintain the steady output voltage. Linear voltage regulators acts like a voltage divider circuit, in this regulator resistance varies with respect to change in load and gives constant output voltage.

1. Series Voltage Regulator

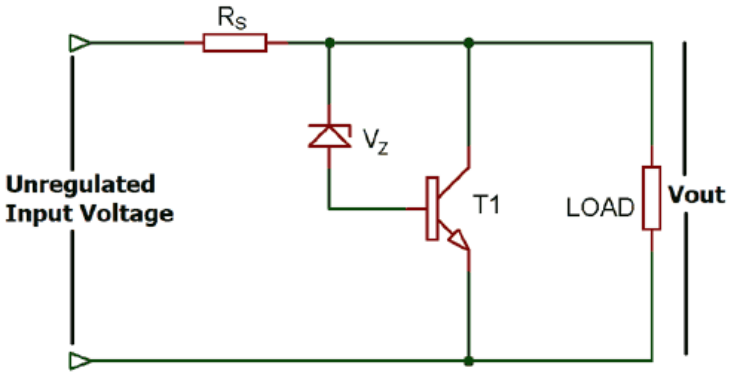
Series Voltage Regulator is a part of Linear Voltage Regulator and also called as Series Pass

Regulator. A variable element connected in series, used for maintaining constant output voltage. As you change the resistance of series element voltage drop across it can be varied to ensure that the voltage across output is constant.



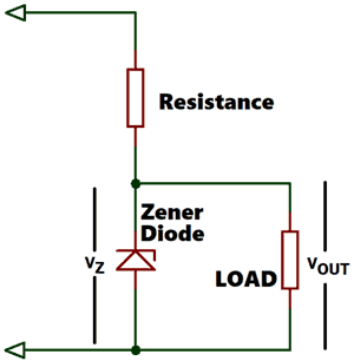
2. Shunt Voltage Regulator

The unregulated voltage is directly proportional to the voltage drop across the resistance connected in series and this voltage drop depends upon the current consumed by the load. If the current consumption of load increases the base current will also decrease and due to this less collector current will flow through the collector emitter terminal and hence the current through load will increase and vice versa.



Zener Voltage Regulator

Zener Voltage Regulators are cheaper and only suitable for low power circuits. It can be used in applications where the amount of power wasted during regulation is not of major concern.



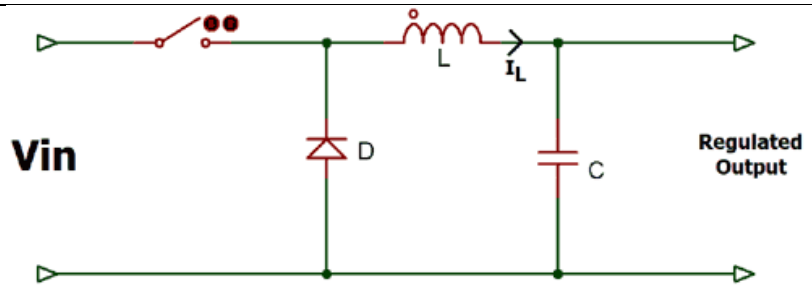
Switching Voltage Regulator

There are three types of switching voltage regulator:

- Buck or Step-Down Switching Voltage Regulator
- Boost or Step-Up Switching Voltage Regulator
- Buck / Boost Switching Voltage Regulator

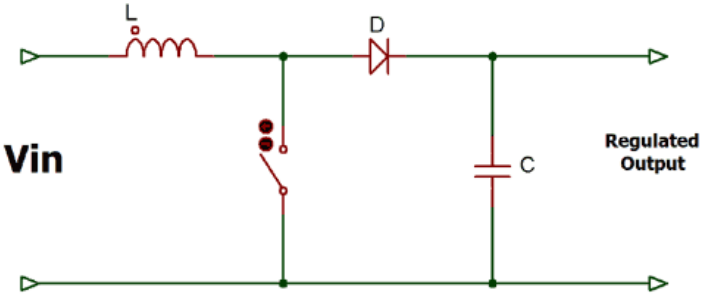
Buck or Step-Down Switching Voltage Regulator

A Buck Regulator is used to step down the voltage at the output, we can even use the voltage divider circuit to reduce the output voltage but the efficiency of voltage divider circuit is low, because resistors dissipates energy as heat.



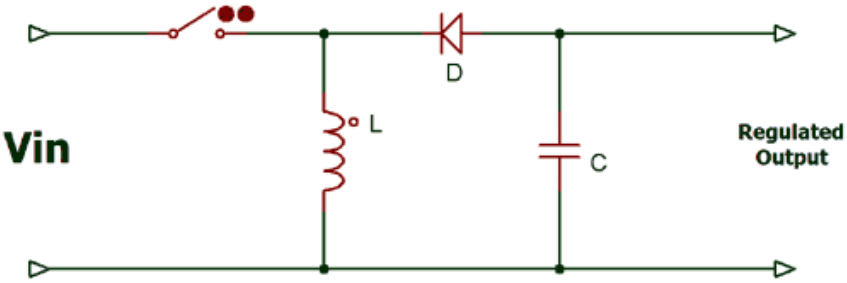
Boost or Step-Up Switching Voltage Regulator

The Boost Regulator is used to step-up the voltage across the load.



Buck-Boost Switching Voltage Regulator

Buck-Boost Switching Regulator is the combination of both Buck and Boost Regulator, it gives inverted output which can be greater or less than the supplied input voltage.



Video Content / Details of website for further learning (if any):

Can be added as link

https://www.youtube.com/watch?v=GSzVs7_aW-Y
https://www.youtube.com/watch?v=rPb0p7N1O00
https://circuitdigest.com/electronic-circuits/voltage-regulators

Important Books/Journals for further learning including the page nos.:

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LECTURE HANDOUTS

MDE

II/IV

Course Name with Code : 19MDC04 – LOGIC CIRCUITS FOR CLINICAL ENGINEERS

Course Faculty : Mrs.M.Birunda

Unit : V – Specialized IC Applications

Date of Lecture:

Topic of Lecture: Fixed and Adjustable voltage regulators

Introduction : Some regulators, such as the LM317, allow the designer to select a desired output voltage based on an external resistive-divider. They are called adjustable. The major difference between the fixed and adjustable regulators is the place where the resistors are, inside or outside the chip.

Prerequisite knowledge for Complete understanding and learning of Topic:

Operation of Op Amp, Basic Analog electronics and Electronic Devices, and Circuit theory

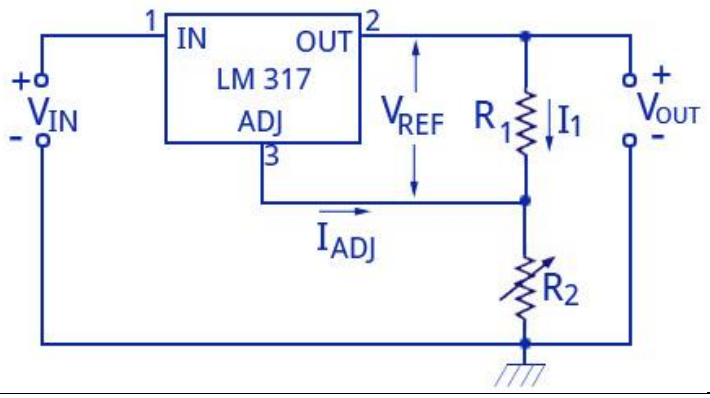
Fixed Voltage Regulators

These regulators provide a constant output voltage. A popular example is the 7805 IC which provides a constant 5 volts output. A fixed voltage regulator can be a positive voltage regulator or a negative voltage regulator. A positive voltage regulator provides with constant positive output voltage.

Adjustable Voltage Regulator

An adjustable voltage regulator is a kind of regulator whose regulated output voltage can be varied over a range. There are two variations of the same; known as positive adjustable voltage regulator and negative adjustable regulator. LM317 is a classic example of positive adjustable voltage regulator, whose output voltage can be varied over a range of 1.2 volts to 57 volts.

ADJUSTABLE VOLTAGE REGULATOR USING LM 317



The resistors R1 and R2 determine the output voltage Vout. The resistor R2 is adjusted to get the output voltage range between 1.2 volts to 57 volts. The output voltage that is required can be calculated using the equation:

Vout = Vref (1+R2/R1) + Iadj R2

Video Content / Details of website for further learning (if any):

Can be added as link
http://www.circuitstoday.com/ic-voltage-regulators

Important Books/Journals for further learning including the page nos.:

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LECTURE HANDOUTS

MDE

II/IV

Course Name with Code : 19MDC04 – LOGIC CIRCUITS FOR CLINICAL ENGINEERS

Course Faculty : Mrs.M.Birunda

Unit : V – Specialized IC Applications

Date of Lecture:

Topic of Lecture: Dual Power Supply

Introduction : Dual power supply units are common equipment in electrical engineering and electronics. They supply positive polarity (+Vcc) as well as negative polarity (-Vcc, not connected to ground!) and ground potential. In particular cases both the positive and negative rails are required for the proper operation of your circuit.

Prerequisite knowledge for Complete understanding and learning of Topic:

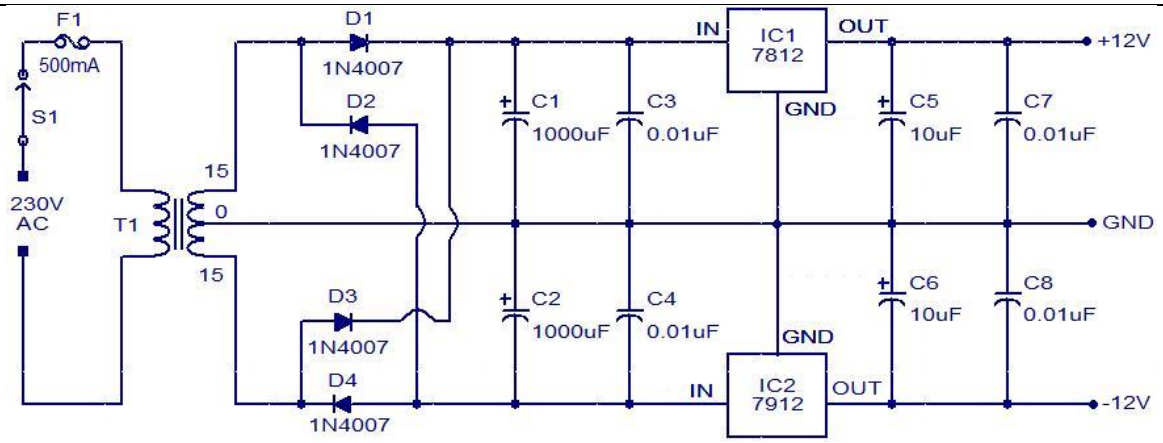
Operation of Op Amp, Basic Analog electronics and Electronic Devices, and Circuit theory

Dual Power Supply Circuit

Description

The circuit given here is of a regulated dual power supply that provides +12V and -12V from the AC mains. A power supply like this is a very essential tool on the work bench of an electronic hobbyist.

The transformer T1 steps down the AC mains voltage and diodes D1, D2, D3 and D4 does the job of rectification. Capacitors C1 and C2 does the job of filtering.C3, C4, C7and C8 are decoupling capacitors. IC 7812 and 7912 are used for the purpose of voltage regulation in which the former is a positive 12V regulator and later is a negative 12V regulator. The output of 7812 will be +12V and that of 7912 will be -12V.



Video Content / Details of website for further learning (if any):

Can be added as link
http://www.circuitstoday.com/regulated-dual-power-supply-circuit
https://www.youtube.com/watch?v=WVE4jklXD74

Important Books/Journals for further learning including the page nos.:

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LECTURE HANDOUTS

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II/IV

Course Name with Code : 19MDC04 – LOGIC CIRCUITS FOR CLINICAL ENGINEERS

Course Faculty : Mrs.M.Birunda

Unit : V – Specialized IC Applications

Date of Lecture:

Topic of Lecture: Universal Active Filter

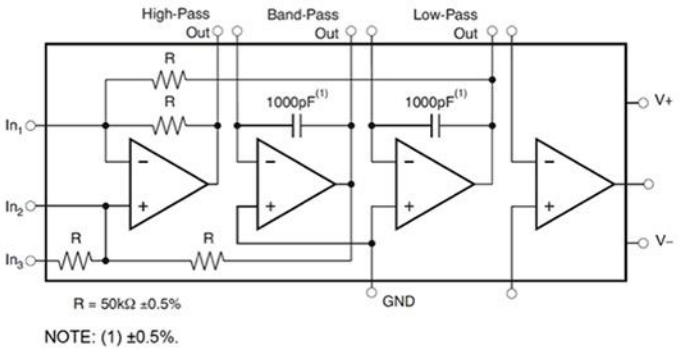
Introduction : Continuous signal active filters are implemented using operational amplifiers with resistor/capacitor (RC) passive elements. Several integrated circuit suppliers offer universal active filters containing the op-amps and critical RC components to simplify filter design and fabrication.

Prerequisite knowledge for Complete understanding and learning of Topic:

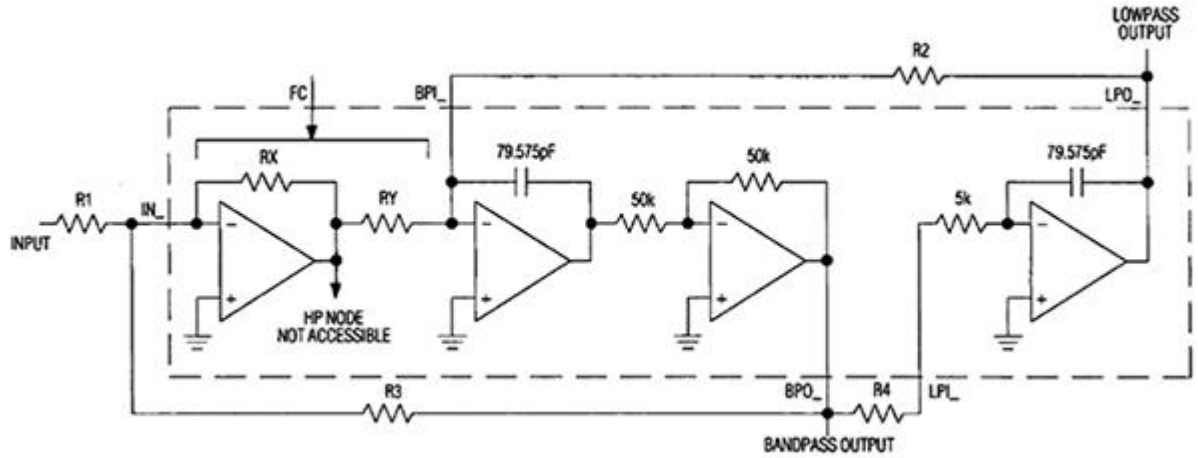
Operation of Op Amp, Basic Analog electronics and Electronic Devices, and Circuit theory

Universal Active Filter

This universal filter uses a classic state variable topology employing three operational amplifiers - two as integrators and a third as a summer. A fourth, uncommitted, op-amp is included to provide design flexibility (Figure 5). Each of these ICs offers a two-pole or second-order filter element with a maximum pass-band of 100 kHz.



Maxim Integrated offers universal active filters with up to four second-order sections per device. The MAX274 includes four sections of second-order state variable filter blocks. The MAX274 offers a maximum bandwidth of 150 kHz. All four sections can be cascaded to create up to an eighth-order filter.



All of these universal filter integrated circuits can be configured with Butterworth, Bessel, or Chebyshev responses. Most can be designed as any of the common filter types: low-pass, high-pass, band-pass, or band-stop.

Video Content / Details of website for further learning (if any):

Can be added as link
https://www.digikey.in/en/articles/techzone/2017/nov/use-monolithic-universal-active-filter-ics-to-speed-iot-analog-front-end-design

Important Books/Journals for further learning including the page nos.:

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II/IV

Course Name with Code : 19MDC04 – LOGIC CIRCUITS FOR CLINICAL ENGINEERS

Course Faculty : Mrs.M.Birunda

Unit : V – Specialized IC Applications

Date of Lecture:

Topic of Lecture: Switched Capacitor filter

Introduction : A switched capacitor (SC) is an electronic circuit element implementing a filter. It works by moving charges into and out of capacitors when switches are opened and closed. Usually, non-overlapping signals are used to control the switches, so that not all switches are closed simultaneously.

Prerequisite knowledge for Complete understanding and learning of Topic:

Operation of Op Amp, Basic Analog electronics and Electronic Devices, and Circuit theory

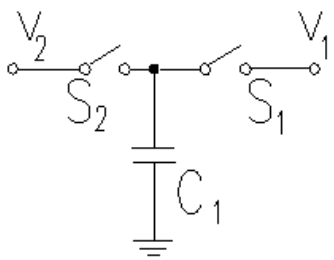
Switched Capacitor Circuits

In the last decade or so many active filters with resistors and capacitors have been replaced with a special kind of filter called a switched capacitor filter. The switched capacitor filter allows for very sophisticated, accurate, and tuneable analog circuits to be manufactured without using resistors. This is useful for several reasons.

Chief among these is that resistors are hard to build on integrated circuits (they take up a lot of room), and the circuits can be made to depend on ratios of capacitor values (which can be set accurately), and not absolute values (which vary between manufacturing runs).

The Switched Capacitor Resistor

To understand how switched capacitor circuits work, consider the circuit shown with a capacitor connected to two switches and two different voltages.



The Switched Capacitor Integrator

Now consider the integrator circuit. You have shown (in a previous lab) that the input-output relationship for this circuit is given by (neglecting initial conditions):

$$v_o(t) = -\frac{1}{RC_2}\int v_i(t)dt = -\omega\int v_i(t)dt$$

Video Content / Details of website for further learning (if any):

Can be added as link

http://www.swarthmore.edu/NatSci/echeeve1/Ref/FilterBkgrnd/SwitchedCap.html

Important Books/Journals for further learning including the page nos.:

Linear Integrated Circuits By D. Roy Choudhury, Shail B. Jain T1

Course Faculty

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